Analog Layout

Device Matching

- Why do I care?
- Matching 'theory'
- Basic approach for transistors, capacitors, resistors

Noise and Decoupling

- Capacitive coupling
- Substrate noise
- Thermal noise
- Shielding

Floorplanning

- Board and package considerations
- Placement of blocks

Matching

Analog designers think a lot about matching:

- Basic operation of some circuits depends directly on matching

  eg. pipelined A/D converters
- Common-mode rejection limited by matching

  Common-mode to differential-mode conversion is proportional to mismatch
- Supply noise rejection limited by mismatch in fully-differential circuits

  In fully-differential circuits supply noise appears like a common-mode signal applied to the supply
- Amplifier offsets greatly degrade the performance of bandgap references

Digital designers also care about matching of transistors and routing because of skew and in memories.

Matching Theory

Two papers on reserve by M. Pelgrom present measured data and statistical calculations to predict random mismatch in various CMOS technologies.

Basic idea: if you have a collection of nominally identical devices and you did everything right in laying them out, they will have a β and a V_T mismatch of:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2$$

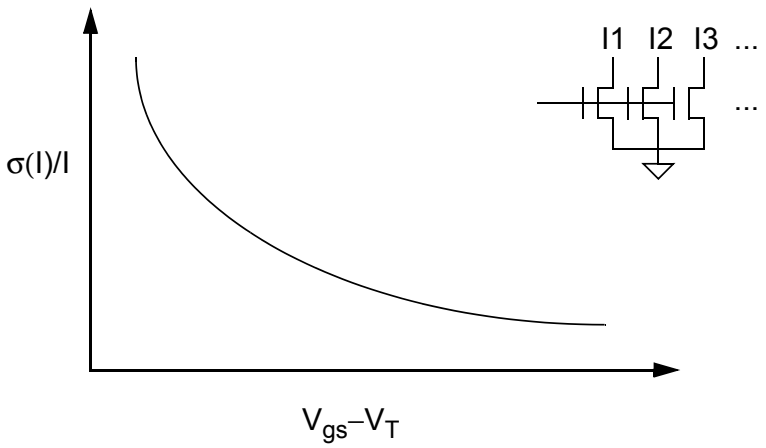
$$\sigma^2(V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2$$

where A_β, A_{VT}, S_β, and S_{VT} are technology dependent constants and D is the separation between the devices. The second term in the equation is typically not significant except over very large distances and for large transistors.

The key idea is the square-root dependence of the standard deviation of mismatch factors with respect to the area of the device. For a 0.6-μm process, you can assume A_{VT} = 20mVμm and A_β = 2%μm.

Matching vs. Bias

For a collection of nominally identical current sources, mismatch in the drain currents is bias dependent. V_T mismatch has a larger effect at low bias levels while β mismatch dominates at high currents. So, don't let Vgs-V_T drop too much if you need good matching! In general, it's good to keep it above 200mV.



The Golden Rules of Matching

If you follow some simple rules, you can avoid gross matching problems. If you're trying to ratio two transistors

- Use the same W and L and vary M (takes out ΔW and ΔL effects)
- Use M's that are even, preferably factors of 4 (transistors are not truly symmetrical!)
- Use common-centroid, or nearly common-centroid, layout (takes out oxide and doping gradients)
- Use dummy transistors at the ends of the row (takes out poly etch loading and mask misalignment effects)
- Make clean and well balanced routing
- Use a suitable area and overdrive
- Use plenty of substrate and well taps
- Route currents a long way, not voltages - IR drops can cause big mismatches

Systematic Mismatch

Systematic mismatch refers to a spatial gradient in component values. It is very undesirable: it can be very large and swamp out random mismatch, it can cause various circuit problems such as harmonic distortion in A/D converters, while random mismatch is usually somewhat more benign in its impact on higher level specs.

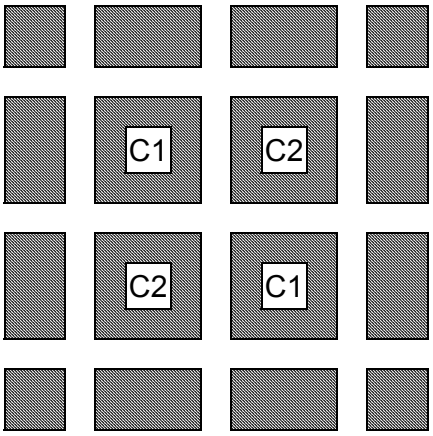
Systematic mismatch can be caused by processing gradients and inadequate layout. Follow the rules of matching.

Imbalanced loads can look like a systematic mismatch: eg. the strobe signal in an edge triggered regenerative latch can easily imbalance the circuit by 100mV! This is hard to distinguish from a static offset in the test lab although it is a dynamic effect.

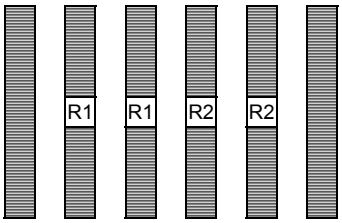
A good test of the symmetry of routing is a power supply rejection simulation on the back annotated netlist.

Matching Capacitors and Resistors

To match caps and resistors, use unit cells and dummy edge devices



A 2x2 capacitor array with dummy cells along the edges
C1 and C2 are composed of 2 unit cells
Make sure routing has identical effects

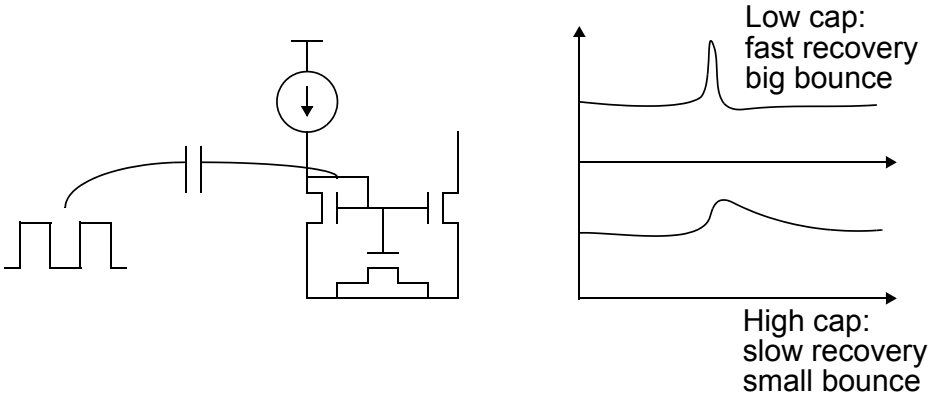


Two poly resistors, not common-centroid to make routing cleaner
Don't forget about the resistance of the contacts - use identical contact geometries
To get ratios use parallel/series rather than varying W or L

Noise and Decoupling

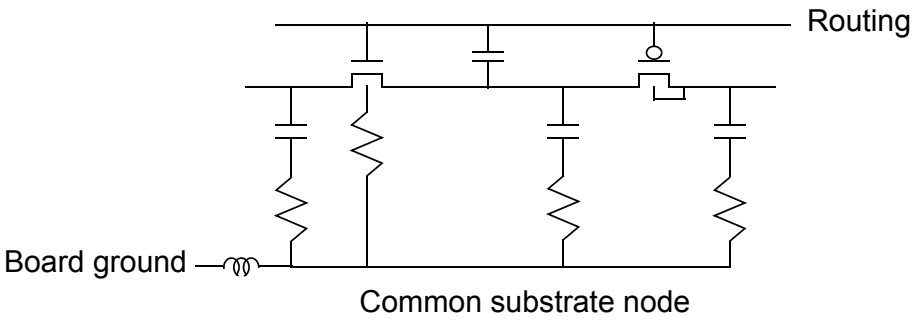
Most common form of noise coupling is capacitive coupling through neighboring wires such as clocks.

Noise can couple into bias nodes and signal node. For bias nodes, use decoupling capacitors to reduce the amplitude of noise coupling in. But, if noise is deterministic and occurs at the right point in time, you might be better off not decoupling, but making the bias node fast so it can recover quickly.



Substrate Noise

Noise can couple from one end of a chip to the other even if there are no wires to carry the noise: it can go right through the substrate! An epitaxial substrate can be viewed as a single node connecting all transistors to each other. A very simple, low frequency, model is

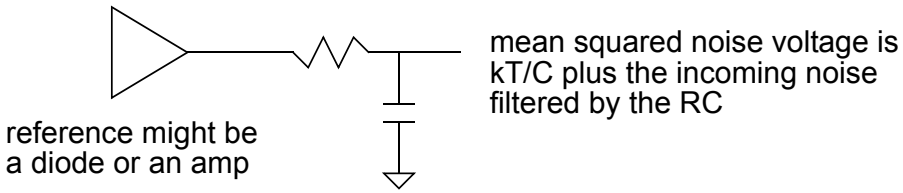


Well and diffusion guard rings don't help that much because they only penetrate the first few microns of the substrate, which is hundreds of microns deep.

Bulk substrates are much more complicated to model and tricky to use. The single node substrate model does not apply.

Thermal Noise

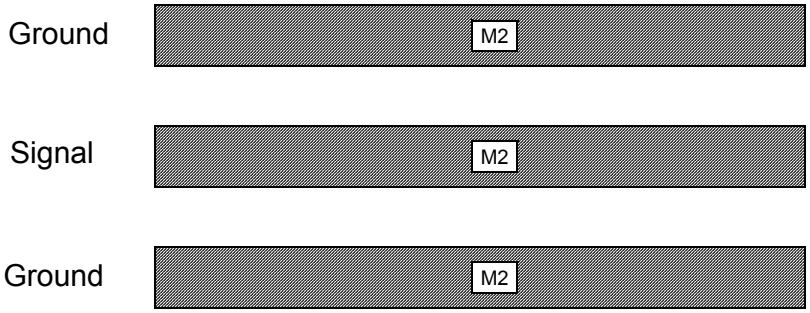
A common approach to reducing noise on a line is to filter is using an RC network. The mean squared thermal noise across the capacitor is kT/C, so just make the capacitor big enough and forget about the thermal noise, right?



Maybe. In some circuits, we also care about noise density at a particular frequency. In that case, the value of R is also important. The point is that noise is hard to estimate and get rid of and the cure sometimes hurts more than the disease, so tread carefully.

Noise Coupling into Single-Ended Signals

With single-end signals, the best you can do is to minimize the amount of noise coupling. Once noise gets in, it's indistinguishable from the signal. Critical nodes should be shielded and routed away from noisy circuits



Can also have a shield layer underneath, such as poly or diffusion. This is a very useful technique but can also get you in trouble. If the impedance of the shields to ac ground gets high, they will actually degrade the performance by making coupling stronger! Unfortunately, shields increase loading and slow the circuit.

Finally, be sure to shield with whatever the signal is referenced to (gnd or vdd.)

Noise Coupling into Differential Signals

With differential signals, it's important to both minimize the noise coupling and to make the coupling equal into both halves of the signal.

Any noise that appears on both components of a differential signal appears as a common-mode signal and gets attenuated by the common-mode rejection of the subsequent circuits.

So, use shielding as before, and when a signal crosses one of the differential signals, make it cross the other one too. Always route differential signals together.

Generally, it's desirable to use a high metal layer to carry signals to reduce the coupling into them and to minimize the loading. Of course, in a two metal process, your options are somewhat limited.

Final bit of advice: know when to stop! You can easily get so carried away with these issues that your layout takes a very long time to complete. The key is to do what is right for an application. An RF mixer should minimize capacitance, but a 14-bit A/D converter needs well a very balanced layout. Use your judgement and ask questions.

Shielding Noise Generators

There isn't an awful lot you can do about noisy signals. One somewhat helpful trick is to put a floating well under clock busses. The well provides some measure of isolation by placing a series capacitor in the noise path. Since both the well and the substrate are lightly doped, the capacitance per unit area is low. However, there ends up being so much well, that the total amount of capacitance is still somewhat large.

Physical separation of noisy signals from sensitive ones reduces the direct capacitive coupling, but does not help with substrate coupling in epi silicon.

Multiple supply domains reduce the amount of noise on the power supplies of sensitive circuits. Also, heavily bypassing the analog and digital supplies with capacitors is useful. Note that if the series resistance of the capacitors is too high, they won't be of much help at high frequencies.

Watch out for the LCR tanks formed by bypass capacitance, bond wire inductance, and bondwire and routing resistance. Ringing on the supplies is sure to be disastrous for most designs!

Floorplanning

A common mistake is to do a great job of laying out lots of little cells but then make a big mess when pulling the design together. A good floorplan is essential to being able to quickly make a good layout with few iterations.

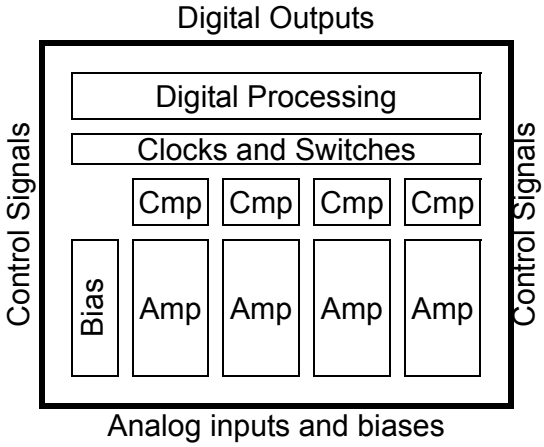
A floorplan is an evolving document that helps the designer organize the chip into pieces that fit together well. Don't be afraid to change it as you go along and discover new issues, just start out with one so you don't miss the obvious things that can be very painful later.

When generating a floorplan, keep the ultimate test setup in mind. If you have to cross sensitive and noisy signals, it's best to do it on chip where you only get a few femto Farads of coupling rather than doing it on the board where you will get much more coupling.

Bond wire and package traces have inductance and resistance. By putting multiple pins in parallel, you can reduce these parasitics. However, mutual inductance of neighboring pins fights the reduction. The inductance of two adjacent pins is about 0.7 times that of one, and for three pins, you get about 0.5 times the inductance of one pin.

Floorplanning: Placement of Blocks

A/D Example:



Separates analog and digital as much as possible, divides board into analog and digital sides, uses normally inactive digital control signals and supplies between analog and digital pins.