A Comprehensive Analysis of IMD Behavior in RF CMOS Power Amplifiers

Christian Fager, *Member, IEEE*, José Carlos Pedro, *Senior Member, IEEE*, Nuno Borges de Carvalho, *Member, IEEE*, Herbert Zirath, *Member, IEEE*, Fernando Fortes, and Maria João Rosário, *Member, IEEE*

***Abstract*—This paper presents a comprehensive analysis of nonlinear intermodulation distortion (IMD) behavior in RF CMOS power amplifiers (PAs). Separate analyses are presented for small- and large-signal operation regimes. Especially, a new, simple, large-signal behavioral IMD analysis method is presented that allows the mechanisms dominant for IMD generation to be identified and their individual contributions to be studied. By combining these analyses, typical IMD versus input power characteristics of MOSFET PAs can be predicted and understood for different classes of operation.**

Various measurements made on a 950-MHz RF CMOS PA are used to demonstrate typical behavior and validate the proposed theory. Prediction of IMD using a standard CMOS transistor model is also evaluated and is shown to give good agreement with the measurements.

***Index Terms*—CMOS, distortion, intermodulation, large-signal, modeling, power amplifiers, two-tone measurements.**

I. Introduction

THE advances in CMOS technology for high-frequency applications have made it a natural choice for integrated low cost RF power amplifiers (PA) in mass-market wireless front-end applications [1]–[3].

These applications often make use of both amplitude and phase modulation. Thus, minimization of intermodulation distortion (IMD) in the RF front-end transceiver parts is of great importance for maximizing overall system performance. To understand how IMD is generated in such components, analytical analysis methods are required.

In the receiver, the mixer, or RF sampler, and the low-noise amplifier (LNA) are the most critical parts. Since the operating power level is usually low, the IMD can be successfully analyzed using low-order Volterra series [4]–[6].

In the transmitter, on the other hand, the amplifiers are operated at high power levels. Since efficiency is important, they are usually biased close to turn-on, for class-AB operation. In this case, the signals can no longer be considered as small perturbations of a fixed bias point and a true large-signal IMD analysis is necessary.

Still, existing analyses presented for IMD behavior in RF CMOS PAs are all based on the weak nonlinearity assumption [3], [4], [7], [8]. Weak nonlinearity figures of merit, like extrapolated third-order intercept point (IP3) are also being used to characterize PA IMD performance. True large-signal IMD is simulated using numerical methods, e.g., harmonic balance or transient analysis, which reveals no information about the origins of the IMD simulation results obtained.

In this paper, both the small- and large-signal IMD behavior of MOSFET-based PAs are treated using analytical methods. First, after discussing the general nonlinear operation of PAs, the small-signal IMD behavior is investigated in detail. Thereafter, for large-signal operation, the amplifier is represented by a transfer function (TF). The TF is the output current as function of the input voltage along the load line where the PA is operated, and describes the mechanisms dominant for IMD generation. By approximating the TF by a piecewise function, a simple analytical large-signal IMD analysis is developed where the individual contributions to the overall large-signal IMD behavior in PAs can be studied. By combining these small- and large-signal IMD analyses, the overall IMD versus input power characteristics can be explained and understood for different classes of operation.

Finally, for demonstration purposes, various measurements on a 950-MHz CMOS PA are made to illustrate typical IMD behavior and validate the presented theory. Predictions of IMD using the industry standard BSIM3v3 model are also investigated.

II. PA Nonlinear Operation

Since the source and body terminals are normally connected, the PA circuit can be represented as shown in Fig. 1. (V_S, Z_S) is a frequency domain representation of the Thevenin equivalent circuit seen from the gate, which includes the MOSFET input parasitic elements, gate bias circuitry, and source matching network. (V_L, Z_L) play the same role for the load matching and drain bias circuitry.

A. PA Operation Regimes

In what follows, it is assumed that the dominant source of nonlinearity is the channel current, $i_{\mathrm{DS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}})$. This can be approximately represented as the product of one function describing the gate voltage dependence (turn-on transition)

Manuscript received January 28, 2003; revised July 22, 2003. This work was supported by The Swedish Foundation for Strategic Research, SSF, Chalmers Centre for High Speed Technology, CHACH, Vinnova, and the Portuguese Science Bureau, FCT, under the Project LDMOSCA.

C. Fager and H. Zirath are with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Göteborg, Sweden (e-mail: christian.fager@mc2.chalmers.se; herbert.zirath@mc2.chalmers.se).

J. C. Pedro and N. Borges de Carvalho are with the Telecommunications Institute, University of Aveiro, Aveiro 3810-193, Portugal (e-mail: jcpedro@ieee.org; nborges@det.ua.pt).

F. Fortes and M. J. Rosário are with the Telecommunications Institute, Technical University of Lisbon, 1049-001 Lisbon, Portugal (e-mail: mrosario@ex.it.pt).

Digital Object Identifier 10.1109/JSSC.2003.820860

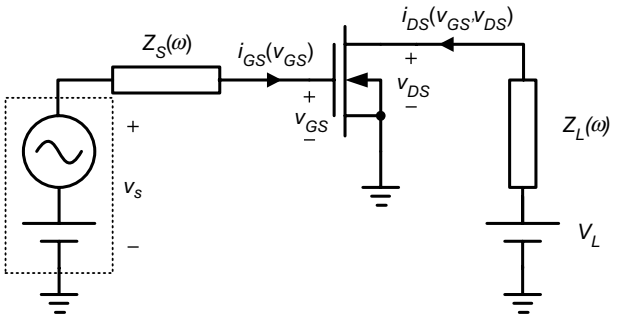


Fig. 1. Equivalent circuit diagram of the MOSFET PA for nonlinear analysis.

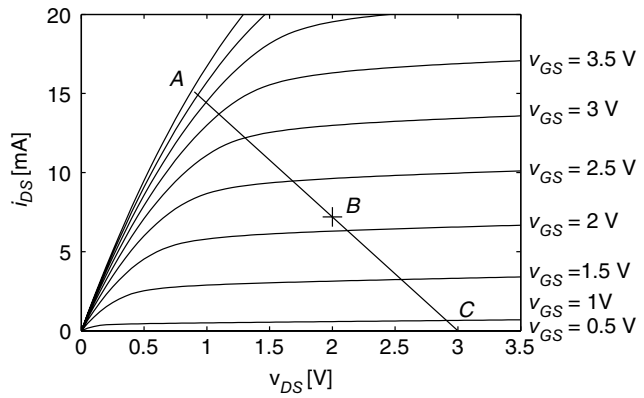


Fig. 2. Typical MOSFET $i_{\rm DS}$ versus $v_{\rm DS}$ characteristic and PA load line (ABC) for a resistive load impedance. B is the bias point and A and C are at the linear region and current turn-on, respectively.

and another function describing the drain voltage dependence (linear-to-saturation transition):

$$i_{\rm DS}(t) = \beta \ln\left[1 + e^{K_G(v_{\rm GS}(t) - V_T)}\right] \cdot v_{\rm DS,eff}(t) \tag{1}$$

where

$$v_{\rm DS,eff}(t) = V_{\rm dsat} - \frac{1}{2}\left[V_{\rm dsat} - v_{\rm DS}(t) - \delta + \sqrt{(V_{\rm dsat} - v_{\rm DS}(t) - \delta)^2 + 4\delta V_{\rm dsat}}\right]. \tag{2}$$

In these expressions, $\beta, K_G, V_T, V_{\rm dsat}$, and δ are fitting constants. This is also, to a first approximation, the expression used in the BSIM3v3 model [9]. A typical MOSFET dc characteristic is shown in Fig. 2.

Assuming $C_{\rm gs}$ is an approximately constant capacitance, the gate current is given by

$$i_{\rm GS}(t) = C_{\rm gs}\frac{dv_{\rm GS}(t)}{dt}. \tag{3}$$

The boundary conditions imposed on the transistor terminal voltages by the source and load are given by

$$v_{\rm DS}(t) = V_L - z_L(t) * i_{\rm DS}(t) \tag{4}$$

$$v_{\rm GS}(t) = v_S(t) - z_S(t) * i_{\rm GS}(t) \tag{5}$$

where $*$ denotes convolution. $v_S(t)$ is the time domain representation of V_S, while the time-dependent $z_S(t)$ and $z_L(t)$ play the same role for Z_S and Z_L, respectively. Together with the expressions for $i_{\rm DS}(t)$ and $i_{\rm GS}(t)$, these equations determine the load line trajectory and, thus, the nonlinear operation of the PA. The load line obtained for a typical PA with a resistive load impedance is shown in Fig. 2 [10].

Two different operation regimes can now be identified. In the small-signal regime, the excitation $v_S(t)$ has relatively small amplitude. Then, $i_{\rm DS}(t)$ amplitude is also quite small, and thus $v_{\rm DS}(t)$ represents only a small perturbation of V_L, the drain bias voltage (B in Fig. 2). Therefore, the MOSFET does not leave saturation region $(v_{\rm DS,eff} \approx V_{\rm dsat})$ and the PA nonlinear characteristics are almost completely determined by the gate voltage dependence.

In the large-signal regime, $v_S(t)$ has a large amplitude. $v_{\rm GS}(t)$ and $v_{\rm DS}(t)$ then also have wide signal excursions, implying that the device's channel current excursion has its lower and upper limits determined by turn-on (C in Fig. 2) and linear region (A in Fig. 2), respectively.

B. PA Nonlinear Distortion Phenomena

In RF applications, nonlinear distortion is usually studied using a two-tone test, in which the input signal may be expressed as

$$v_S(t) = A[\cos(\omega_1 t) + \cos(\omega_2 t)] \tag{6}$$

with A being the equal amplitude of the two sinusoidals.

In the RF wireless field, the in-band third-order intermodulation distortion (IM3),[1] which in a two-tone test appears in the output current spectrum as IMD sidebands at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, is of main interest. Additionally, this form of nonlinear distortion creates mixing products at ω_1 (e.g., $\omega_1 + \omega_1 - \omega_1$ and $\omega_1 + \omega_2 - \omega_2$) and ω_2 (e.g., $\omega_2 + \omega_2 - \omega_2$ and $\omega_2 + \omega_1 - \omega_1$) that appear exactly on top of the input frequency components. Depending on the sign of these, they are responsible for creating PA gain compression or expansion.

The amplitude, but also the phase of these IMD products, thus play a key role in explaining nonlinear PA behavior.

III. Small-Signal IMD Behavior

As seen from the preceding discussion, in the small-signal regime, the MOSFET's control voltages can be assumed as small perturbations of the bias point. Therefore, the assumptions for Volterra series analysis hold and the channel current can be expressed as the following bidimensional Taylor series, where only dominant terms are included:

$$i_{\rm DS}(v_{\rm GS}, v_{\rm DS}) \approx i_{\rm DS}(V_{\rm GS}, V_{\rm DS}) + \frac{\partial i_{\rm DS}}{\partial v_{\rm GS}}v_{\rm gs} + \frac{\partial i_{\rm DS}}{\partial v_{\rm DS}}v_{\rm ds} + \frac{1}{2}\frac{\partial^2 i_{\rm DS}}{\partial v_{\rm GS}^2}v_{\rm gs}^2 + \frac{1}{6}\frac{\partial^3 i_{\rm DS}}{\partial v_{\rm GS}^3}v_{\rm gs}^3 \tag{7}$$

or

$$i_{\rm DS}(v_{\rm GS}, v_{\rm DS}) \approx i_{\rm DS}(V_{\rm GS}, V_{\rm DS}) + g_m v_{\rm gs} + g_{\rm ds}v_{\rm ds} + g_{m2}v_{\rm gs}^2 + g_{m3}v_{\rm gs}^3. \tag{8}$$

[1]*Third-order* intermodulation distortion (IM3) is hereafter used as a general term for the IMD appearing closest to the carrier in a two-tone test, although this tone in fact contains IMD contributions from all orders greater than or equal to three when the input power is increased.

Hereafter, uppercase symbols, e.g., $V_{\rm GS}$, denote bias voltages and lowercase symbols, e.g., $v_{\rm gs}$, denote small-signal deviations. The total gate-to-source voltage, $v_{\rm GS}$, consequently represents $v_{\rm GS} = V_{\rm GS} + v_{\rm gs}$.

In the context of Volterra series, it is known that in-band two-tone IM3 nonlinear distortion products at $2\omega_1 - \omega_2$ have two origins. They are mainly generated by direct third-order mixing of input frequencies, $V(\omega_1) * V(\omega_1) * V(\omega_2)^*$, via the last term of (8) (here $*$ represents spectral convolution and superscript * the complex conjugate). The IM3 sign and magnitude is then determined by g_{m3} [11].

But small-signal IM3 can also arise by mixing second-order products at the second harmonic or the difference frequency with the inputs, i.e., $V(2\omega_1) * V(\omega_2)^*$ or $V(\omega_1) * V(\omega_1 - \omega_2)^*$ [11], [12]. However, the necessity of guaranteeing PA stability demands for low internal feedback, or nearly short circuit terminations at the out-of-band components, so that $V_{\rm gs}(\omega_1 - \omega_2)$ and $V_{\rm gs}(2\omega_1)$ amplitudes both become very low. Thus, in well-behaved PAs these contributions are normally small. Furthermore, since in small-signal regime all generated nonlinear components are already very small, mixing products generated by remixing nonlinear components will be negligible.

Fig. 3 presents measured and predicted values of the $i_{\rm DS}(v_{\rm GS})$ Taylor series expansion coefficients in (8) from a real MOSFET[2] ($W = 60\ \mu$m) biased in saturation at constant $V_{\rm DS}$. The extracted coefficients were obtained using measured harmonic and intermodulation levels [13], while the predicted values are the result of numerical differentiation of the accompanying BSIM3v3 nonlinear MOSFET model.

This is, to the best of our knowledge, the first time that the distortion prediction capabilities of the BSIM3v3 model are evaluated using dedicated derivative measurements. In that respect, it seems that it describes the weak device nonlinearities reasonably well. This is also verified in Fig. 4, where simulated and measured small-signal two-tone IM3 at $2\omega_1 - \omega_2$ versus gate bias are compared. A careful observation of Fig. 4 leads to the following conclusions for the MOSFET small-signal behavior.

First, measured IM3 approximately follows the shape of g_{m3}, although the discrepancy increases for higher $V_{\rm GS}$ bias. This was attributed to the gentle rise of $i_{\rm DS}$ that occurs in MOSFETs before breakdown, which was not very well described by the BSIM3v3 implementation used. However, since the measurements were made at a constant $V_{\rm DS}$ bias whereas, in practical PAs, $v_{\rm DS}$ is decreased for high $v_{\rm GS}$ along the load line trajectory (see Fig. 3), it seems that PA small-signal IM3 can still be predicted with enough accuracy by the BSIM3v3 model.

Second, small-signal nonlinearity decreases as $V_{\rm GS}$ bias is increased beyond turn-on, toward class-A operation. Note, however, that this may also lead to reduced available signal excursion and thus a compromise between optimized small-signal IMD and maximum class-A output power.

Third, in-band small-signal MOSFET nonlinearity presents a very high lobe near turn-on, followed by another lobe of smaller amplitude. This is evidence of the widespread knowledge that a FET presents a severe nonlinear regime near turn-on. Nevertheless, it also shows that, between the two lobes, there is a

[2]Austria Mikro Systeme (AMS) 0.6-μm CMOS process.

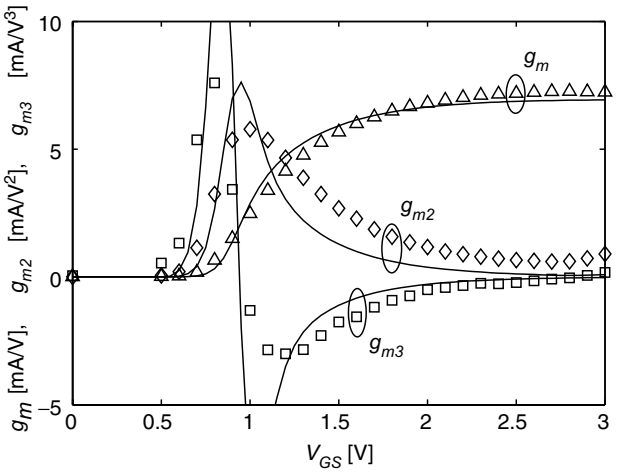


Fig. 3. $i_{\rm DS}(v_{\rm GS})$ Taylor series expansion coefficients, as measured (markers) on a real MOSFET ($W = 60\ \mu$m, $L = 0.6\ \mu$m) in saturation, and numerically differentiated (—) from the corresponding BSIM3v3 nonlinear device model at $V_{\rm DS} = 2.0$ V.

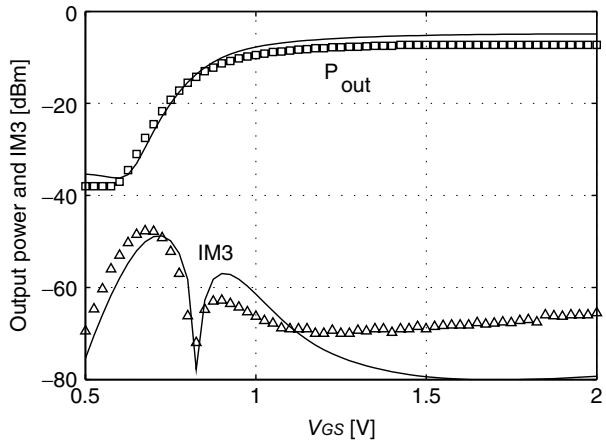


Fig. 4. Simulated (—) and measured (markers) small-signal output power and third-order IMD (IM3) versus gate bias voltage ($V_{\rm GS}$). Input power $= -20$ dBm and $V_{\rm DS} = 3$ V.

$V_{\rm GS}$ bias point having zero IM3. Unfortunately, this does not correspond to linearity but to an almost pure, although local, quadratic behavior (notice, in Fig. 3, that the highest value of g_{m2} indeed coincides with this null g_{m3}). This is, actually, an indication of the expected good in-band distortion performance presented by ideal class-B PAs. In practice, however, it has a limited value because the analysis was restricted to small-signals. If a larger signal excursion was considered, higher order contributions, e.g., of fifth or seventh orders, would become increasingly important, and those very good IMD values obtained for small-signals would rapidly deteriorate.

IV. Large-Signal IMD Behavior

Large-signal effects are noticed whenever any of the MOSFET's strong nonlinearities are traversed. As seen in Section II, in a typical MOSFET, those are identified as current turn-on and current saturation imposed by the load line reaching linear region. The preceding small-signal analysis, which was

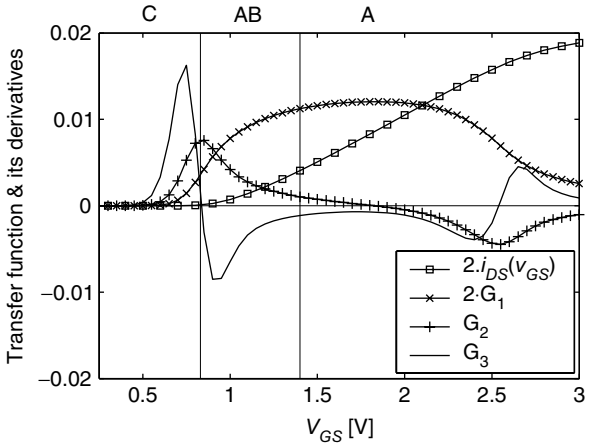


Fig. 5. Typical PA input-voltage/output-current transfer function and its derivatives versus input voltage bias $V_{\rm GS}$. Approximate bias ranges for different classes of operation are indicated in top of the figure. To enhance plot visibility, $i_{\rm DS}$ and G_1 are expanded with a factor 2.

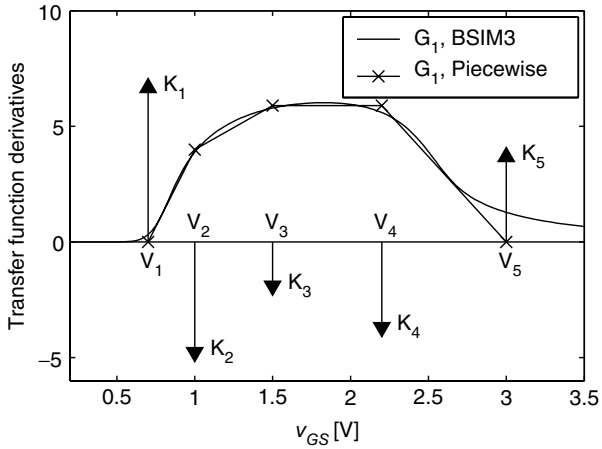


Fig. 6. Simulated first-order transfer function derivative G_1 and a piecewise linear approximation of it. The corresponding third-order derivative G_3 is a set of Dirac-delta functions as indicated by arrows in the figure.

based on a low-order Volterra series analysis, then becomes inappropriate.

This section focuses on understanding the dominant PA large-signal IMD behavior and mechanisms. For that, a simple analytical memoryless IMD model will be developed. Memory effects are addressed with the measurements in Section V.

A. Transfer Function Representation

For a given load impedance and drain bias, $v_{\rm DS}$ follows a fixed load line (see Fig. 2). The output current $i_{\rm DS}$ is then only dependent on the input voltage $v_{\rm GS}$, so that the PA can be represented by an equivalent input-voltage/output-current TF [12]. Fig. 5 shows the TF obtained as the numerical solution to (4) and (5) with the BSIM3v3 model and a resistive load impedance used for maximum output power [10]. The TF may be expanded in a Taylor series similar to (8), as follows:

$$i_{\rm DS}(V_{\rm GS}+v_{\rm gs}) = i_{\rm DS}(V_{\rm GS}) + G_1 v_{\rm gs} + G_2 v_{\rm gs}^2 + G_3 v_{\rm gs}^3 + \cdots \tag{9}$$

The resulting coefficients G_n are shown versus input voltage in Fig. 5.

When comparing the TF coefficients G_1 and G_3 to the device coefficients g_m and g_{m3} of Fig. 3 (where $V_{\rm DS}$ was held constant), the most obvious differences appear at higher input voltages. There, transconductance G_1 now collapses and two corresponding lobes in G_3 emerge. This is due to the $i_{\rm DS}$ compression when entering the linear region, which also causes PA output power compression.

As we will show in the following, this TF representation allows a simple analytical method for understanding the PAs' large-signal IMD behavior.

B. Analysis

First, it is noted that the contribution from the high-order terms in (9) becomes dominant for large input signals. Actually, these higher order components can still be expressed using the Taylor series by a residual term [14]:

$$i_{\rm DS}(V_{\rm GS}+v_{\rm gs}) = i_{\rm DS}(V_{\rm GS}) + G_1(V_{\rm GS})v_{\rm gs} + G_2(V_{\rm GS})v_{\rm gs}^2 + \frac{1}{2}\int_0^{v_{\rm gs}} (v_{\rm gs}-x)^2 G_3(x+V_{\rm GS})\,dx. \tag{10}$$

G_1 and G_2 are here taken at the bias point whereas G_3 is being integrated from the bias point $V_{\rm GS}$ to the instantaneous *large-signal* voltage deviation, $v_{\rm gs}$. Note that only the last, residual, term contributes to odd-order IMD.

The G_1 characteristic in Fig. 5 is now approximated by a piecewise linear function in order to allow for further analytical calculations. The resulting G_3 versus $v_{\rm GS}$ characteristic then becomes a set of Dirac-delta functions (impulses) centered at the G_1 breakpoints, with magnitudes equal to the change of slope in each of those (see Fig. 6).

In order to preserve analysis simplicity, a[illegible]ntuitive interpretation, a one-tone sinusoidal input signal is considered in the following analysis. As a matter of fact, several numerical tests have shown that the resulting one-tone third-harmonic distortion (HD3) is closely related to the IM3 behavior obtained in a two-tone test for a memoryless nonlinearity.

So we now consider a sinusoidal input signal of amplitude A:

$$v_{\rm GS}(t) = V_{\rm GS} + v_{\rm gs}(t) = V_{\rm GS} + A\cos(\omega t). \tag{11}$$

With G_3 expressed by impulses, the part of $i_{\rm DS}(t)$ generating third-order products ($i_{\rm DS,3}(t)$) can be expressed using the residual term in (10) as

$$i_{\rm DS,3}(t) = \frac{1}{2}\int_0^{A\cos(\omega t)} (A\cos(\omega t)-x)^2 \times \underbrace{\left(\sum_{i=1}^{N} K_i \delta(x+V_{\rm GS}-V_i)\right)}_{G_3} dx \tag{12}$$

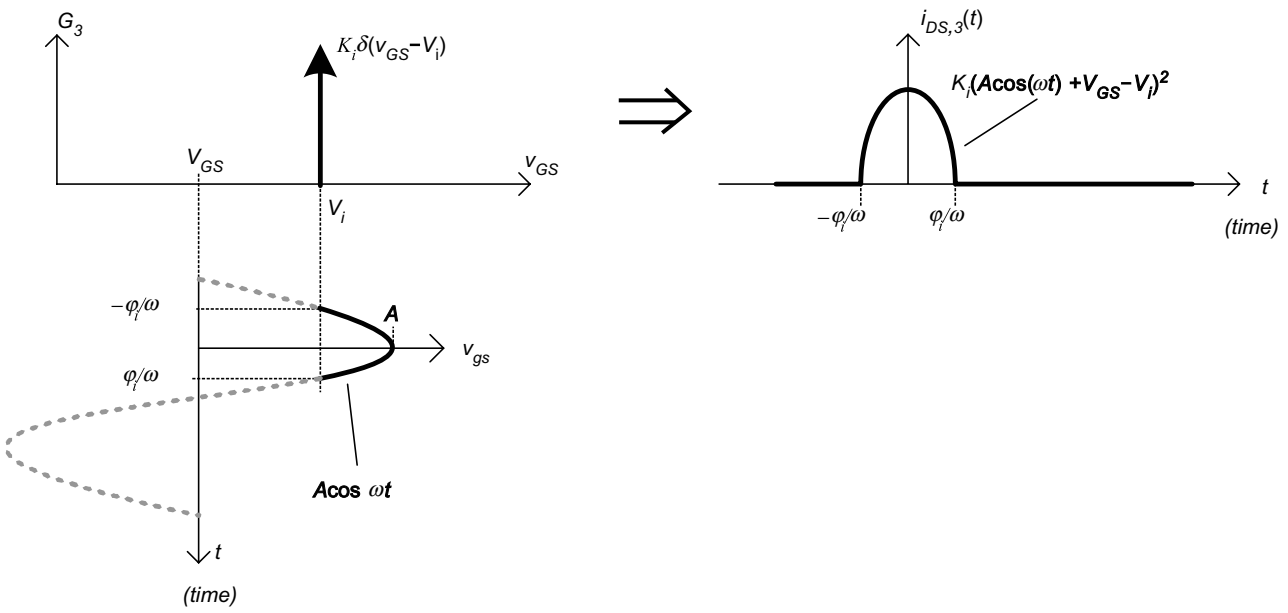


Fig. 7. Illustration of the time during which the input signal traverses the i'th impulse and, thus, contributes to $i_{\mathrm{DS},3}(t)$.

where K_i and V_i are the magnitude and voltage positions of the impulses $\delta(\cdot)$, respectively. The Dirac-delta functions have the property that the integral becomes equal to the integrand evaluated at the impulse positions, i.e., $x = V_i - V_{\mathrm{GS}}$. Impulses not traversed by the signal excursion give no contribution. The integration limit in (12) is, however, time varying according to the input signal. Thus, only the time when each impulse is traversed by the input signal contributes to $i_{\mathrm{DS},3}(t)$. This is illustrated in Fig. 7.

The generated third harmonic amplitude of $i_{\mathrm{DS}}(t)$ is then given as the third Fourier series coefficient of $i_{\mathrm{DS},3}(t)$, $I_{\mathrm{ds},3}$. For convenience, ωt has been substituted by θ.

$$I_{\mathrm{ds},3} = \frac{1}{2\pi} \sum_{i\in\Omega} K_i \int_{-\varphi_i}^{\varphi_i} (A\cos(\theta) + V_{\mathrm{GS}} - V_i)^2 \cos(3\theta)\, d\theta \tag{13}$$

where Ω represents the set of impulses being traversed. φ_i, being the phase for which the input signal reaches the ith impulse (see Fig. 7), is given by

$$\varphi_i = \arccos\left(\frac{V_i - V_{\mathrm{GS}}}{A}\right) \tag{14}$$

which is valid if $V_{\mathrm{GS}} < V_i$. A similar expression is found for the opposite case so that, when combined with (13), the following solution for $I_{ds,3}$, i.e., HD3, is found:

$$I_{\mathrm{ds},3} = \frac{2}{15\pi} \sum_{i\in\Omega} \frac{K_i (A^2 - (V_i - V_{\mathrm{GS}})^2)^{5/2}}{A^3}. \tag{15}$$

If the signal excursion does not reach a particular impulse, $A^2 - (V_i - V_{\mathrm{GS}})^2$ is negative and the corresponding ith term in (15) becomes purely imaginary. Thus, (15) can be rewritten as

$$I_{\mathrm{ds},3} = \frac{2}{15\pi} \mathrm{Re} \sum_{i=1}^{N} \frac{K_i (A^2 - (V_i - V_{\mathrm{GS}})^2)^{5/2}}{A^3} \tag{16}$$

where the summation is now over all N impulses in G_3.

The piecewise TF presented in Fig. 6 was obtained for a typical RF CMOS PA. Although it was originally determined using numerical simulations, dominant breakpoints may be easily depicted from basic PA and device characteristics. Normally, only a few breakpoints are needed to predict the large-signal IMD behavior well.

Equation (16), in combination with the piecewise TF approximation, thus provides a simple analytical tool for predicting and understanding large-signal HD3 (and thus IM3) behavior of practical PAs.

For small input signals, where the signal excursion will not cross any impulses, zero IMD will be predicted. The presented large-signal analysis is therefore used in combination with the preceding small-signal analysis to understand the overall PA IMD behavior, as described for different classes of operation in the subsections below. For verification purposes, the predictions are compared to numerical one-tone harmonic balance simulations.

C. Class-AB Operation

Most linear PAs are operated in class AB. Therefore, its IMD behavior is studied in detail first. As seen in Fig. 6, G_3 is always negative in class AB and, consequently, small-signal behavior already implies gain compression. Nevertheless, two completely different IMD versus P_{in} patterns may arise.

In the first case, the amplifier is biased slightly above the turn-on voltage. Fig. 8 then shows the resulting HD3 versus input power behavior. Predictions using the presented small- and large-signal analyses are compared to a harmonic balance simulation using the BSIM3v3 model.

For small-signal operation, HD3 (i.e., $I_{\mathrm{ds},3}$) is proportional to $G_3 A^3$, where A is the input signal amplitude [12]. Since G_3 is negative in class AB, HD3 also has a negative sign for small-signal input power levels.

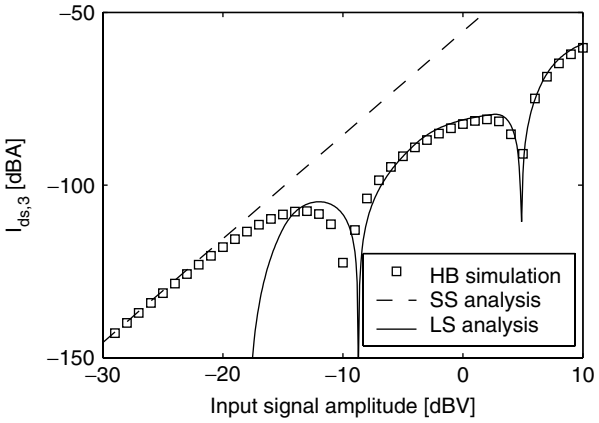


Fig. 8. Third harmonic distortion versus input amplitude A predicted using the presented small-signal (SS) and large-signal (LS) analyses for class-AB operation at $V_{\rm GS} = 0.875$ V. A harmonic balance (HB) simulation is presented as reference.

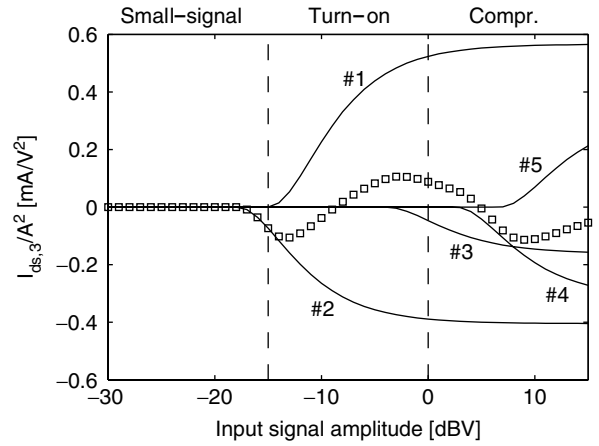


Fig. 9. The simulated compound signed large-signal $I_{\rm ds,3}$ behavior (markers) and its contributions (—) numbered corresponding to the Dirac-delta functions in Fig. 6. $I_{\rm ds,3}$ is normalized with respect to A^2 to improve the plot visibility.

Soon after the first strong nonlinearity is reached—in this case the turn-on knee—the HD3 starts following the behavior predicted by the large-signal analysis instead (see Fig. 8). The agreement between the large-signal analysis and harmonic balance simulation is seen to be good even with the small number of impulses used in Fig. 6.

To fully understand the class-AB large-signal HD3 behavior in Fig. 6, it is noted that, according to (16), the total large-signal IMD is a sum of contributions from different regions in the PA TF, corresponding to the breakpoints in Fig. 6. The compound signed large-signal HD3 behavior and its contributions are shown versus input power in Fig. 9.

From Fig. 9, after the initial negative small-signal HD3, the turn-on knee (contribution #1) is seen to invert the sign of HD3, which then becomes positive. This change of sign corresponds to the lower large-signal IMD minimum (sweet spot) present in Fig. 8.

However, IMD cannot remain positive as, for sufficiently large input power, the output power must compress. This is manifested in Fig. 9 by the negative IMD contributions #3 and #4, corresponding to the output current quadratic-to-linear and

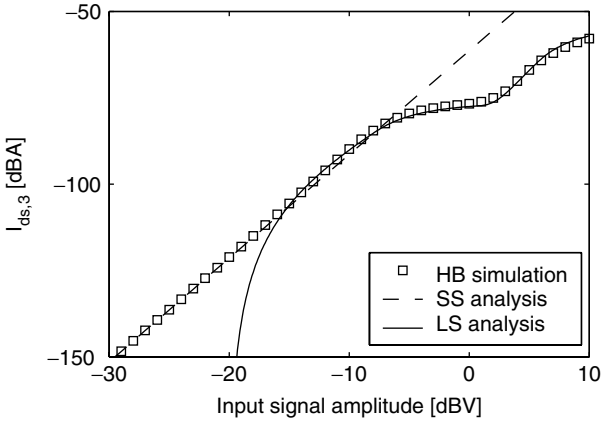


Fig. 10. HD3 (i.e., $I_{\rm ds,3}$) versus input signal amplitude A for class-AB operation at $V_{\rm GS} = 1.1$ V.

compression transitions, respectively. This results in a second change of sign in HD3, and in another sweet spot close to the output power compression point in Fig. 8. Similar behavior with two sweet spots has also been identified in LDMOS transistors [15].

Note the possibility of adjusting the relative position of the two sweet spots by carefully selecting the bias point, since, for higher gate bias, a larger input power is required for the signal excursion to reach the turn-on knee. Combined with associated high power-added efficiency (PAE) values, this turns class-AB CMOS PAs into serious candidates for applications where simultaneous efficiency and linearity is of prime concern.

In the second case, the PA is biased with higher $V_{\rm GS}$, more toward class-A operation. Still, the small-signal HD3 is negative. In this case, however, the turn-on knee contribution (#1 in Fig. 9) is smaller compared to the previous case, as the corresponding term $A^2 - (V_1 - V_{\rm GS})^2$ in (16) is now reduced. HD3, therefore, never changes sign but remains negative. Nevertheless, the turn-on knee still has its beneficial effect, decreasing the HD3 magnitude as shown in Fig. 10.

D. Class-C Operation

In the lower extreme of possible $V_{\rm GS}$ biases, the PA operates in class C. In this case, Figs. 3 and 5 indicate that small-signal IMD corresponds to a positive G_3 (and g_{m3}), which also determines gain expansion.

In terms of the presented large-signal IMD analysis, the strong positive turn-on knee region contribution (#1) will be the first one reached and, therefore, reinforce the already positive small-signal G_3 contribution. However, at sufficiently high input power levels, the negative HD3 contributions will always dominate and force the HD3 sign to become negative. Thus, HD3 will change sign and a large-signal IMD sweet spot occurs close to compression, which is similar to those already reported for MESFETs [12] and LDMOSFETs [15]. This may be an interesting benefit of this PA operation class, especially for low-frequency applications where its recognized deficiencies in terms of PAE and power gain are less penalizing. Fig. 11 shows the typical HD3 versus input power obtained in class-C operation. The large-signal analysis is seen to predict the IMD behavior very well also in this case.

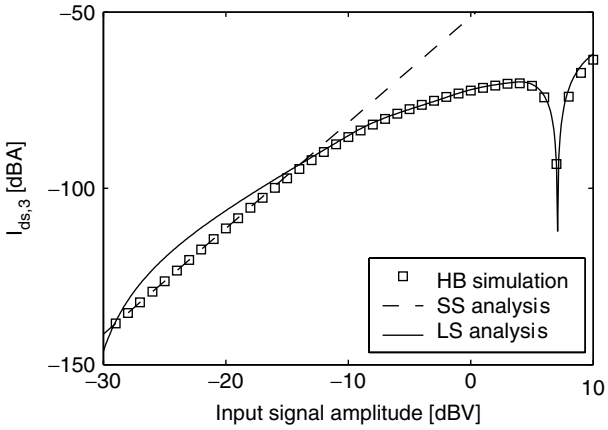


Fig. 11. HD3 versus input signal amplitude A for class-C operation at $V_{\rm GS} = 0.675$ V.

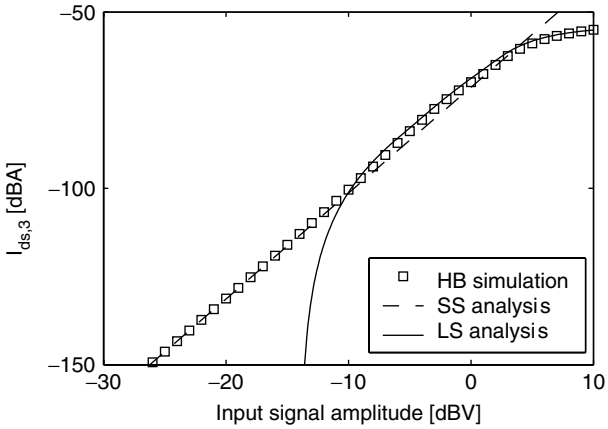


Fig. 12. HD3 versus input signal amplitude A for class-A operation at $V_{\rm GS} = 2.0$ V.

E. Class-A Operation

The upper extreme of gate bias voltages corresponds to class-A operation. In this situation, small-signal IMD is still negative, although very small, as seen from G_3. However, the positive HD3 contributions from the turn-on knee and saturation regions (#1 and #5 in Fig. 6) are now even further away from the bias voltage and, therefore, have a small influence on the HD3 behavior. They can, therefore, only manifest at very high input power levels. Since they cannot alter the IMD sign, no sweet spots will be present in class A. On the contrary, and since their small-signal distortion is always negative, class-A PAs tend to present a degradation of HD3 when large-signal regime is reached. This is also confirmed in Fig. 12, which shows the IMD versus input power behavior in class-A operation.

Class A is recognized for its low PAE and is, therefore, only used for highly linear PA designs kept comfortably in small-signal regimes.

V. PA Measurements

A. RF-CMOS PA Prototype

To study the IMD behavior in a real circuit application, a broadband CMOS PA [16] was built using a 1200-μm device of the same technology as the smaller 60-μm device used in previous sections for model evaluation. The PA schematic is shown in Fig. 13.

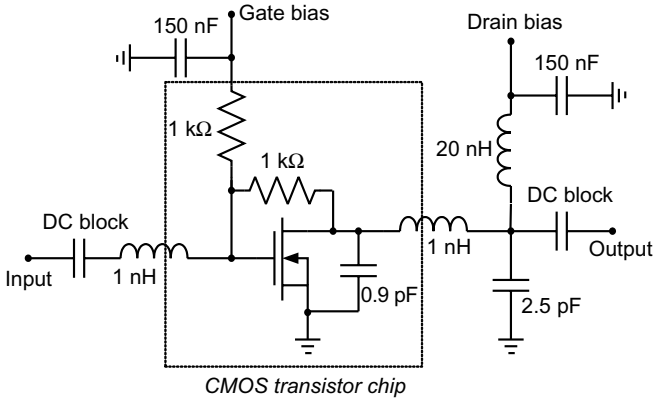


Fig. 13. RF CMOS power amplifier circuit schematic.

B. Two-Tone Measurements

Two-tone measurements were performed on the amplifier at 950 MHz, with 1-MHz frequency separation. The drain bias was held constant at 3 V during the measurements, whereas the gate bias was varied for testing different classes of operation. The power levels in the plots of Fig. 14 are given per tone.

From the small-signal IMD analysis, it is known that the IM3/$P_{\rm in}$ should follow a 3-dB/dB slope at low input power. This is actually the assumption underlying extrapolated IP3 calculation. The measured slope is, therefore, indicated in each of the figures.

Harmonic balance simulations of output power and IM3 using the BSIM3v3 model are also presented in Fig. 14 and shown to give good agreement with the measurements for all classes of operation. This indicates that, not only BSIM3v3 provides a good description of the MOSFET nonlinear details, as seen when the $i_{\rm DS}(v_{\rm GS})$ derivatives were addressed, as it also accurately represents the device's strong nonlinearities.

1) Class C: Fig. 14(a) shows the measured output power and IM3 versus input power for $V_{\rm GS} = 0.675$ V, corresponding to class-C operation. As predicted from the behavioral analysis in the preceding section, a large-signal sweet spot appears in the measurements close to the compression point. Locally, this large-signal IMD sweet spot creates a large carrier-to-intermodulation ratio (C/I). Unfortunately, the overall IMD performance of class C may not be very good if operated over a wide input power range.

The measured low-power IM3 slope is 2.4 dB/dB. This indicates that the small-signal analysis is not suitable for predicting IMD in class C, even at these very low input power levels. Accordingly, it also indicates that an attempt to force IMD characterization by any small-signal figure of merit like IP3, will lead to erroneous results in which this figure of merit would be seen to depend on the actual test power.

2) Class AB: In class-AB operation, G_3 is negative. As described in the previous section, this makes it possible to have two large-signal IM3 sweet spots for different input power levels. Since the first one takes place when the input signal excursion

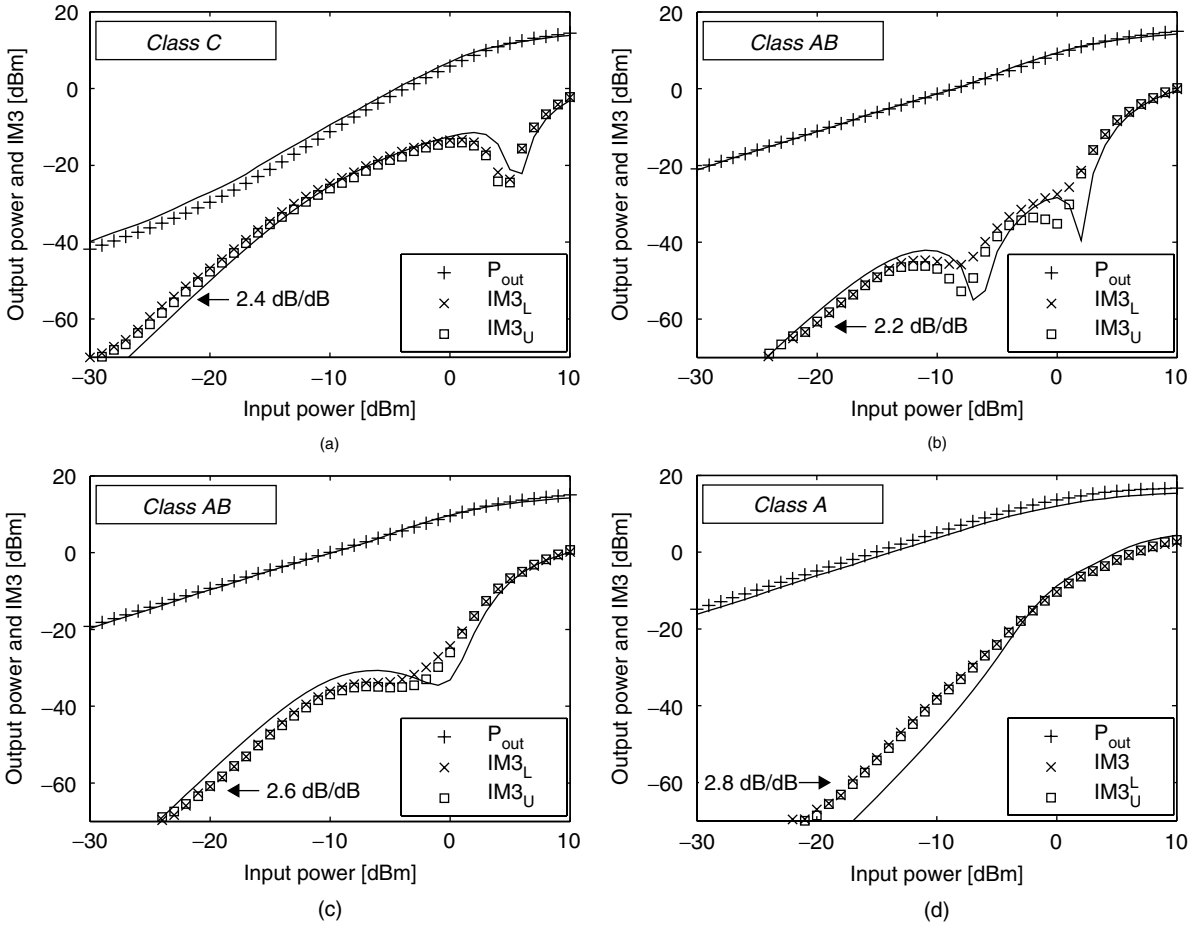


Fig. 14. Two-tone measurements (markers) and HB simulations (—) of output power $P_{\rm out}$ and lower/upper IM3 sideband power levels $\mathrm{IM3_L}/\mathrm{IM3_U}$ for: (a) $V_{\rm GS} = 0.675$ V; (b) $V_{\rm GS} = 0.875$ V; (c) $V_{\rm GS} = 0.925$ V; (d) $V_{\rm GS} = 2.0$ V. The measured low-power IM3 slope is also indicated.

reaches the turn-on knee, it will occur at higher input power for higher gate bias, becoming, thus, bias dependent. The second large-signal sweet spot then appears close to the compression point. This is confirmed in Fig. 14(b) where class-AB measurements at $V_{\rm GS} = 0.875$ V are shown. This also corresponds to the first case presented in the preceding IMD analysis for class-AB operation.

The second IMD behavior case is reflected in the measurements made at $V_{\rm GS} = 0.925$ V and shown in Fig. 14(c). In that case, the positive knee contribution arising from turn-on is, in fact, not large enough to make IM3 change sign before $v_{\rm DS}(t)$ swing reaches linear region, and thus no two sweet spots are observed but rather a decrease in IM3.

It is interesting to note that, especially in Fig. 14(b), the IM3 slope observed for the lowest input driving levels is already 2 dB/dB rather than the 3 dB/dB that should be expected from a pure small-signal IMD analysis. Thus, even for these very low input powers, the small-signal analysis is obviously no longer suitable. A slope of 2 dB/dB is actually predicted by the large-signal IMD analysis if only one contribution is considered, e.g., the turn-on knee.

3) Class A: Finally, measurements made in class A are shown in Fig. 14(d). Class A gives the highest gain, and is usually considered the most linear mode of operation. However, due to the possibility of having double IMD minima, class AB may in fact be more linear over a wide input power range. Considering also its higher efficiency, class AB is the most attractive mode of operation for linear power amplifiers.

4) Memory Effects: IMD asymmetry was observed in the two-tone measurements. This is a symptom of low-frequency (signal envelope) memory effects which can, in general, be related to the active device thermal dynamics, reactive load impedance at the two-tone difference frequency, or nonlinear capacitances [17], [18]. In this PA circuit, the 150-nF bypass capacitors on the bias lines (see Fig. 13) partially helped in reducing the asymmetries, which constituted a clear indication of their source.

IMD asymmetries are one of the possible effects induced by envelope dynamics that affect the PA behavior to wideband-modulated signals. When these envelope memory effects are added to our memoryless nonlinearity model, they tend to smoothen the studied IMD minima or even eliminate them [19]. Careful design of the PA bias networks and good thermal mounting of the active device are therefore crucial.

The PA can also manifest memory effects induced by its bandpass characteristics and so presenting time constants comparable to the carrier period. Fortunately, in wireless PAs where typically the signal bandwidth is only a very small fraction of the available PA RF bandwidth, its impact on IMD can be usually neglected.

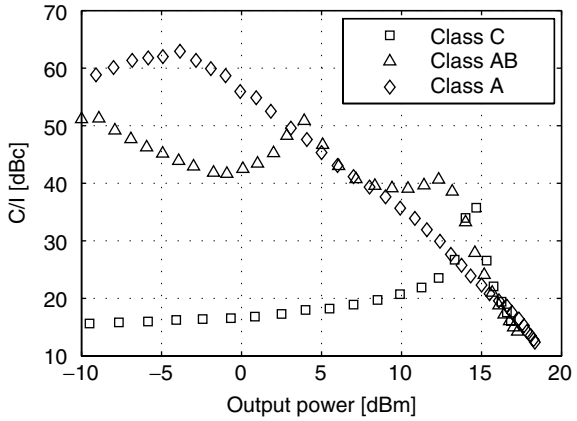


Fig. 15. Measured carrier-to-intermodulation ratio (C/I) versus output power for different classes of operation.

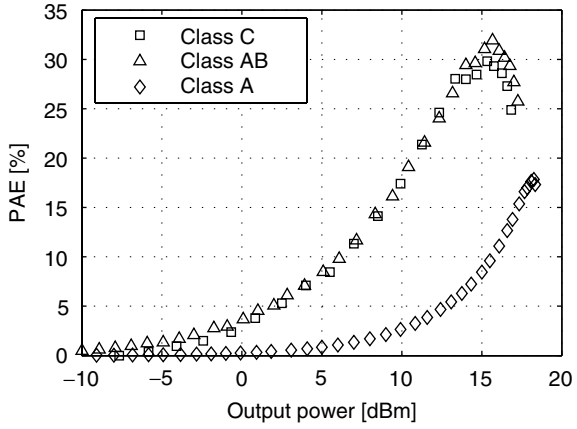


Fig. 16. Measured PAE versus output power for different classes of operation.

5) Efficiency and Linearity Comparison: The different classes of operation are compared in terms of C/I and PAE in Figs. 15 and 16, respectively. As an example, for a specified C/I of 35 dBc, class AB is in fact seen to give 3.5 dB higher output power than class A. Furthermore, in class AB, the maximum PAE under the linearity requirement is 25%, whereas for class A it is below 5%.

The poor linearity of class C, associated to its recognized low gain, makes it impossible to benefit from the good theoretical drain efficiency in practical applications where optimized linearity and PAE are needed.

C. Wideband IMD Measurements

In realistic applications, power amplifiers are operated with wideband input signals, not with the standardized two-tone excitation that cannot carry information. Therefore, to test the suitability of two-tone tests for predicting IMD behavior in such real situations, the amplifier IMD characteristics have been evaluated using a 1.2 MHz channel bandwidth CDMA signal excitation at 950 MHz. The signal was generated using an Agilent E4438C ESG generator with a chip rate of 1 Mchip/s and the input power level swept. Fig. 17 shows the output spectrum for class-AB operation at -30 and -15 dBm input power. The measured adjacent channel power ratio (ACPR) versus output power for class C, AB, and A operation is shown in Fig. 18.

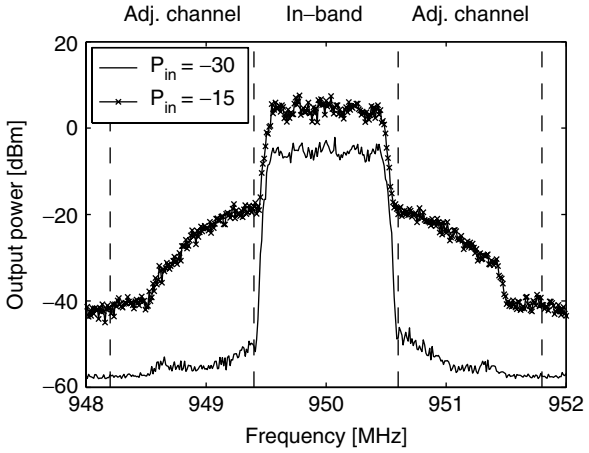


Fig. 17. Output spectrum for -30 and -15 dBm input power with a 1.2-MHz-wide CDMA input signal.

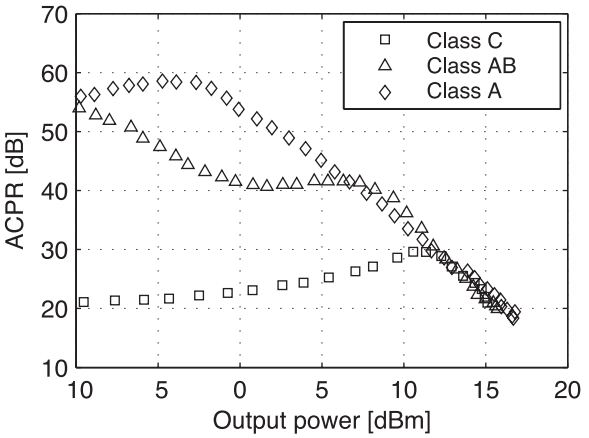


Fig. 18. Measured adjacent channel power ratio versus input power $P_{\rm in}$.

Even if the statistical properties of the input signal in this case are completely different compared to the two-tone excitation, the multitone measurements presented in Fig. 18 are similar to the two-tone measurements previously presented in this section (Fig. 15). Thus, the analysis, which was used to explain the measured two-tone IMD behavior, is applicable also under realistic input signal conditions.

VI. Conclusion

In this paper, a thorough analysis for the IMD behavior of RF MOSFET power amplifiers has been presented. The traditional small-signal analysis of MOSFET amplifiers used to understand PA IMD becomes inaccurate when the input signal excursion reaches the turn-on knee. A simple analysis method was, therefore, presented which allowed the large-signal IMD behavior to be predicted and dominating device and PA mechanisms to be identified. In particular, it was found that the large positive contribution from the turn-on knee region was important for understanding the overall IMD behavior in class-AB operation, in which most linear power amplifiers are operated. In combination with the compressing nonlinearity of the saturation-to-linear region transition, this resulted in an overall very linear operation and high efficiency.

The analysis has been used to explain both two-tone and more realistic wideband CDMA measurements in a 950 MHz power amplifier circuit. The ability of an industry-standard BSIM3v3 model in predicting IMD has also been evaluated.

ACKNOWLEDGMENT

The authors would like to thank Dr. K. Yhland and Dr. N. Rorsman at the Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden, for helpful comments on the manuscript.

REFERENCES

[1] M. Steyaert, P. Coppejans, W. De Cock, P. Leroux, and P. Vancorenland, "A fully-integrated GPS receiver front-end with 40 mW power consumption," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 1, 2002, pp. 396–397.

[2] S. Mahdavi and A. A. Abidi, "Fully integrated 2.2-mW CMOS front-end for a 900-MHz wireless receiver," *IEEE J. Solid-State Circuits*, vol. 37, pp. 662–669, May 2002.

[3] J. A. Weldon *et al.*, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, pp. 2003–2015, Dec. 2001.

[4] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Norwell, MA: Kluwer, 1998.

[5] M. T. Terrovitis and R. G. Meyer, "Intermodulation distortion in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1461–1473, Oct. 2000.

[6] W. Yu, S. Sen, and B. H. Leung, "Distortion analysis of MOS track-and-hold sampling mixers using time-varying Volterra series," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 101–113, Feb. 1999.

[7] C.-H. Feng, F. Jonsson, M. Ismail, and H. Olsson, "Analysis of nonlinearities in RF CMOS amplifiers," in *Proc. 6th IEEE Int. Conf. Electronics, Circuits and Systems*, vol. 1, 1999, pp. 137–140.

[8] S. Kang, B. Choi, and B. Kim, "Linearity analysis of CMOS for RF application," in *Proc. IEEE Int. Microwave Symp.*, 2002, pp. 279–282.

[9] W. Liu *et al.*, "BSIM3v3.2.2 MOSFET Model: Users' Manual," Univ. California, Berkeley, 1999.

[10] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[11] S. A. Maas, *Nonlinear Microwave Circuits*. Norwood, MA: Artech House, 1988.

[12] N. B. Carvalho and J. C. Pedro, "Large- and small-signal IMD behavior of microwave power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 2364–2374, Dec. 1999.

[13] J. C. Pedro and J. Perez, "Accurate simulation of GaAs-MESFETs intermodulation distortion using a new drain-source current model," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 25–33, Jan. 1994.

[14] L. Råde and B. Westergren, *Beta: Mathematics Handbook*. Bromley, U.K.: Chartwell-Bratt, 1990.

[15] C. Fager, J. C. Pedro, N. B. Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 2834–2842, Dec. 2002.

[16] F. Fortes and M. J. Rosário, "A second harmonic class-F power amplifier in standard CMOS technology," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1216–1220, June 2001.

[17] N. B. Carvalho and J. C. Pedro, "A comprehensive explanation of distortion sideband asymmetries," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 2090–2101, Sept. 2002.

[18] J. Voulevi and T. Rahkonen, *Distortion in RF Power Amplifiers*. Norwood, MA: Artech House, 2003.

[19] J. C. Pedro and N. B. Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits*. Norwood, MA: Artech House, 2003.

Christian Fager (S'02–M'03) was born in Varberg, Sweden, in 1974. He received the M.Sc. and Ph.D. degrees in electrical engineering and microwave electronics from Chalmers University of Technology, Göteborg, Sweden, in 1998 and 2003, respectively.

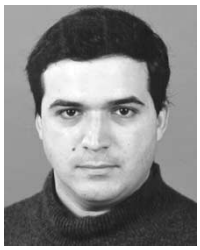
Currently, he is a Senior Research Scientist with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology. His research interests are in the areas of large-signal transistor modeling and nonlinear circuit design.

Dr. Fager received the Best Student Paper Award from the IEEE International Microwave Symposium in 2002.

José Carlos Pedro (S'90–M'95–SM'99) was born in Espinho, Portugal, on March 7, 1962. He received the Diploma and Ph.D. degrees in electronics and telecommunications engineering from the University of Aveiro, Portugal, in 1985 and 1993, respectively.

From 1985 to 1993, he was an Assistant Lecturer at the University of Aveiro, where he is currently an Associate Professor at the same University, and a Senior Research Scientist at the Telecommunications Institute. His main scientific interests include active device modeling and the analysis and design of various nonlinear microwave and optoelectronics circuits, in particular, the design of highly linear multicarrier power amplifiers and mixers. He has authored or coauthored several papers in international journals and symposia, and served as a reviewer for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the IEEE MTT-S International Microwave Symposium.

Dr. Pedro received the Marconi Young Scientist Award in 1993 and the 2000 Institution of Electrical Engineers (IEE), U.K., Measurement Prize.



Nuno Borges de Carvalho (S'92–M'00) was born in Luanda, Portugal, in 1972. He received the Diploma and Ph.D. degrees in electronics and telecommunications engineering from the University of Aveiro, Aveiro, Portugal, in 1995 and 2000, respectively.

From 1997 to 2000, he was an Assistant Lecturer at the same University. Currently, he is an Auxiliary Professor at the University and a Senior Research Scientist at the Telecommunications Institute. His main research interests include CAD and measurement of nonlinear circuits and design of RF-microwave power amplifiers. He has authored or coauthored several papers in international journals and symposia and has been a reviewer for several journals and symposia.

Dr. Carvalho is a member of the editorial board of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He was the recipient of the 1995 University of Aveiro and the Portuguese Engineering Association Prize for the best 1995 student at the University of Aveiro, the 1998 Student Paper Competition (third place) presented at the IEEE International Microwave Symposium and the 2000 Institution of Electrical Engineers (IEE), U.K., Measurement Prize. He is a member of the Portuguese Engineering Association.

Herbert Zirath (S'84–M'86) is currently Head of the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden, where he became a Professor in 1996. His main scientific interest is high-frequency electronics, in particular, design and fabrication of InP-HEMT devices and circuits, SiC-MESFETs and diodes and GaN-HEMTs and related circuits, device modeling, including noise and large-signal models for FET and bipolar devices, and foundry-related MMICs for microwave and millimeter-wave applications. He is also one of the founders of Norse AB, a company specializing in SiC high-frequency components.

Fernando Fortes was born in Setúbal, Portugal, in 1970. He graduated in electrical and computer engineering in 1995 and received the Ph.D. degree from the Instituto Superior Técnico (Technical University of Lisbon), Lisbon, Portugal, in 2001.

Since 1995, he has been engaged in research on microwave circuits at the Telecommunications Institute, University of Aveiro, Aveiro, Portugal. Since 1998, he has been a Member of the teaching staff at the Instituto Superior de Engenharia de Lisboa. His research interests are in the area of active device modeling in silicon and the design of microwave circuits for wireless applications.

Maria João Rosário (S'90–M'93) was born in Olhão, Portugal. She received the Licenciatura, M.S., and the Ph.D. degrees in electrical and computer engineering from the Instituto Superior Técnico (Technical University of Lisbon), Lisbon, Portugal, in 1978, 1986, and 1992, respectively.

Since 1985, she has been a Member of the teaching and research staff at the Instituto Superior Técnico, where she is currently Assistant Professor. Her research interests are in the area of field-effect transistors modeling and the design of microwave mixers and filters.