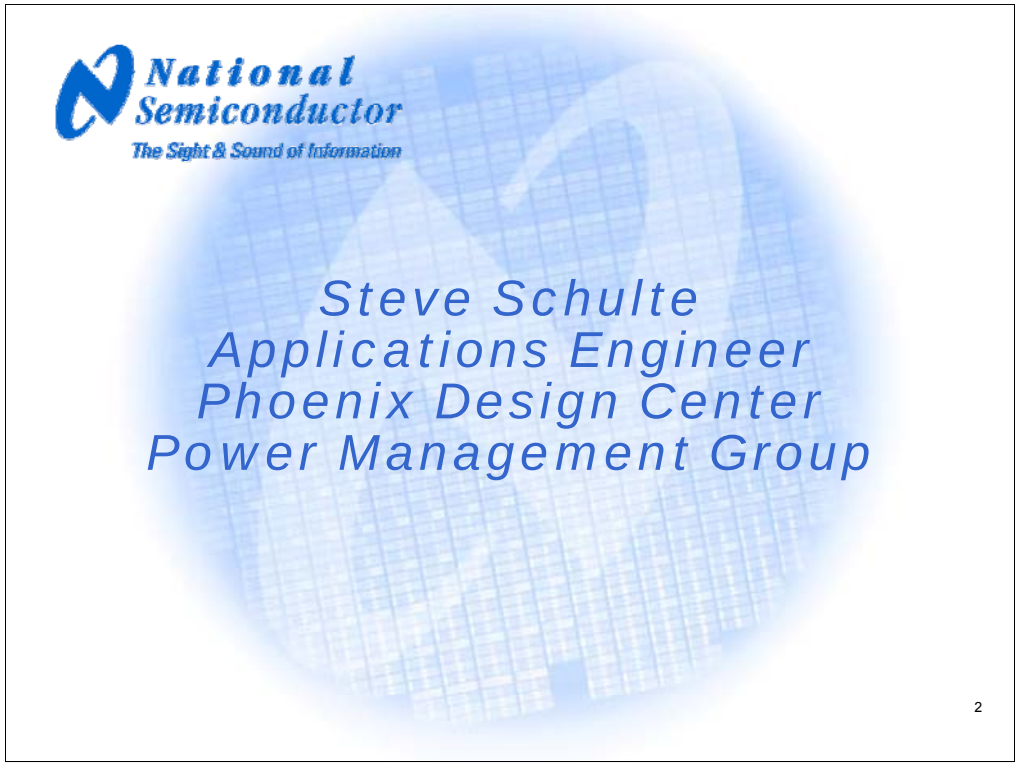
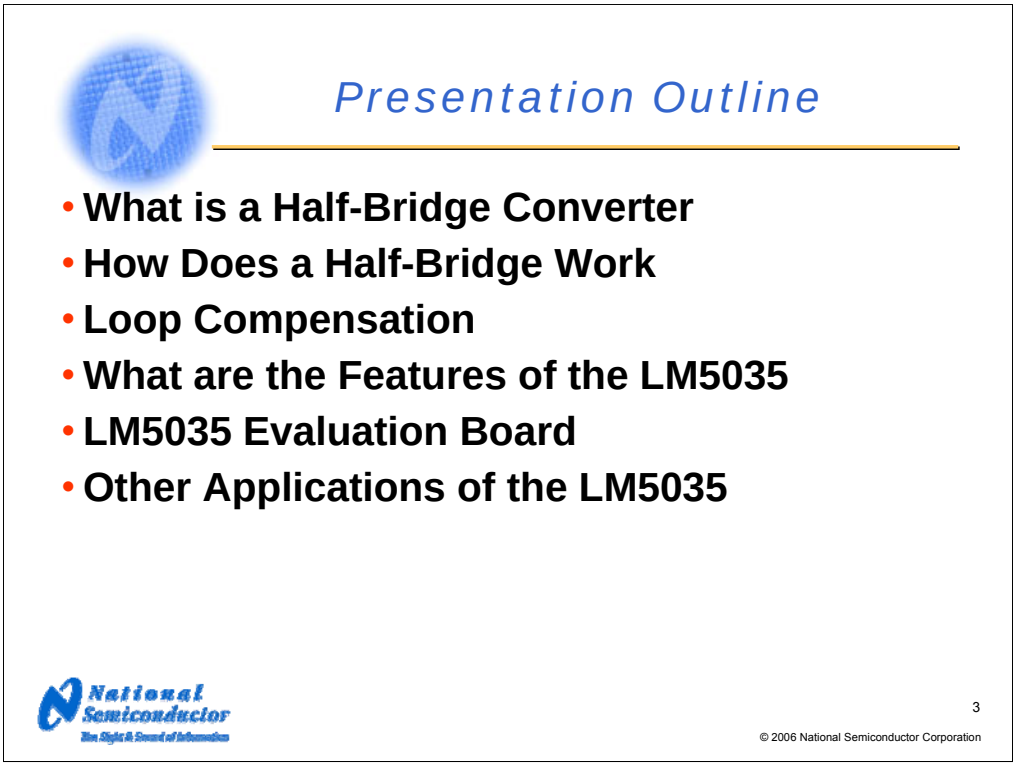
Hello! Welcome to National Semiconductor's continuing series of On-Line Seminars

The topic of this presentation is the design of Half-Bridge Power Converters.



My name is Steve Schulte and I'm an applications engineer for the High Voltage product line in the Power Management group.



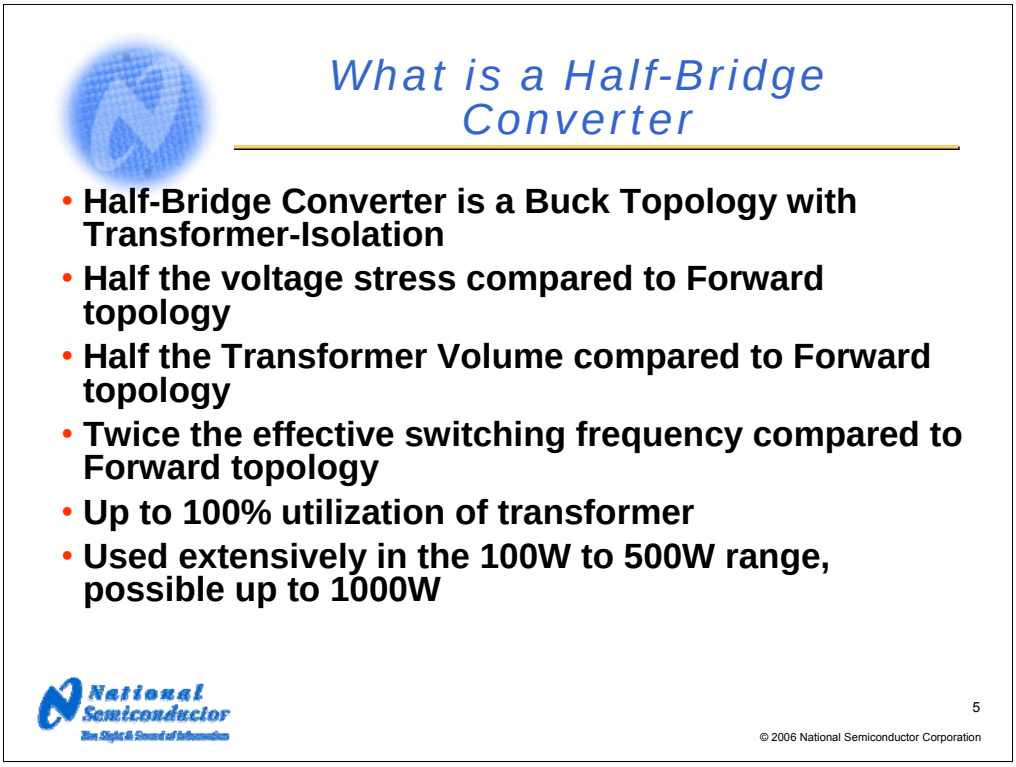
The first section of this seminar will describe the Half-Bridge topology and contrast it with other topologies.

Next we'll delve into the power flow through the transformer, the heart of the converter.

Then loop compensation analysis and design process for a Type 3 compensator is presented.

Following this, the features of the LM5035 Half-Bridge Controller and Driver are reviewed, along with the reference design and a couple alternate uses for the LM5035.

First, what is a Half-Bridge converter?



The Half-Bridge topology is derived from the Buck converter family, which also includes the Forward topology and the Full-Bridge topology. This family transfers power from the primary to the secondary during the 'on' time, rather than storing energy in the transformer as in the Flyback topology.

The Half-Bridge returns the core magnetizing energy to the input capacitors through the MOSFETs, so a reset method required for Forwards is not necessary. The Forward typically causes the MOSFET drain voltage to double the VIN during reset.

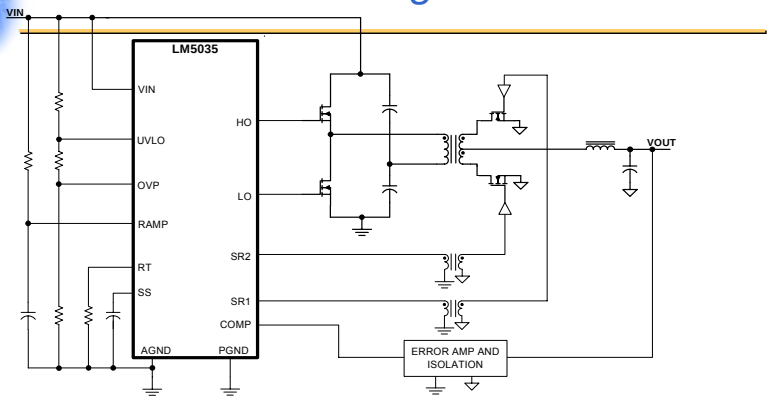
Forward uses the transformer in one direction, while Half-Bridge uses the core's entire B-H loop. This makes better use of the Half-Bridge core so the transformer can be smaller for the same power level.

During the switching cycle the Forward drives one power pulse and Half-Bridge drives two. The output filter components can be smaller for Half-Bridge due to this.

Forward needs at least 30% of the switching cycle for core reset, Half-Bridge can use up to all the switching cycle.

Full-Bridge applies twice the voltage to the transformer compared to Half-Bridge, so the current levels are more manageable at power levels greater that 1KW.

Basic Half-Bridge Converter



Advantages: Up to 100% effective Duty Cycle (high power density)
Low voltage stress on Primary Switches (allows lower $R_{DS(ON)}$ MOSFETs)
Smaller Transformer required due to 2 quadrant core swing

Disadvantages: Only Half of VIN applied to Primary
Voltage Mode only
Type 3 Compensation Required

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To summarize, the Half-Bridge offers many advantages compared to Forward in the 100W to 500W range. These include lower voltage MOSFETs, smaller transformer and output filter, and lower output ripple. The Half-Bridge does require 2 primary MOSFETs though, and 2 drivers.

Half-Bridge is usually designed with Voltage Mode Control, since current mode tends to unbalance the capacitor divider. Voltage Mode Control necessitates Type 3 compensation, which is more complex than Current Mode compensation.

Primary currents in a Half-Bridge are twice that of Full-Bridge at the same power level, though Full-bridge requires twice again the primary side component count.

Now for the details of power flow in a Half-Bridge converter.

Half-Bridge Converter Equation

$$VOUT = n \bullet \tfrac{1}{2} VIN \bullet D$$

- **'n' is the Primary-to-Secondary turns ratio, 1 : n**
- **D is the HO 'on' time plus the LO 'on' time divided by the total switching period**

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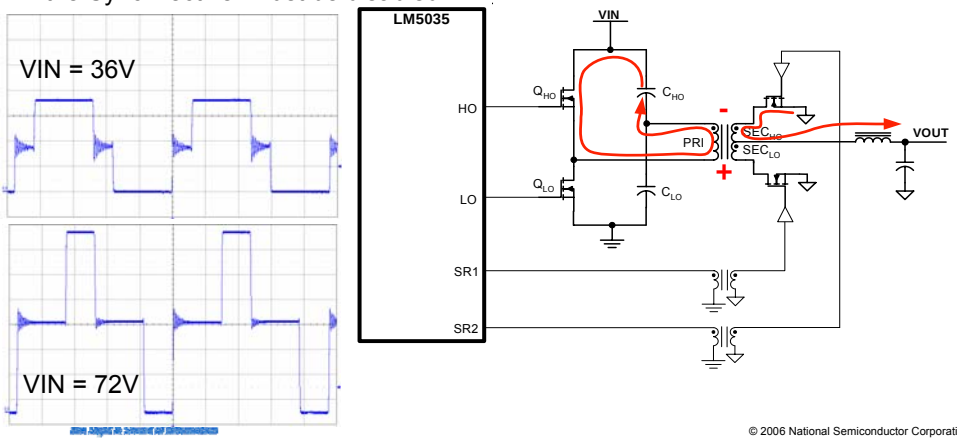
As with any Buck family converter, the basic equation is the output voltage equals the input voltage times the duty cycle. The duty cycle in this case is taken as the high-side switch 'on' time plus the low-side switch 'on' time divided by the entire period of a high-side and low-side cycle. The Half-Bridge modification of the Buck equation is that only half of the input voltage is applied to the transformer and the transformer turns ratio 'n' also scales the equation.

Half-Bridge Transformer Power Pulses

A Half-Bridge Transformer alternates positive and negative power pulses through the primary into alternate secondary windings. When the HO FET is enabled, C_{HO} is discharged through the primary, into SEC_{HO} and the output inductor, while C_{LO} is charged. During this time, SEC_{LO} is driven to twice the SEC_{HO} voltage, so the Sync Rectifier must be disabled.



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The transformer primary is a single winding while the secondary has 2 symmetric windings. During a high-side switching cycle, one of the secondary windings is energized and provides power to the output inductor while the other winding is ‘off’. The ‘off’ winding has twice the voltage, so if it weren’t disconnected from ground the secondary would be shorted and obviously bad things would happen. The SR controls insure that these bad thing don’t happen.

During a low-side switching cycle the secondary windings swap roles, so one secondary winding is always paired with a specific primary MOSFET.

The arrows on the schematic indicate the direction of power flow during a high-side switching cycle. The + and – symbols show the voltage applied to the primary and developed in the secondary.

The scope traces at the left show the voltage applied to the primary by the FETs with low input voltage and high input voltage. Note the product of voltage and ‘on’ time are the same in both cases.

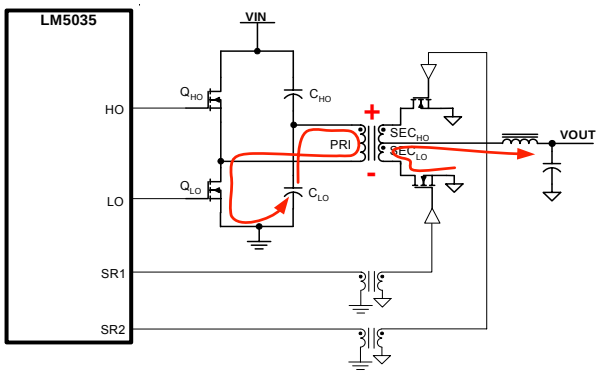
Half-Bridge Transformer Power Pulses

•When the LO FET is enabled, C_{LO} is discharged through the primary in the opposite direction, into SEC_{LO} and the output inductor, while C_{HO} is charged.
•The capacitor divider centerpoint Ripple voltage is determined by "q = C • V". For instance, if VIN = 48V, Pout = 100W, efficiency = 90%, D = 50% and the switching frequency is 400KHz, for C_{HO} = C_{LO} = 2 x 6.8µF the ripple voltage is:

$$I\_divider\_center = \frac{\frac{100W}{90\%}}{50\% \bullet \frac{48V}{2}} = 9.26A$$

$$q = \frac{I\_divider\_center}{400KHz} = 23.2\mu C$$

$$V\_ripple = \frac{q}{2 \times 6.8uF} = 1.7Vp-p$$



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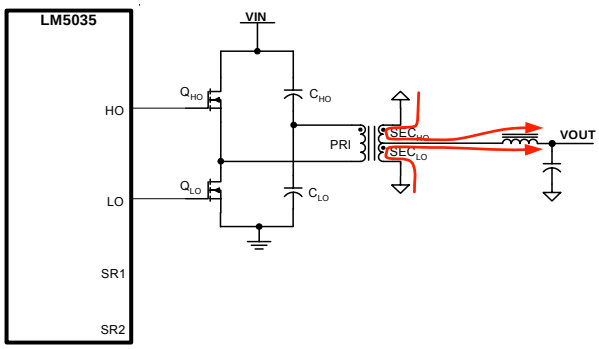
During a low-side switching cycle, the voltage polarity is flipped and the other secondary winding is energized. There is a small ripple voltage at the capacitor divider center point. This can be simply calculated by the amount of charge required to maintain the output load power and the values of the capacitor divider components. The ripple voltage is not significant unless high ESR capacitors are used, which then may cause unwanted heating. Low ESR ceramic capacitors are recommended. Since ceramic's capacitance falls with increased voltage, analysis should take this into account.

Half-Bridge Transformer "Off" Time

Between power pulses, the HO FET and LO FET are disabled while the Sync Rectifiers are enabled. Since the ***secondaries are shorted*** together with opposite polarity, the secondary has no inductance and ***appears as a short to ground***. This provides the current path for the output inductor as it continues to deliver power to the output cap and load.

Each secondary carries approximately ***half the load*** current.



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When neither the hide-side or low-side switches are 'on' the SR controls turn 'on' both secondary synchronous rectifiers which effectively connects the windings together, but in opposition so that their inductances cancel and appear to the output inductor as just a ground connection.

This allows the inductor to continue supplying it's stored energy to the output capacitors and the load. Each secondary winding carries about half the inductor current during this time.

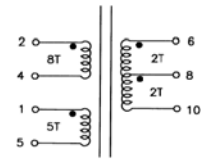
Half-Bridge Transformer Operation

The Half-Bridge Transformer (Coilcraft) used on the LM5035 Eval Board has an 8 turn primary with 120µH magnetizing inductance. The leakage inductance is low (< 250nH) due to planar construction. There are 2 secondaries with 2 turns each.

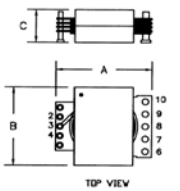
MECHANICAL SPECIFICATIONS

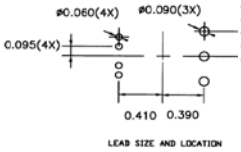
PHYSICAL PARAMETERS (INCHES)		
DIMENSIONS	MIN	MAX
A: WIDTH		.920
B: LENGTH		.810
C: HEIGHT		.360
D: COPLANARITY WITHIN .006		

CHECK DIMENSION D: 100%



SCHEMATIC





LEAD SIZE AND LOCATION

ELECTRICAL SPECIFICATIONS

INDUCTANCE(uH) 100% 200.0kHz, 1 VRMS, 0 ADC		
PINS	MIN	MAX
2–4	120.0	

HI POT 100% (VDC, to be applied for 1 second)		
VOLTAGE:	FROM PINS	TO PINS
1500	1,2	6

VOLTAGE RATIO 100% Apply 100mVrms, 10 kHz to pins 2–4		
MEASURE PINS:	MIN	MAX
6–10	.490	.510
1–5	.613	.638

DC RESISTANCE (mOHMS) A/R		
PINS	MIN	MAX
2–4		50.00
1–5		250.00
6–10		2.00

LEAKAGE INDUCTANCE (uH) 100% 200 kHz, 1 Vrms,		
TEST PINS	SHORT PINS	MAX
2–4	6,8,10	.25

The 5 turn AUX winding is peak detected and provides the 10 – 20mA gate drive current to the LM5035.

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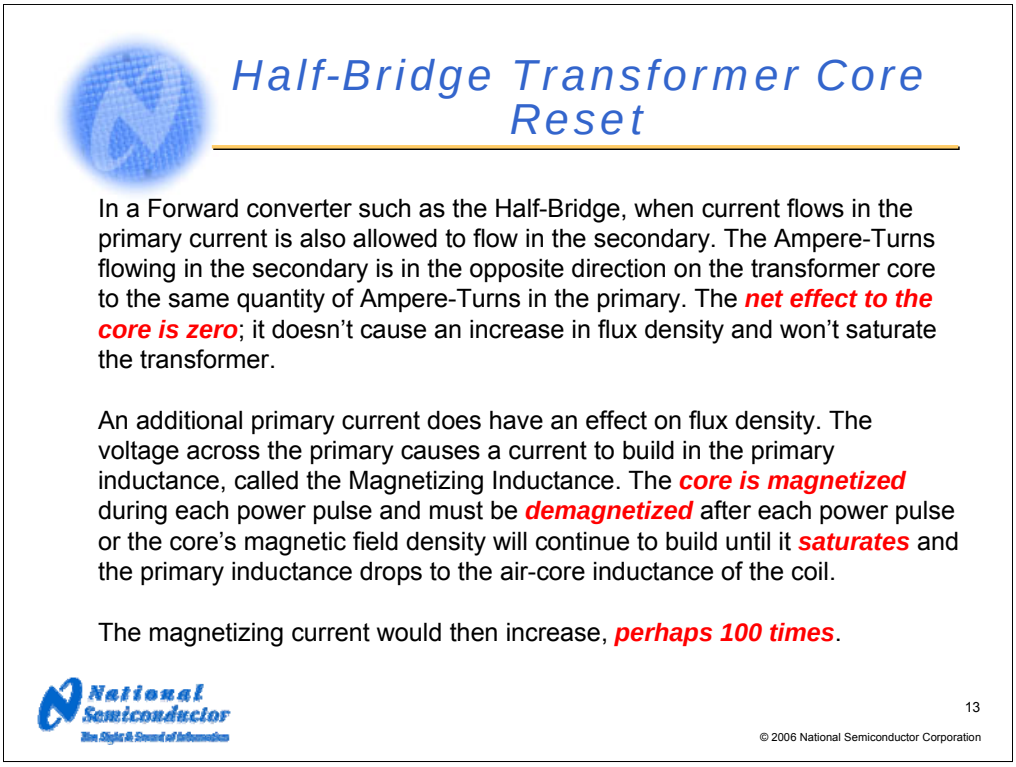
The Coilcraft transformer used on the reference design is a surface mount planar type with stamped sheet copper turns for low DCR losses. The primary to secondary one to secondary two turns ratio is 8:2:2. An additional low current 5 turn winding provided low voltage power to the LM5035, mostly for the power MOSFET gate charge.

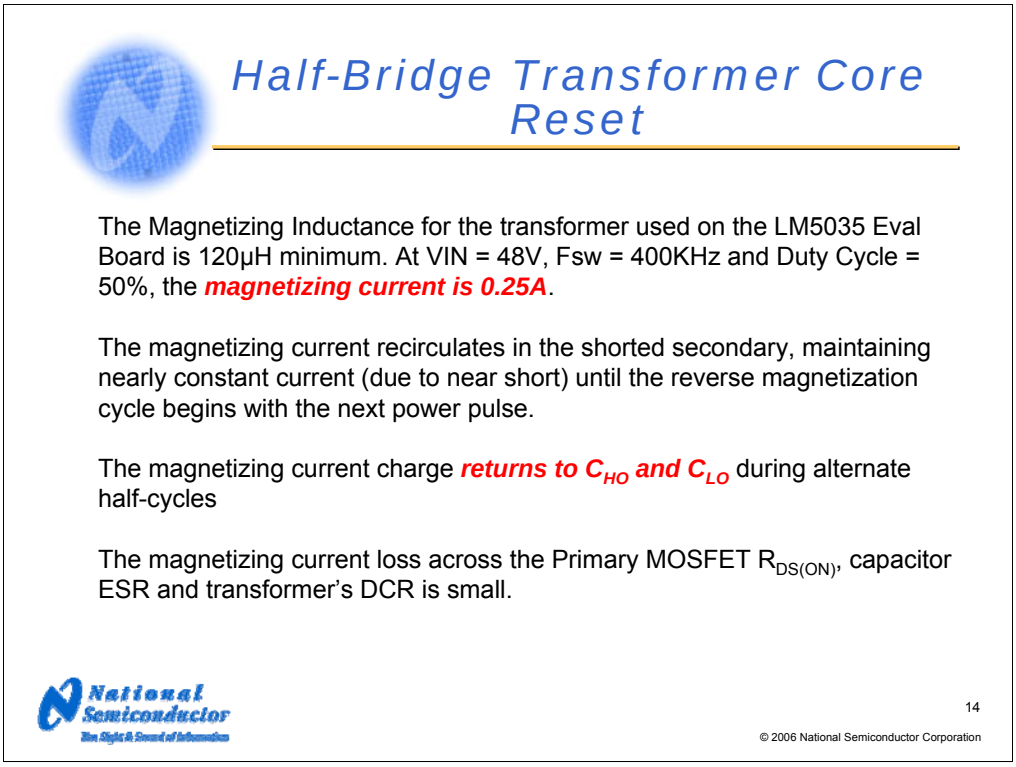
The primary magnetizing inductance is shown as 120 micro henries, which will be discussed in the next slide.

A benefit of planar construction is low leakage inductance, which is specced at less than 250 nano henries of the datasheet.



All types of Forward converter transformers (including the Half-Bridge) create a magnetic field with the primary winding and the current induced into the secondary winding creates a magnetic field of opposite polarity so that the net effect on the transformer core is zero.

The core is effected by what is called the magnetizing inductance. I tcan be thought of as the inductance that is measured across the primary when nothing is connected to the secondary. Since no power is transferred in this case, it's easy to see how this acts exactly like any other inductor. While either primary MOSFET is 'on' it stores energy in the core that must be removed, or the core will quickly saturate. When a core saturates, it's as if the core was physically removed from the transformer, so the value of the inductor drops maybe 100 times. Then the switching pulses cause primary current inversely proportional to the inductance drop, and huge currents burn the MOSFETs!



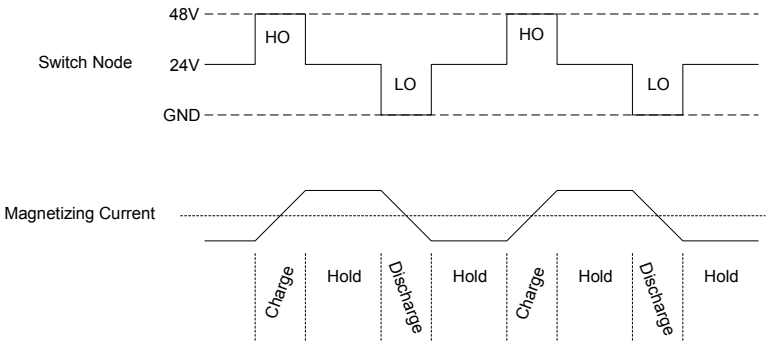
An advantage that Half-Bridge has over the Forward topology is that the full B-H swing causes automatic demagnetizing of the core. A standard Forward needs an extra reset winding or more complex circuits to achieve this.

The magnetization progresses in first one direction during a switching half-cycle and back again during the second half-cycle.

During the 'off' times the energy stored in the core continues to cause a current, but now it flows through the secondary windings which are connected together by the synchronous rectifiers. Since the SRs have very little 'on' resistance, this current doesn't create much voltage so the stored energy is not dissipated. The current essentially 'idles' until the next half-cycle on the primary.

Half-Bridge Transformer Core Reset

- **The Magnetizing Current increases during one half-cycle, then returns to the initial condition on the second half-cycle**



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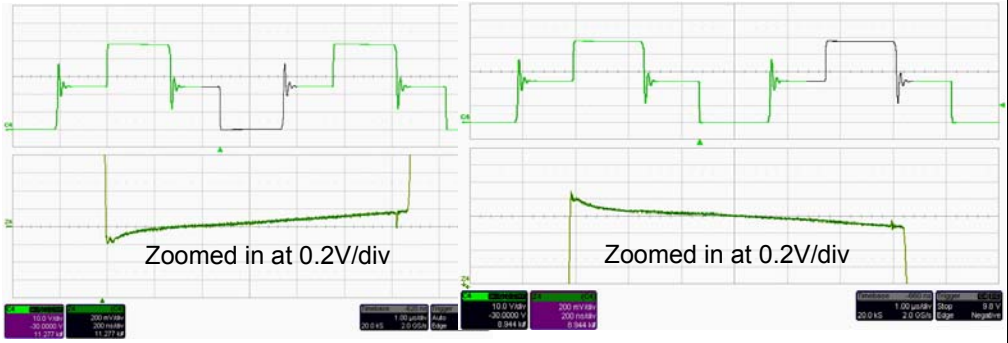
Perhaps this picture will help clarify. The magnetizing (and demagnetizing) current only changes during the primary power pulses. Otherwise, the current still flows but since it's a function of volt-seconds across the primary at relatively high voltage, the low voltage across the shorted secondary takes orders-of-magnitude more time to demagnetize the core.

Half-Bridge Transformer Core Reset

48V – No Load Traces



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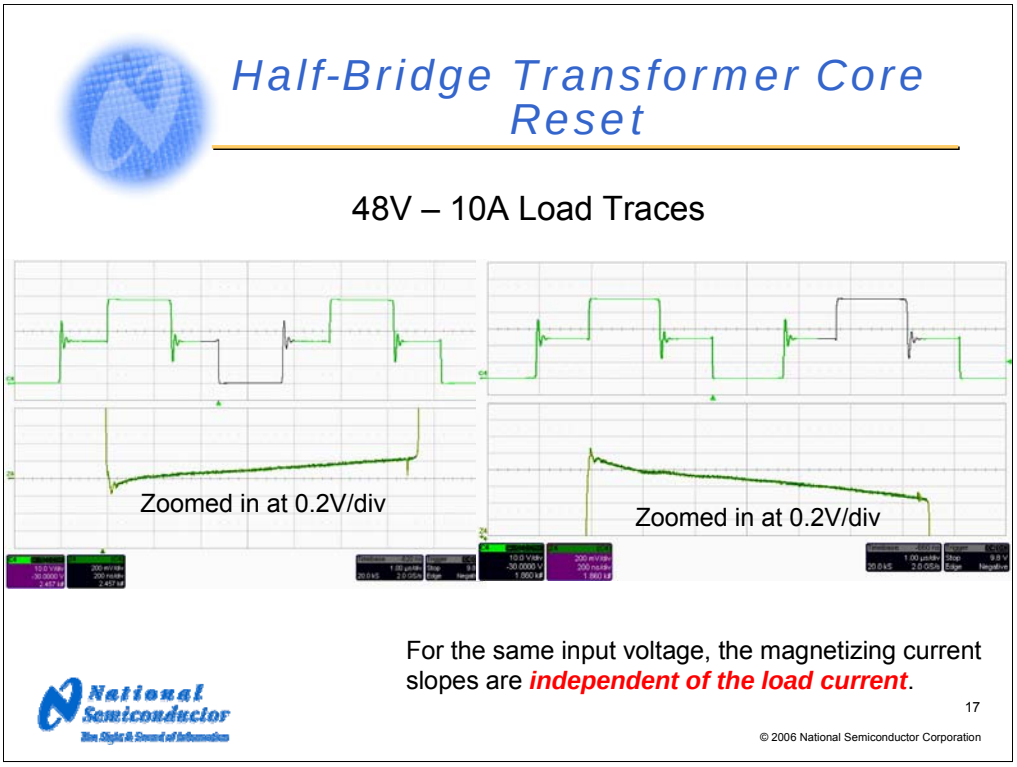
These scope traces and the traces on the following slide show the magnetizing and demagnetizing slopes on the switching pedestals. Note that the demagnetizing action of the transformer forces the low-side MOSFET drain below ground!

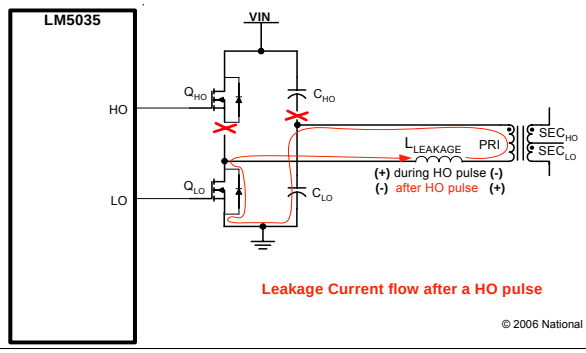


The previous slide showed the switch node with no load on the out. These traces show the switch node with a 10 amp output current. Note that the slope is the same in both cases.

Magnetization and demagnetization are independent of power load.

Half-Bridge Transformer Leakage Inductance

- Leakage Inductance in the Transformer is due to the physical difference in the Primary winding geometry and the Secondary winding geometry
- Total Leakage Inductance is the sum of the Transformer Leakage and PWB wiring
- The Primary MOSFET body diodes return the energy stored in Leakage Inductance to C_{LO} after a HO pulse, and C_{HO} after a LO pulse
- If Leakage Energy is low, it will just ***resonate with Q_{HO} and Q_{LO} Drain-to-Source capacitance***, which may need a snubber for emissions (worst case is full load)



Leakage Current flow after a HO pulse

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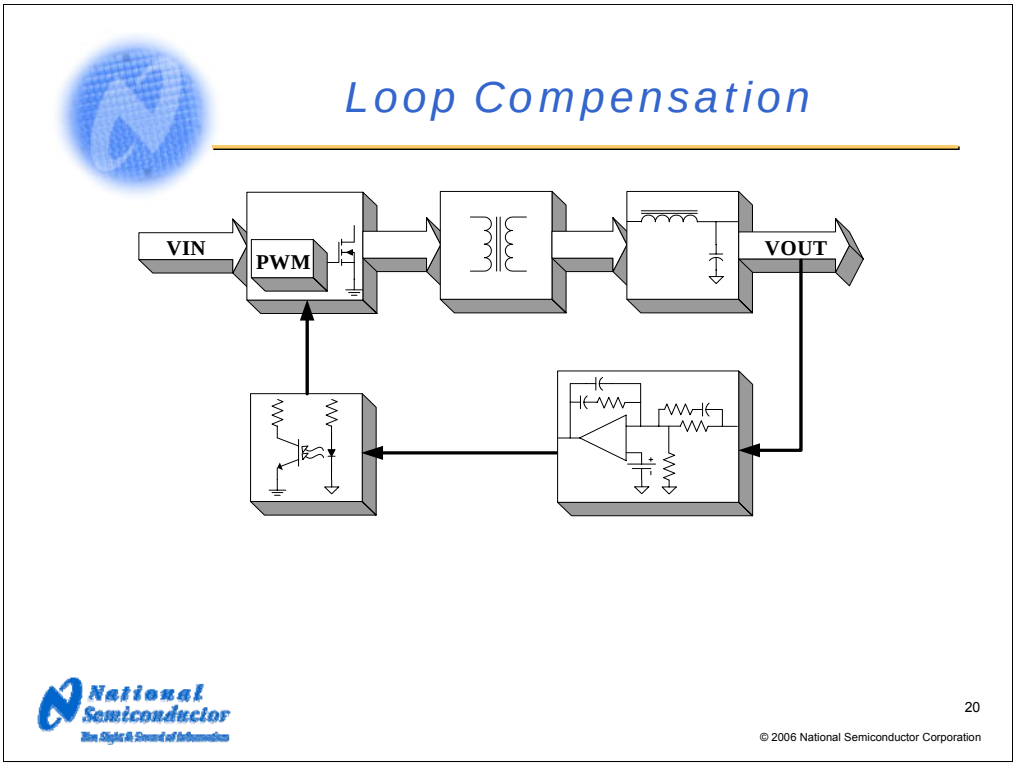
Leakage inductance is unavoidable in the real world. Since the primary windings and the secondary winding can't occupy exactly the same space, the will always be some small percentage of the energy that's not transferred and therefore is stored. Also, since the MOSFETs and capacitor have some routing length, they also store some energy.

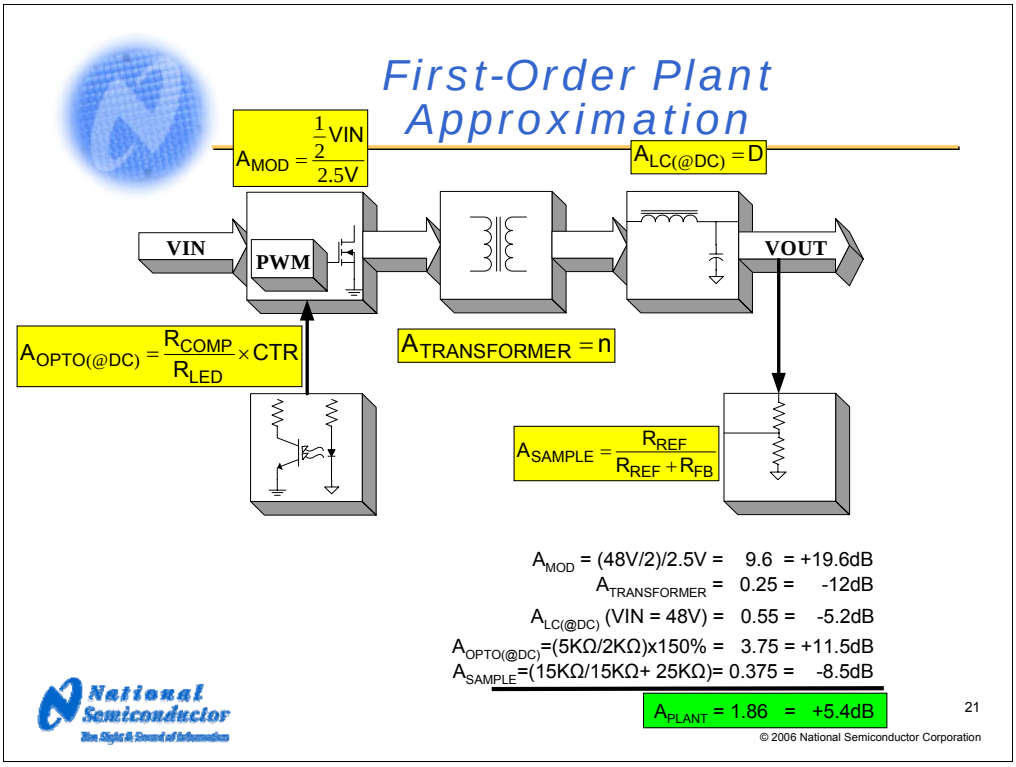
Half-Bridge topology automatically returns this energy to the input capacitors through the primary MOSFET body diodes. There is some loss due to the diode forward voltage, but additional clamping circuits aren't required.

If the leakage energy is low enough, instead of turning the body diodes 'on' the energy charges the drain-source capacitance and then oscillates with the magnetizing inductance and the capacitor divider. This can be snubbed with an RC if desired or dictated by radiated emissions testing.

Next we address loop compensation.



The voltage mode loop is shown with the Plant Gain represented by the optocoupler block, the modulator block , the transformer and the LC output filter blocks. The compensator block is responsible for providing sufficient gain to make the output voltage very nearly equal to the reference voltage (times a constant) and sufficient phase margin so that the output voltage doesn't ring or oscillate in response to a load step. At the same time, too much phase margin will cause the output voltage to respond too slowly to a load step. A good target phase is about 55º, though 45º is usually acceptable, and sometimes even 40º.



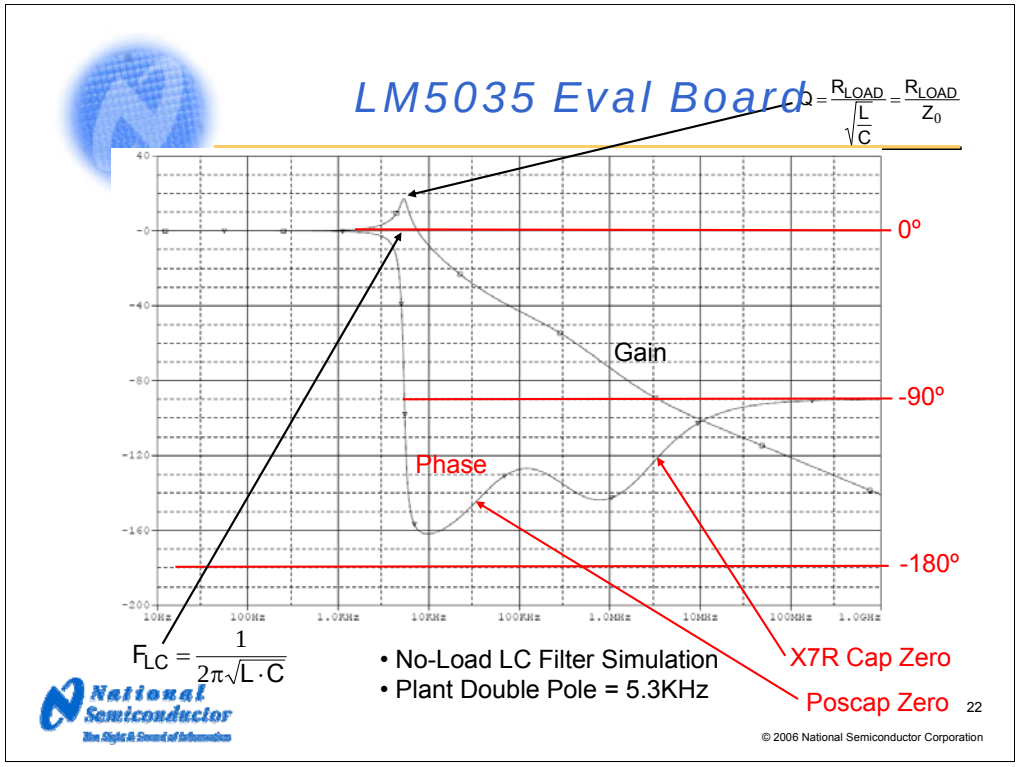
The Plant gain can be calculated for low frequency with a few simple equations. Doing so provides the approximate target for compensator gain at the Loop Unity Gain Frequency (LUGF), also referred to as the crossover frequency.

The LC output filter has -12dB per octave roll off from the resonant frequency, so choosing the LC resonance and the loop unity gain point tells the designer how much gain to provide in the compensator. To determine the number of octaves between LC resonance and loop unity gain, take the logarithm of the ratio and divide by the logarithm of 2 (either natural log or log base 10, it doesn't matter which).

The optocoupler can be approximated by the Current Transfer Ratio and the burden resistors, but in reality most have poor frequency response above 10KHz, so the measured Plant gain versus frequency will probably be influenced by this.

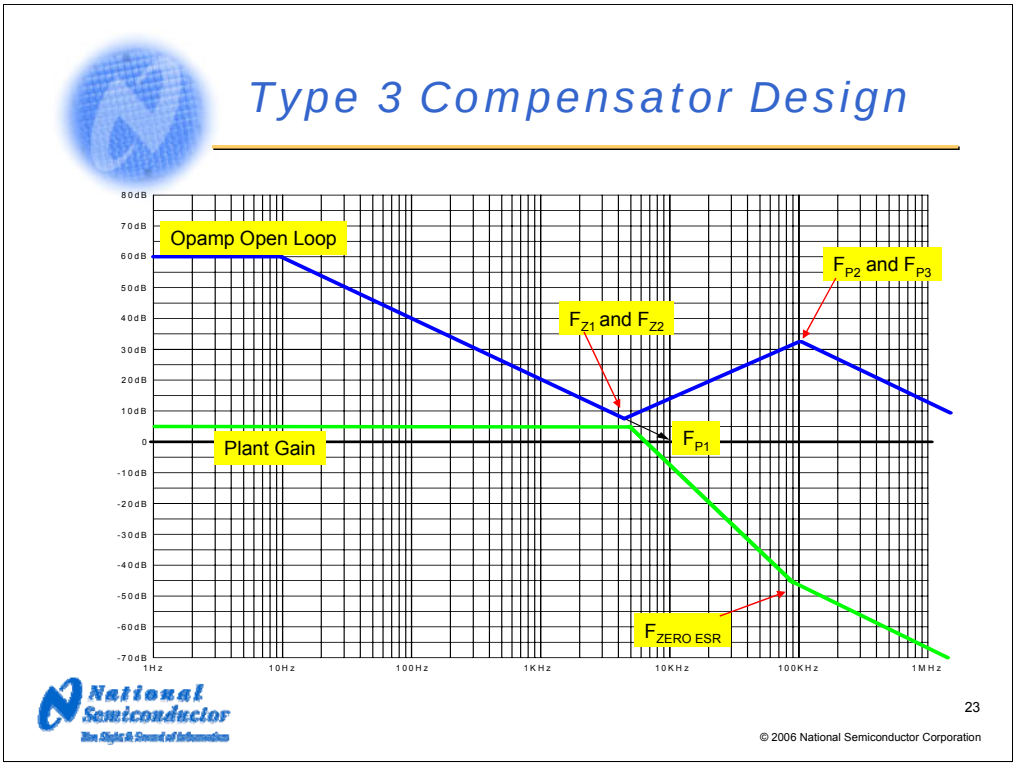
The modulator gain uses one-half VIN due to the Half-Bridge primary configuration. The 2.5V RAMP voltage assumes a feed-forward ramp that self adjusts for variations in VIN.

Finally, the output voltage sampling divider is a simple attenuator to match the output voltage to the reference voltage of the error amplifier.



This is a Pspice plot of the inductor and capacitors used on the LM5035 Evaluation Board, including the DCR and ESRs. The gain peaking pointed to by the Q arrow results from the load resistance being higher than the characteristic impedance of the LC network. When the load is 0.7 times the characteristic impedance, there is no peaking and the phase “crash” is not so severe.

The phase “crash” is the drop in phase by 160º in about one-tenth decade of frequency. The ESR of the POSCAP saves it from crashing 180º, which would be more difficult to compensate. Generally, if the additional ripple voltage can be tolerated, more ESR is better behaved (less phase loss) for voltage mode control.



This graph demonstrates the goals of a Type 3 compensator. The green line represents the Plant response with the LC filter's -40dB per decade slope from resonance to the output capacitor ESR zero, where it changes to -20dB per decade. On the -40dB slope, the phase shifts nearly 180º.

The blue line represents the compensator gain. The open loop gain is set by the opamp, and it's roll off is a -20dB per decade slope set by the input resistor and the feedback capacitors. Since low ESR capacitors are used in this example, the Plant's -40dB slope has to be compensated with a +20dB slope to be stable at the LUGF.

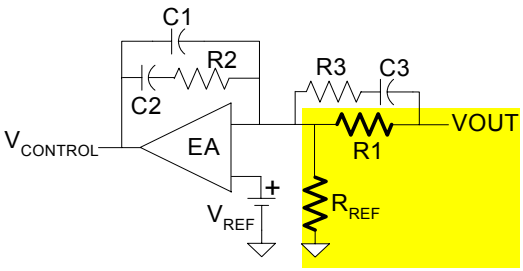
Placing the 2 zeros at a frequency lower than the LUGF provides this +20dB slope and causes phase boost that insures adequate phase margin at LUGF.

2 poles above the LUGF attenuates the loop's high frequency response to switching noise.

The ratio of the zeros to the LUGF should be the same as the LUGF ratio to the poles. This gives the peak boost at the LUGF. The further apart (larger ratio) the zeros and poles are, the greater the phase boost. The limiting factor is the amount of low frequency gain (particularly at 120Hz for input ripple) and the high frequency switching noise which causes jitter (noise) in the output voltage.

Type 3 Compensator Analysis

- **R1 and R_{REF} form the Error Amplifier Setpoint divider**
- **R_{REF} doesn't effect the Compensator transfer function.**
- **The voltage across R_{REF} is equal to V_{REF}.**



$$R_{REF} = \frac{V_{REF}}{\left(\frac{VOUT - V_{REF}}{R1}\right)}$$

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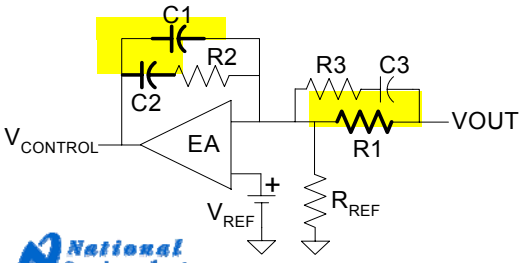
DC regulation is set by the ratio of R1 and RREF. The value of RREF is only important with respect to R1, and RREF doesn't effect the small signal transfer function. It can be calculated that increasing or decreasing RREF has an equal effect on it's ratio with R2 as it's ratio with R1.

R1 and RREF should be the highest precision in the design as they, along with the voltage reference, determine the ultimate accuracy of the converter.

Type 3 Compensator Analysis

- **The input resistance (R1) and the feedback capacitance (C1+C2) establishes the low frequency pole, where the open loop gain of the opamp begins to roll off**
- **$F_{P1\_UNITY\_GAIN}$ is the frequency that this pole crosses 0dB**
- **Rises 20dB/decade up to the opamp's open loop gain.**
- **F_{P1} should allow sufficient gain to attenuate 120Hz line ripple**



$$F_{P1\_UNITY\_GAIN} = \frac{1}{2\pi \cdot R1(C1+C2)}$$

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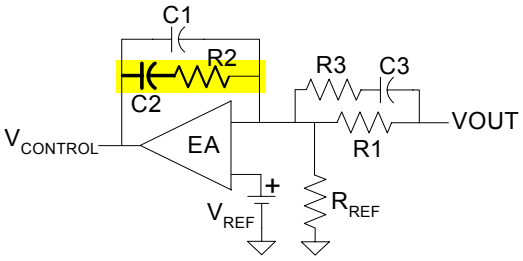
At very low frequencies, the Type 3 compensator is an integrator with theoretically infinite gain. This is desirable because the feedback error is the reciprocal of the loop gain, so infinite gain provides zero error. In reality, opamps don't have infinite gain, so this bounds the loop gain. Practical compensators typically have 60 to 80dB open loop gain.

The integrator components C1, C2 and R1 form a pole frequency that is not the usual roll off frequency, but the unity gain frequency. A single pole has -6dB per octave attenuation. To calculate where this pole causes the opamp open loop gain to roll off, the open loop gain is divided by 6dB and this is the number of octaves below the unity gain frequency where the roll off 'knee' is located.

The goal here is to get as much low frequency gain as possible while not moving this pole too close to the loop unity gain frequency so it's impossible for FZ1 and FZ2 to boost the phase enough to reach the phase margin target.

Type 3 Compensator Analysis

- **F_{Z1} is the frequency where the gain becomes flat and the phase boosts to compensate the double pole of the output LC filter, which creates -180º loss**



$$F_{Z1} = \frac{1}{2\pi \cdot R2 \cdot C2}$$

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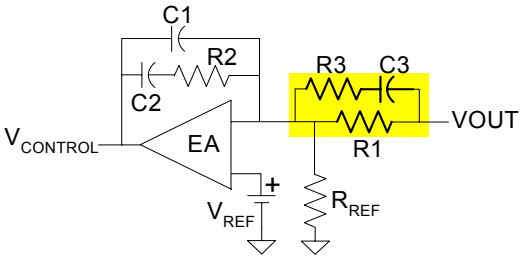
FZ1 is usually set equal to FZ2 below the loop unity gain frequency.

These zeros set the compensator gain at a level to counter the LC filter attenuation at the loop unity gain frequency.

They also boost the loop phase so that the LC filter poles don't cause oscillation.

Type 3 Compensator Analysis

- **The second zero frequency is usually the same as the first zero to turn the compensator response to +20dB per decade. When combined with the Plant's -40dB per decade slope, this insures that the loop crosses unity gain with a -20dB gain slope, important for stability.**



$$F_{Z2} = \frac{1}{2\pi \cdot (R1 + R3) \cdot C3}$$

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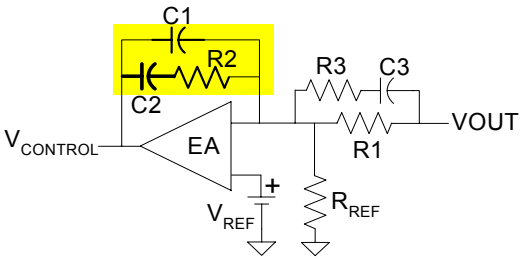
It's best for loop stability for the loop gain to be near a -20dB gain slope at the LUGF. The second zero frequency is usually the same as the first zero to turn the compensator response to +20dB per decade. When added to the Plant's -40dB per decade slope the converter meets this goal.

Type 3 Compensator Analysis

- **So that the EA doesn't respond to high frequency noise, F_{P2} begins to roll off the frequency response at around the ESR pole of the output filter capacitance**



$$F_{P2} = \frac{1}{2\pi \cdot R2\left(\frac{C1 \cdot C2}{C1 + C2}\right)}$$

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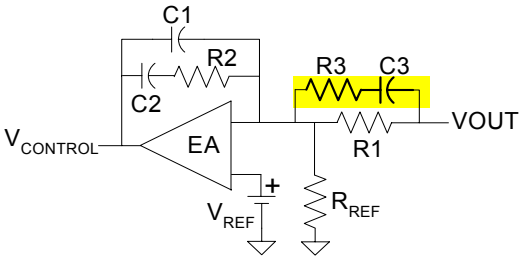
The zeros increase the high frequency gain, so 2 poles are added above the loop unity gain frequency to reject jitter caused by high frequency ringing and switching noise. If FP2 is placed at the output capacitor ESR zero, the pole phase loss is countered by the ESR phase boost to aid the loop stability.

Type 3 Compensator Analysis

- **F_{P3} is usually set at the same frequency as F_{P2} to prevent loop response to high frequency noise and switching noise**



$$F_{P3} = \frac{1}{2\pi \cdot R3 \cdot C3}$$

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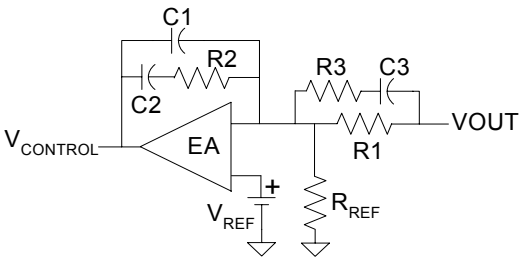
Ideally, the compensator response would drop to zero above the loop unity gain frequency, but placing poles to close would ruin the phase margin since poles begin causing phase effects a decade in frequency below the pole and continue a decade above.

Switching noise is usually present throughout the converter, so FP3 further reduces the high frequency response to attenuate it.

Type 3 Compensator Design



$$R2 = R1 \cdot Plant\_Gain@UGF$$

$$C1 = \frac{1}{2\pi \cdot R2 \cdot F_{P2}}$$

$$C2 = \frac{1}{2\pi \cdot R2 \cdot F_{Z1}}$$

$$C3 = \frac{1}{2\pi \cdot R1 \cdot F_{Z2}}$$

$$R3 = \frac{1}{2\pi \cdot C3 \cdot F_{P3}}$$

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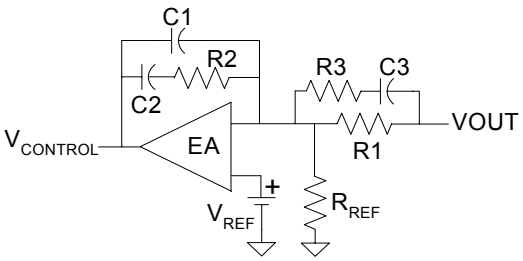
The set of equations discussed in the previous slides analyze an exiting design. To begin a design, first choose a ratio of resistor values for R1 and R2 to provide the compensator gain required to counter the Plant Gain (loss) at the loop unity gain frequency (LUGF) as determined from the plant DC gain, the resonant frequency of the LC filter and -12dB per octave (or -40dB per decade) attenuation between LC resonance and LUGF. Resistor thermal noise is better if the values are kept below 100KΩ.

The values of C1, C2, C3 and R3 are then determined by using the R1 and R2 values in the rearranged analysis equations.

Type 3 Compensator Analysis



$$F_{P1\_UNITY\_GAIN} = \frac{1}{2\pi \cdot R1(C1+C2)}$$

$$F_{Z1} = \frac{1}{2\pi \cdot R2 \cdot C2}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R1+R3) \cdot C3}$$

$$F_{P2} = \frac{1}{2\pi \cdot R2\left(\frac{C1 \cdot C2}{C1+C2}\right)}$$

$$F_{P3} = \frac{1}{2\pi \cdot R3 \cdot C3}$$

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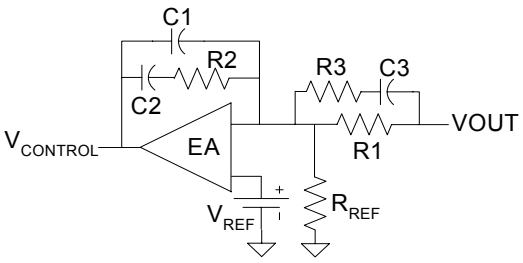
So this is the set of equations that determine the frequency response of the converter. Next, to put it all together and calculate the compensator phase, the ‘j’ operator is introduced into the compensator gain equation.

Type 3 Compensator Transfer Function



$$G(j\cdot f)=\frac{\left(1+\frac{j\cdot f}{F_{Z1}}\right)\left(1+\frac{j\cdot f}{F_{Z2}}\right)}{\frac{j\cdot f}{F_{P1}}\left(1+\frac{j\cdot f}{F_{P2}}\right)\left(1+\frac{j\cdot f}{F_{P3}}\right)}$$

$$\varphi(f)=\frac{180}{\pi}\cdot\arctan\left(\frac{\mathrm{Im}(G(j\cdot f))}{\mathrm{Re}(G(j\cdot f))}\right)$$

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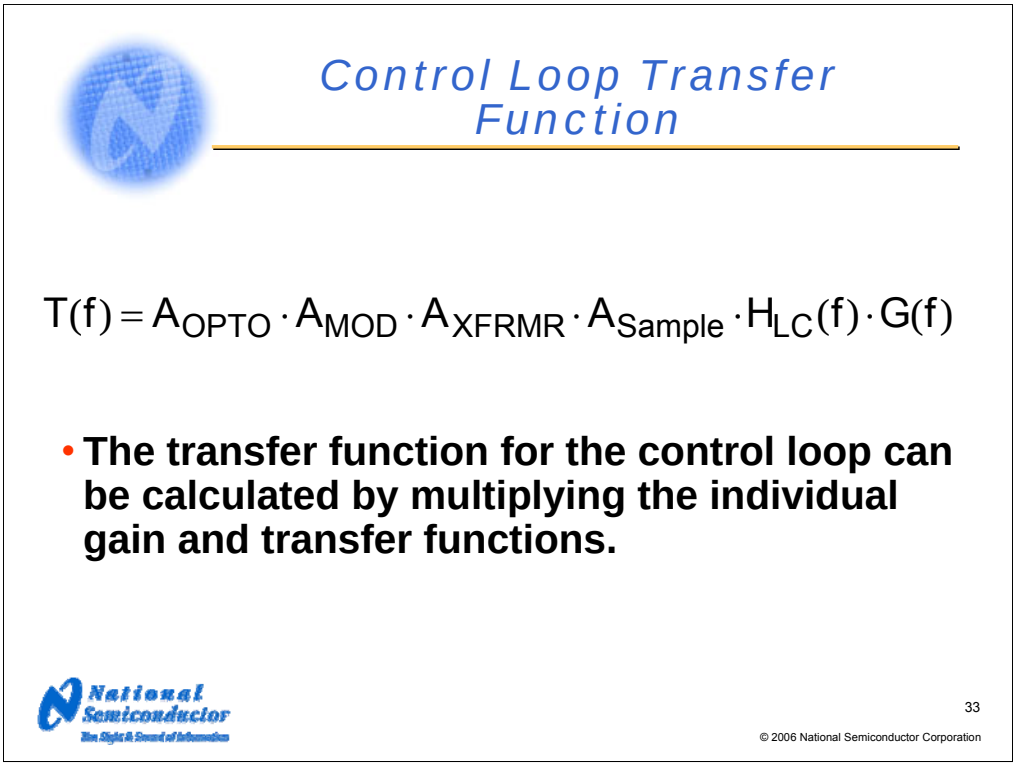
I choose to present the compensator gain equation as a function of frequency rather that a function of ‘s’ for simplicity. You can substitute ‘s’ for j*f and delete all the 2π’s if you like.

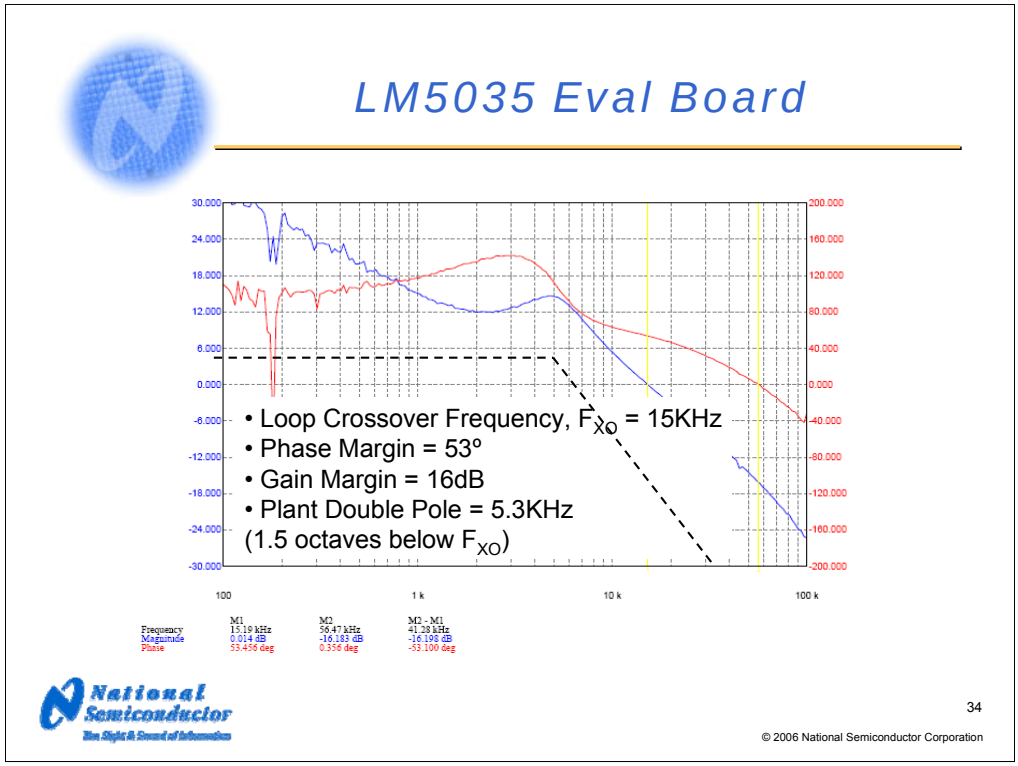
To calculate the phase (in degrees) the arctangent is taken of the ratio of the Imaginary part of the transfer function to the Real part, and multiplying it by 180 divided by π.



Taking the product (or the sum in dB) of all the loop elements predicts the loop performance. Since these are first order approximations and a lot of parasitic details have been glossed over, this is just a starting point for the loop analysis. The next step is empirical observation and iteration.

Once the module has been assembled with the calculated components, a network analyzer (such as Ridley's, Venable's, Agilent's, etc.) is used to determine the accuracy of the prediction for gain and phase.

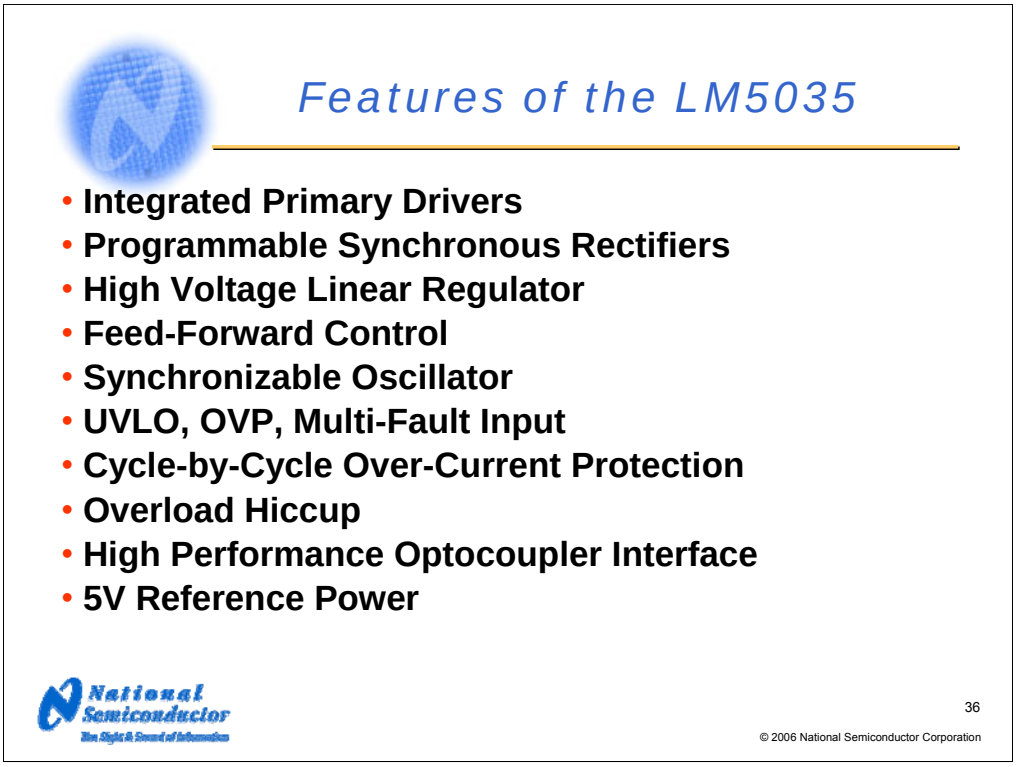
Alternately, a hand wound transformer, a signal generator and a scope can be used, but this is both significantly less accurate and significantly more time consuming.



For reference, this is a plot from a Ridley AP200 Analyzer showing the loop gain of the LM5035 Evaluation Board in blue and the loop phase in red. The approximate LC filter transfer function is shown with a black dashed line to indicate where the gain resonance is and the phase 'crash'.

Note that the compensator provides 53º phase margin at the loop unity gain frequency of 15KHz and the gain is down 16dB when the phase crosses zero (gain margin).

The LM5035 is highly integrated Half-Bridge controller and driver that began full production in March 2006.



The LM5035 is a full-featured controller and driver chip available from National Semiconductor. For highly compact 'brick' designs, the LM5035 has the integrates many functions that previously required additions chips and circuitry. Available in a thermally enhanced 20 pin TSSOP package and even smaller 24 pad leadless LLP package (4mm x 5mm), the LM5035 provided all of the primary side functions needed for a 'brick' in a minimum volume.

Included are high current MOSFET drivers, synchronous secondary FET controls that optimize delays with user programmability for greater efficiency, a start-up regulator that is 105V tolerant, feed-forwarding for optimal line regulation, the ability to switch at up to 2 MHz with an internal oscillator, Under Voltage Lock Out and Over Voltage Protection, both of which can be used for alternate functions such as Remote Thermal Protection, Latched Secondary Over Voltage Protection, etc.

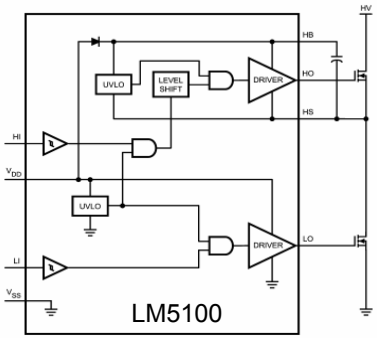
The LM5035 uses voltage mode control, but cycle-by-cycle current limiting is also provided. This function can be used alone, or is user programmable for Hiccup duration.

Since Half-Bridge designs typically are isolated, the LM5035 has a current-mirror COMP interface which improves common optocouplers bandwidth. Common optocouplers have a pole between 5 and 10KHz due to the large base-collector capacitance necessary for a good Current Transfer Ratio. The current-mirror interface holds the base-collector voltage constant, which moves the optocoupler pole up above 50KHz. Optocouplers are no longer the limiting factor in the design.

Precision +5V power is provided to operate the optocoupler, as well as other fault sensing circuitry.

Integrated Primary Drivers

- **Single chip Primary solution for compact designs**
- **2 amp, 15ns risetime**
- **Derived from the LM5100**
- **Can be configured for dual low-side operation (i.e. Push-Pull)**
- **For Offline (>105V) applications, HS is grounded and HO drives a Gate Transformer**
- **HB pin can be driven to 118V**



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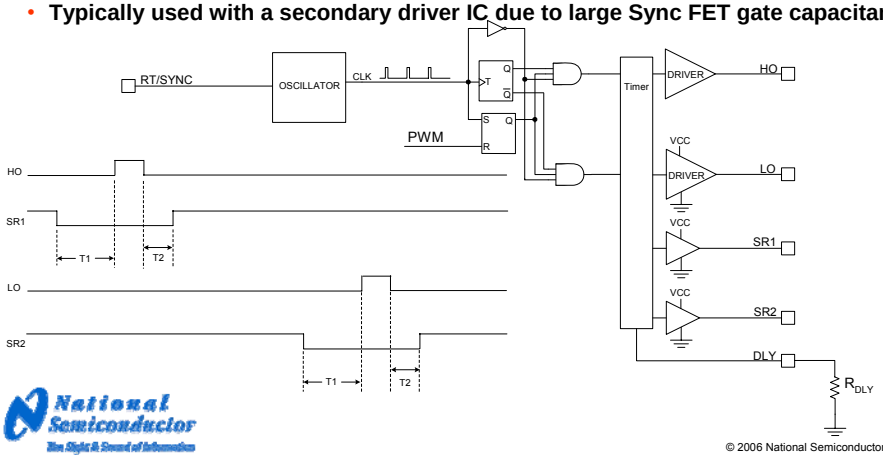
LM5035 uses the proven technology of the LM5100 driver IC. Two-amp-current-drive switches large gate charge MOSFET with 15 nanosecond risetime to reduce transition power loss. These high voltage outputs can drive the high-side gate to as much as 118 volts.

Other optional configurations include driving a gate transformer for offline applications (120VAC, 240VAC, etc.). Also, the LM5035 can be configured as a Push-Pull controller, with both drivers referenced to ground.

Programmable Synchronous Rectifiers

- **0.5 amp Non-Overlapping Isolated Secondary drivers**
- **RDLY tunes the deadtime to optimize Sync FET efficiency while preventing Shoot-Thru conduction**
- **Leading edge timer (T1) is twice the trailing edge timer (T2)**
- **Typically used with a secondary driver IC due to large Sync FET gate capacitance**



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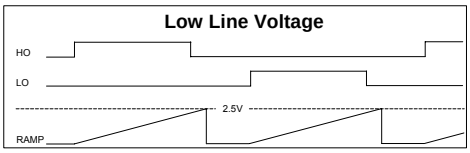
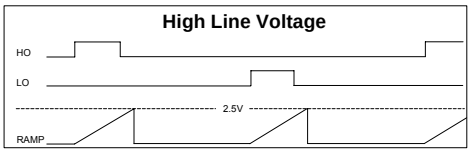
Half-amp-synchronous FET drivers can drive the secondary MOSFETs through a gate transformer or, for large gate charge and paralleled MOSFETs for greater low-output-voltage efficiency, drive an isolated driver IC.

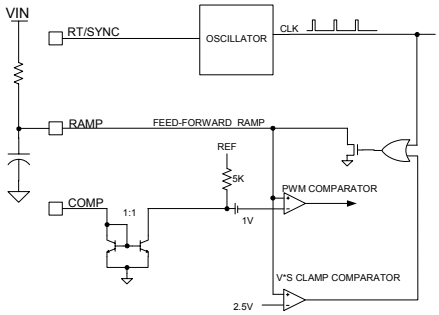
User programmable lead and trailing edge deadtime offers flexibility for various layers of propagation delays. Therefore shoot-through is not a concern and optimal efficiency is controllable.

Feed-Forward Control

- **Provides Current-Mode like Line Regulation in Voltage-Mode**
- **Limits 'transient condition' PWM pulse widths**







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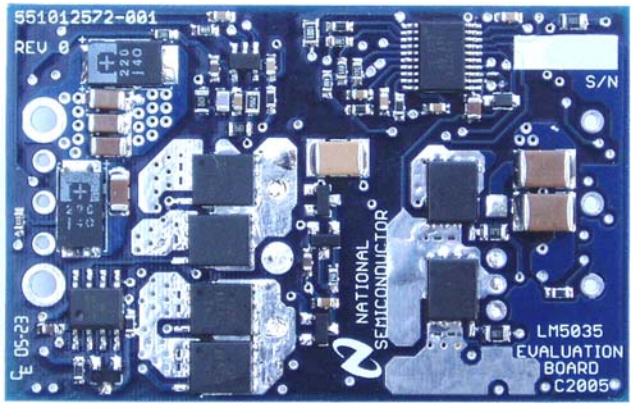
Input voltage feed-forwarding provides the line regulation advantage of current mode control, while maintaining the superior noise immunity of voltage mode control. Feed-forwarding changes the PWM comparator RAMP slope with changes in the input voltage, so the loop transfer function is not effected by change in VIN and the loop does experience an 'adjustment lag time' for input disturbances.

An evaluation board is available from the National Semiconductor website (part number LM5035EVAL) to experience the performance of the LM5035 IC.

LM5035 Evaluation Board



- 36 to 75V input
- 3.3V @ 30 amps output
- Quarter-Brick format (2.28” x 1.45” x 0.5”)

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This is a picture of the evaluation board for the LM5035. It is a 100 watt converter in quarter-brick format. The unused space indicates that the high level of integration provided by LM5035 could enable further space reduction.

The TSSOP package in the upper right corner is the LM5035. Below it are the primary side MOSFETs and the four packages to the left are the secondary side synchronous MOSFETs.

LM5035 Evaluation Board

- 36 to 75V input
- 3.3V @ 30 amps output
- Quarter-Brick format (2.28” x 1.45” x 0.5”)

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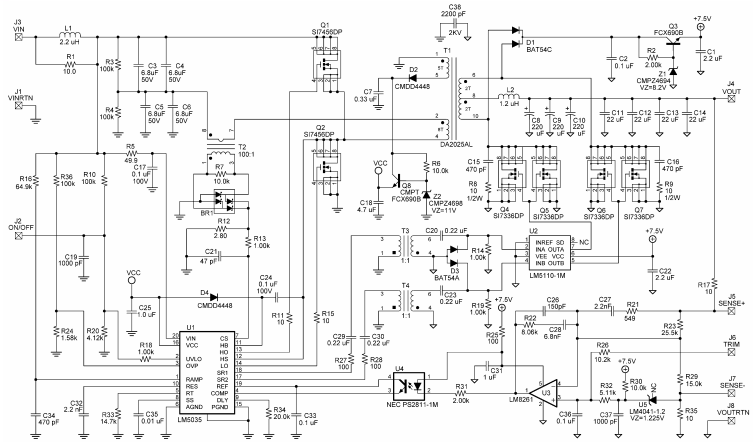
This is the magnetics side view of the evaluation board. Again, alternate construction of these components would allow perhaps an eighth-brick format.

LM5035 Evaluation Board



- 36 to 75V input
- 3.3V @ 30 amps output
- Quarter-Brick format (2.28” x 1.45” x 0.5”)
- Schematic details shown in appnote AN-1435

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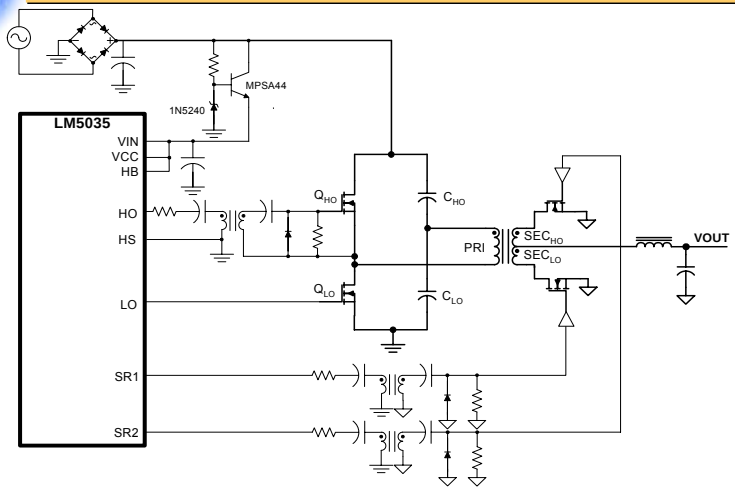
This schematic for the reference design is shown in the LM5035 datasheet and in application note AN-1435 along with the PWB artwork and the Bill Of Materials. Both are available on the National Semiconductor website.

In addition to the design shown in previous slides, two more circuits are presented in the next slides.

Offline Half-Bridge Converter



- HO FET uses same Gate Transformer circuit as SRs
- VCC circuit costs a few pennies

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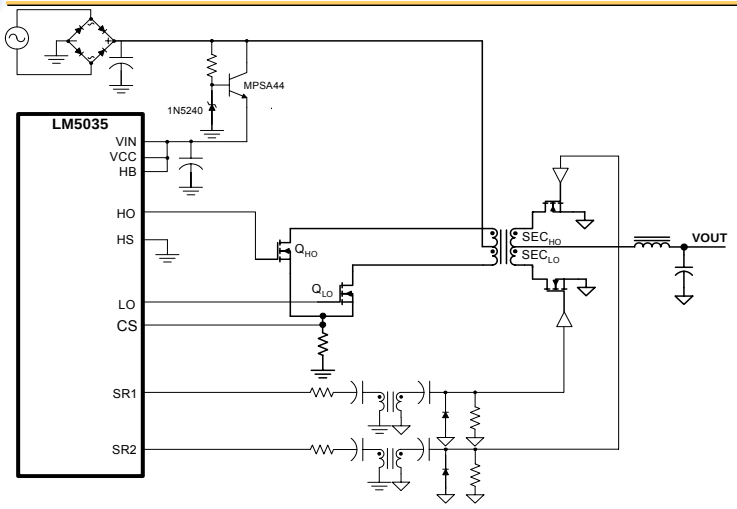
For Offline applications where the supply voltage is 120VAC or 240VAC, the LM5035 can be used with the HO driver connected to ground and the HO drive supply pin (HB) connected to VIN and VCC.

The same gate transformer circuit used for the SR drivers is inserted between HO and the high-side MOSFET gate.

Since VIN is only rated to 105V, a high voltage NPN and a 10V zener diode is used to supply VIN, VCC and HB. Since the current required is low (maybe 10 mA) and the NPN is in use only until the AUX winding on the power transformer begins supplying power, this circuit can be very small and inexpensive.

Offline Push-Pull Converter



- No Gate Transformer circuit required
- Current Sense Transformer replaced by resistor

Another configuration is Push-Pull. This too can be an offline design using the same NPN bias circuit. In Push-Pull, the cycle-by-cycle current limit can be provided with a sense resistor instead of a current transformer.

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Thank you for attending!

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