An Improved Isolated MOSFET Gate Driver Scheme for Wide Duty Cycle Applications

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***Abstract*—An improved transformer coupled gate driver scheme for high speed switching applications in power supply or motor drive is proposed in this paper. It improves the deficiencies caused by the conventional transformer coupled gate driver scheme, such as oscillation of the output PWM signal that will make MOSFET improper turn-on, when the duty cycle of input PWM signal reduces from large value to small value suddenly or turn off. Good performance is achieved using this driver scheme in a digital controlled synchronous rectifier (SR) Buck converter. Operation principle of the proposed scheme is described. Design procedure and experiment results of the scheme are explained and provided in details.**

Keywords-driver scheme;isolated mosfet gate drive; wide duty cycle; high frequency

I. INTRODUCTION

Transformer coupled MOSFET gate driver circuits provide higher level of protection, isolation, immunity from transient or common mode noise rejection than integrated chip driver circuits. However, some fatal deficits exist among the transformer coupled gate driver schemes for wide duty cycle application which are widely adopted nowadays. The transformer coupled gate driver circuit will perform an uncontrolled behavior when duty cycle reduces dramatically or turn off [1].

A new scheme was proposed which showed good performance in simulation [2]. But it does not work well in practical application. The output duty cycle of the driver is always smaller than the input duty cycle. The reason of this non-ideal situation is analyzed in this paper. To solve this problem, an improved scheme is presented here.

II. PROMBLEMS IN THE FORMER DRIVER SCHEME

A driver scheme has been proposed which had good performance in simulation. However, this circuit does not work well in practice. A practical circuit is built as Fig. 1 [2]. The turn ratio of the transformer is 1:1:1. To verify the performance of the driver, a programmed input PWM signal is given. The frequency is set to a fixed 300kHz, the duty cycle increases gradually. Once it reaches 0.8, the duty cycle reduces to 0.1 immediately, and increases gradually once again. The output PWM signal of the circuit is shown as Fig. 2. It can be seen that the PWM signal is distorted, some small duty cycle signal is lost.

This distortion is caused by the parallel capacitor C_{ds} of Q1. It is in series with the level-shift capacitor C2 and the secondary side inductor of the transformer. The equivalent circuit is shown as Fig. 3. When the PWM signal is given by the controller or diver chip, C2 and C_{ds} make the secondary side of the transformer instantaneous short circuit, shown as Fig. 4. This is the drawback of adding Q1 to this driver circuit.

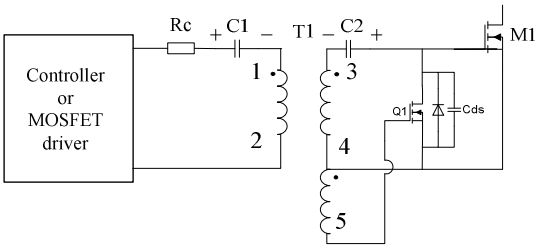

Figure 1. A practical circuit for wide duty cycle application.

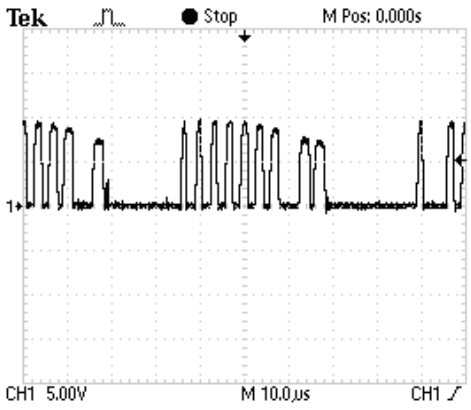

Figure 2. The output PWM signal of driver as shown in Figure.1.

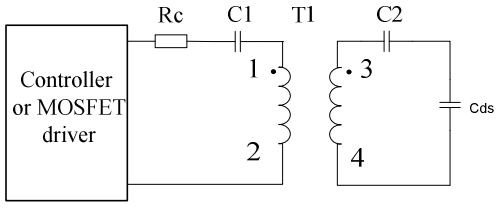

Figure 3. The equivalent circuit of Figure.1.

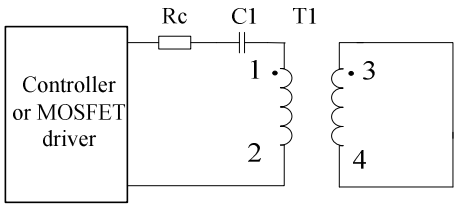

Figure 4. Instantaneous shot circuit status.

III. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

In this paper, an improved scheme is given which solves the problem mentioned above and shows good performance in a digital controlled SR buck converter. A resistor is adding to the circuit in series with Q1, shown as Fig. 3(a). Since this resistor can restrict the charging current to the C_{ds}, the output PWM signal is improved significantly. Fig. 3(b) shows that the output PWM signal can follow the input PWM signal exactly. The value of R1 will affect the performance of the scheme. When it is too small, the short circuit current is not restrained effectively, the output PWM signal will distort again. On the other side, when it is too large the discharging current of C2 will be reduced, the output PWM signal will oscillate again when the duty cycle is reduced suddenly. In this application, a well performed value is chosen between 20 and 30 ohm. In addition, sudden changes in duty ratio will excite the L-C resonance tank formed by the magnetizing inductance of the gate drive transformer and the coupling capacitor. In most cases this L-C resonance can be damped by inserting a low value resistor Rc in series with Cc. The value of Rc includes the equivalent series resistance of other components in the circuits.

It can be seen from Fig. 3(b) that when the duty cycle is small, the high level of PWM is below 5V that is not adequate to drive MOSFET. Although we could change the turn ratio of the transformer to 1:2:2, so the high voltage level of the output PWM signal can be above 5V, it will decrease the output current of the driver circuit and further degrade the driving ability of the circuit, besides it makes the transformer larger and heavier. An alternative solution is to use two driver chips with two complementary signals to drive the transformer, shown as Fig. 4(a). The voltage level of the input PWM signal is doubled comparing to single driver chip. With 1:1:1 turn ratio of the transformer, the output PWM signal voltage level is also doubled, shown as Fig. 4(b).

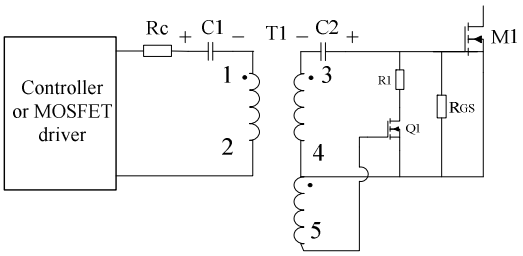

Figure 5. A proposed driver circuit based on Figure.1.

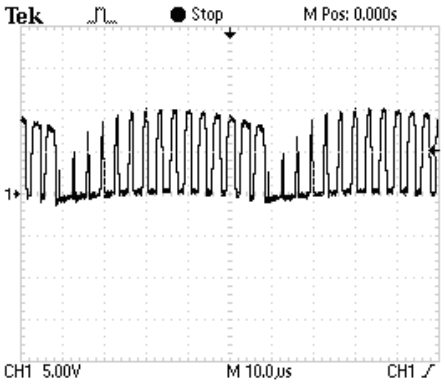

Figure 6. The waveform of the output PWM signal.

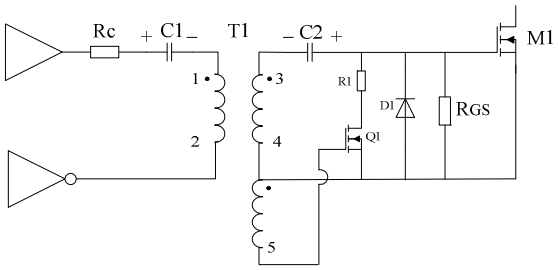

Figure 7. An improved driver scheme.

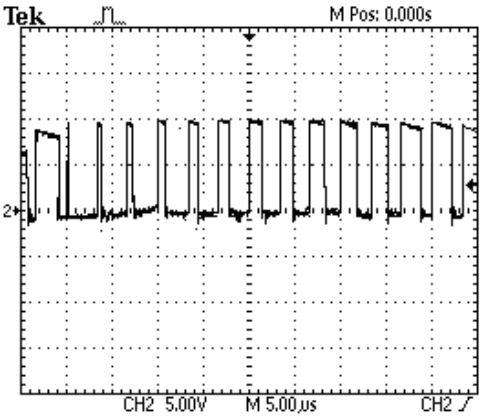

Figure 8. The waveform of the output PWM signal.

IV. PARAMETERS CALCULATION OF THE DRIVER SCHEME

In this section, a practical driver circuit in Fig. 4(a) working at 300kHz is taken as an example to demonstrate how to calculate the value of components.

A. Calculation of the Capacitors

There are two capacitors in this driver. Their values are dependent on the maximum allowable ripple voltage and the amount of charge passing through the capacitor in steady state operation [3].

$$C_{C2} = \frac{Q_G}{\Delta V_{C2}} + \frac{V_{DRV} \cdot D_{MAX}}{\Delta V_{C2} \cdot R_{GS} \cdot f_{DRV}} \quad (1)$$

Where V_{DRV} is the turn-on voltage of the driver chips, V_{DC2} is the DC voltage on C2, Q_G is the amount of gate charge of the MOSFET. In this example, given $f_{DRV} = 300kHz$, $R_{GS} = 1k\Omega$, $D_{MAX} = 1$, $Q_G = 30nC$, $\Delta V_{C2} \approx 0.1V_{DRV} = 1V$, $V_{DC2} = V_C - V_D = V_{DRV} \cdot D - V_D$, it can be derived from (1) that

$$\begin{aligned} C_{C2} &= \frac{Q_G}{\Delta V_{C2}} + \frac{(V_{DRV} - V_{DC2})D_{MAX}}{\Delta V_{C2} \cdot R_{GS} \cdot f_{DRV}} \\ &= \frac{Q_G}{\Delta V_{C2}} + \frac{(V_{DRV} - V_{DRV}D_{MAX} + V_D)D_{MAX}}{\Delta V_{C2} \cdot R_{GS} \cdot f_{DRV}} \\ &= \frac{30nC}{1V} + \frac{(10V - 10V \times 1 + 0.7V) \times 1}{1V \times 1 \times 10^3 \Omega \times 300 \times 10^3 Hz} = 32.3nF \end{aligned}$$

The larger value C2 is chosen, the lower ripple voltage can achieve. That is good for the performance. So a ceramic capacitor of 0.1uF is chosen for C_{C2}.

Calculation of the primary side capacitor C_{C1} is similar to C_{C2}, except that the magnetizing current of the gate drive transformer generates an additional ripple component.

$$C_{C1} = \frac{Q_G}{\Delta V_{C1}} + \frac{(V_{DRV} - V_{DC2})D}{\Delta V_{C1} \cdot R_{GS} \cdot f_{DRV}} + \frac{V_{DRV} \cdot (D^2 - D^3)}{\Delta V_{C1} \cdot 4 \cdot L_M \cdot f_{DRV}^2} \quad (2)$$

Where L_M is the magnetizing inductance of the gate drive transformer. Given D=0.8, $\Delta V_{C1} \approx 0.1V_{DRV} = 0.1 \times 10V = 1V$, it can be derived from (2) that

$$\begin{aligned} C_{C1} &= \frac{Q_G}{\Delta V_{C1}} + \frac{(V_{DRV} - V_{DC2})D}{\Delta V_{C1} \cdot R_{GS} \cdot f_{DRV}} + \frac{V_{DRV} \cdot (D^2 - D^3)}{\Delta V_{C1} \cdot 4 \cdot L_M \cdot f_{DRV}^2} \\ &= \frac{30nC}{1V} + \frac{(10V - 8V + 0.7V) \times 0.8}{1V \times 1 \times 10^3 \Omega \times 300 \times 10^3 Hz} \\ &+ \frac{10V \times (0.8^2 - 0.8^3)}{1V \times 4 \times 300 \times 10^{-6} H \times (300 \times 10^3 Hz)^2} \\ &= 30nF + 7.2nF + 11.9nF = 49.1nF \end{aligned}$$

Likewise, a ceramic capacitor of 0.1uF is chosen for C_{C2}.

B. Gate Drive Transformer Design

The gate drive transformer design is very similar to a power transformer design. The number of turns of the primary winding can be calculated by the following equation [4]:

$$N = \frac{V_{DRV}}{4 f_{DRV} B_{\max} A_c} \times 10^8 \quad (3)$$

Where $B_{\max}$ is the maximum magnetic flux density, A_c is the saturation magnetic.

Toroidal core T $12 \times 3 \times 6$ from TDK corporation is selected as the core of the transformer. The saturation magnetic flux density $B_s = 3300G$, the effective area of the core $A_c = 0.0865cm^2$, $B_{\max} = \frac{1}{3} B_{sat} = \frac{1}{3} \times 3300G = 1100G$, it can be obtained that

$$N_{pri} = \frac{10V}{4 \times 300kHz \times 1100G \times 0.0865cm^2} \times 10^8 = 8.76$$

The number of turns of the primary winding is 9 in this example. The turn ratios of transformer is 1:1:1.

C. Chosen of Other Components

To make sure C2 can be discharged enough during operation, Q1 must have low gate threshold voltage. RJK005N03 is suitable for low voltage gate drive application. D1 is a schottky diode. The driver chips are TC4420 and TC4429 from Telcom company.

V. CONCLUSION

This paper presents an improved transformer coupled gate driver scheme for wide duty cycle applications. Compared with conventional transformer coupled gate driver schemes, the output PWM signal of this scheme can follow the input PWM signal well even when the duty cycle is reduced suddenly or turn off. This driver scheme is designed and tested in detail and can behave good performance in high frequency switching power supply and motion control.

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