FARADAY
TECHNOLOGY CORPORATION

Guideline

Faraday 0.13µm Standard Cell Library FSC0G_D Layout / P&R Guideline

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Version 1.0

Revision History

Date	Rev.	Author	Reason for rewrite	Original conditions	New conditions	Sections effected
June 2004	1.0	Sean Fan	Original	—	—	—

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1. Introduction

This guideline includes layout rules and place and route (P&R) rules on Faraday FSC0G_D 0.13µm standard performance standard cell library applicable to your design. The P&R information provides definitions for each cell. The layout guide describes the layout rules for the following items:

- Grid
- Cell width
- Cell height
- Cell name
- Pin text
- Boundary rules
- ESD rules
- Latch-up rules
- Cell structure

2. Layout guide

2.1. General layout rules

The following layout rules are used for designing chips using Faraday FSC0G_D 0.13µm standard performance, standard cell library. This library is implemented according to UMC's 0.13µm SP process. These layout rules provide you with a standardized set of rules for performing place and route operations. It is very important that you follow these rules. Failure to follow these rules may cause your entire chip to fail.

Table 1. General layout rules

Item	Parameters / examples	Description
Place and routing grid	X-grid = 0.4µm width	Routing pitch
Place and routing grid	Y-grid = 0.4µm height	Routing pitch
DB grid	0.01µm resolution	DB = database
Editing grid	0.01µm resolution	Users can snap 0.01µm widths and heights in editing environment
Cell multiplication rules	Cell width / X-grid = integer	For grid widths
Cell multiplication rules	Cell height / Y-grid = integer	For grid heights
OPUS cell naming rules	INVCHD	In the OPUS environment, the cell name should be in uppercase only. (see Notes 1 and 2)
GDSII cell naming rules	invchd.gds	The GDSII file name should be in lowercase only. (see Notes 1 and 2)
Cell origin	X = 0, Y = 0	The cell origin should be located at the cell's "00" location.
Cell boundary	"outline"	Each cell's boundary should be clearly identified. This can be achieved by drawing a box in the layer named "outline". The box's width in outline layer should be the same as the cell's width.
Pin text syntax	"Pin name: Pin direction"	The direction for each pin (including VCC and GND pins) must be specified. (see Notes 3)
Boundary rules	• metal1➔ top metal • n-well • diff • P+imp	The space between the border objects and the boundary should be half of the width given for each metal, following UMC's design rule specifications. (see Notes 4)
Rule type	ESD	Must follow UMC rules
Rule type	Latch-up	Must follow UMC rules

Notes:

1. The cell name should be added at the cell origin. The layer's name used for cell name text should be "special".
2. It is important that the cell name is consistent with the file name.
3. Faraday removes all pin direction text from Milkyway's core cell views. This is done so pin extractions will go smoothly.
4. Make sure that no DRC violation occurs while conducting a cell abutment.

There are many types of pins. Each pin is designed to operate in a specific direction. The exact direction for each pin type is listed in Table 2 as follows:

Table 2. Pin directions

Types	Directions	Descriptions
I	Input	Without antenna diode
ID	Input	With antenna diode
SI	Input	Check ESD rules
O	Output	No ESD rule
SO	Output	Check ESD rules
B	Bi-direction	No ESD rule
SB	Bi-direction	Check ESD rules
P	Power	General use
G	Ground	General use

2.2. Core cell's layout rules

Table 3. Core cells layout rules

Items	Parameters / examples	Descriptions
Cell height	Eight (8) Y grids = 3.2µm	The cell height must be 3.2µm.
Routing layers in cell	metal1	The core cell has only one routing layers, metal1.
Pin text	"m1text"	• This pin text is required for each pin. • The pin text must be on-grid. • X-coordinate / (1/2 X-grid) = odd_number • Y-coordinate / (1/2 Y-grid) = odd_number • The layer name used for the pin text is "m1text"
Rail's width	0.56µm	Power ground rail width
Lower left ground rail	X = 0 Y = -0.28	The ground rail's location.(see Figure 1)

Items	Parameters / examples	Descriptions
Upper right ground rail	X = cell width Y = 0.28	The ground rail's location. (see Figure 1)
Lower left power rail	X = 0 Y = 2.92	The power rail's location. (see Figure 1)
Upper right power rail	X = cell width Y = 3.48	The power rail's location. (see Figure 1)
Lower left N-well	X = -0.32 Y = 1.54	The N-well's location (see Figure 1)
Upper right N-well	X = cell width +0.32 Y = 4.00	The N-well's location (see Figure 1)
Lower left P+ implant	X = -0.12 Y=1.68.	P+ implant's location (see Notes 1)
Upper right P+ implant	X = cell width +0.12 Y = 3.06	P+ implant's location (see Notes 1)
Lower left N+ implant	X = -0.12 Y = 0.14	N+ implant's location (see Notes 2)
Upper right N+ implant	X = cell width +0.12 Y = 1.68	N+ implant's location (see Notes 2)
Grid line	"phyname"	• The grid line must be on-grid ([2n+1] * [1/2 grid]). • Its layer name is "phyname".

Notes:

1. The top edge must be positioned 0.14µm inside the cell's boundary.
2. The bottom edge must be positioned 0.14µm inside the cell's boundary.

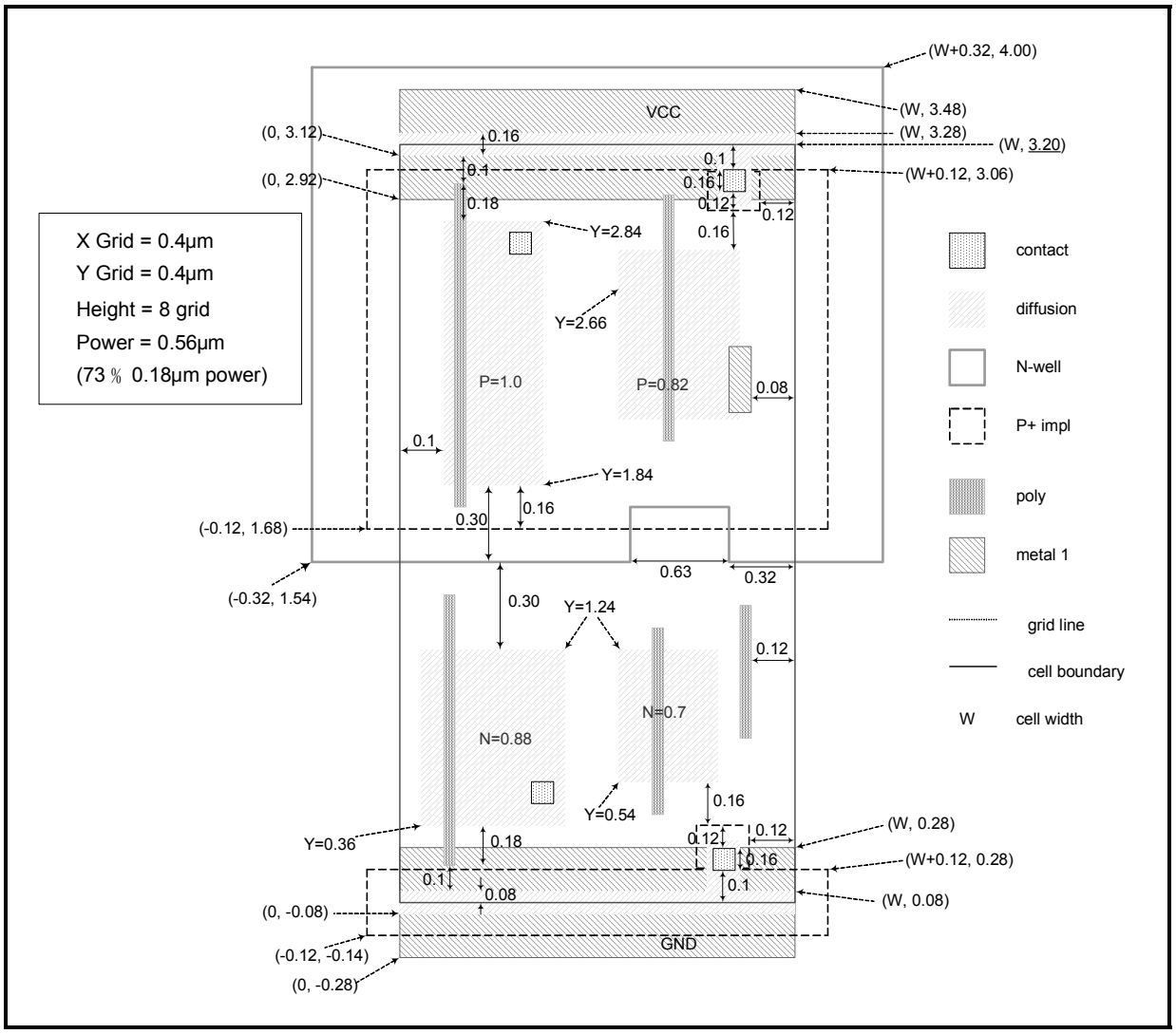


Figure 1. Cell structure

2.3. I/O cells layout rules

Table 4. I/O cells layout rules

Items	Parameters / examples	Description
Version A cell height	218.40µm	Version A IO cell height.
Version B cell height	152.00µm	Version B IO cell height.
Pin text	m8text	• The pin text is used to connect the pin to the bonding pad. • The layer name used for the pin text is "m8text". (see Note 1)
Power rails text	• m4text • m5text • m6text • m7text • m8text	Each power rail's text, depends on which metal layer the object touches. (see Note 1)
I/O pins	• metal1	• This pin text is used to connect the pin to the core. • The layer name used for the pin text is "m1text". • The layer name used to define the area of a port is "portarea-metal1". • The width of the port area should be 1.2um. • The height of the port area should be 0.4um.
Antenna diode	0.32µm * 0.32µm	• Each input pin, in each I/O cell, has an antenna diode. • 0.32µm * 0.32µm, is the diffusion size for each antenna diode.

3. General placement and routing (P&R) rules

This section will provide the basic placement and routing information and clock tree generation rules for using FSC0G_D 0.13µm standard performance standard cell library.

3.1. Basic rules

The basic rules include:

- Routing grids
- Power / ground names
- Mapping tables
- Power / ground pad definitions
- P&R environment

3.1.1. Routing grid

The pre-defined routing grid for each metal layer is shown below:

Table 5. Routing grid

Metals	Width
• metal1 • metal3 • metal5	0.4µm 0.4µm 0.4µm
• metal2 • metal4 • metal6	0.4µm 0.4µm 0.4µm
metal7, metal8 (or thick metal)	0.8µm

3.1.2. Power and ground naming rules

The following names must be used when assigning the power and ground names:

- VCC => power name
- GND => ground name

3.1.3. Mapping tables for layout stream in & out:

The UMC 0.13um process supports more process options offerings. Therefore, it is crucial to understand the required environment setup for your selected process option. In this section, typical stream in/out flows will be described for successful P&R data base integration.

3.1.3.1. Available process options

The list below is the eight (8) process options that can be used in your design. Please make certain that exactly one of these options matches the process specification for your design.

- 8-metal-2-thick
- 6-metal-2-thick
- 5-metal-1-thick
- 7-metal-2-thick
- 6-metal-1-thick
- 5-metal-0-thick
- 7-metal-1-thick
- 6-metal-0-thick

3.1.3.2. Via naming rules

In order to support all available UMC process options in Faraday 0.13µm library, new via naming rules have been adopted. For a specific process option selected, users need to convert via names back to UMC convention for tape-out using a stream out table from Table 7 or Table 9. Following is a list of available process options along with valid via names being applied. Note that A type vias like via4a and via5a are 1X vias, while B type vias like via4b, via5b, via6b, and via7b are 2X vias.

Table 6. Via naming rules for Faraday 0.13µm library

Default Layer: m1+via +m2+via2+m3+via3+m4								
Process	via4	m5	via5	m6	via6	m7	via7	m8
8m2t	via4a	m5	via5a	m6	via6b	**M7**	via7b	**M8**
7m2t	via4a	m5	via5b	**M6**	via6b	**M7**		
7m1t	via4a	m5	via5a	m6	via6b	**M7**		
6m2t	via4b	**M5**	via5b	**M6**				
6m1t	via4a	m5	via5b	**M6**				
6m0t	via4a	m5	via5a	m6				
5m1t	via4b	**M5**						
5m0t	via4a	m5						

3.1.3.3. Cadence DFII environment:

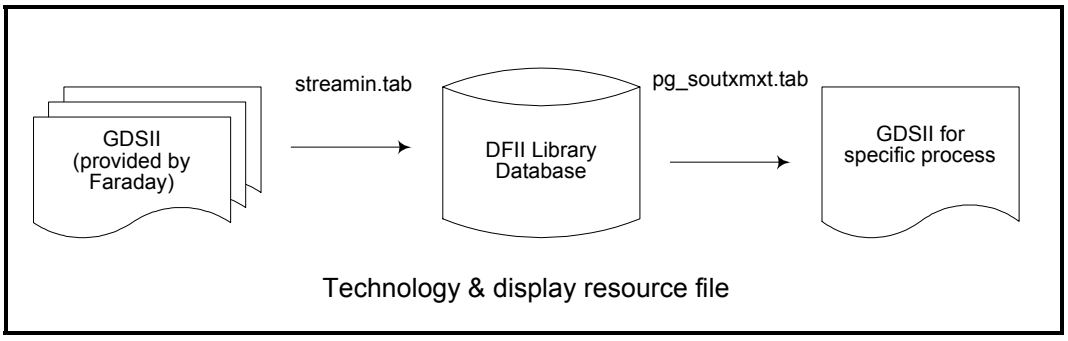
Faraday provides the needed stream-out tables for Cadence's DFII environment. Table 7 is a complete list of layer mapping table options that you can use for streaming out of your design. Please choose the layer-mapping table that matches your design's target process.

Table 7. Stream-out layer-mapping tables for DFII

Target process	Layer mapping table
8-metal-2-thick process	pg_sout8m2t.tab
7-metal-2-thick process	pg_sout7m2t.tab
7-metal-1-thick process	pg_sout7m1t.tab
6-metal-2-thick process	pg_sout6m2t.tab
6-metal-1-thick process	pg_sout6m1t.tab
6-metal-0-thick process	pg_sout6m0t.tab
5-metal-1-thick process	pg_sout5m1t.tab
5-metal-0-thick process	pg_sout5m0t.tab

Notes:

1. If you want to use Faraday's original design layers for all supported layout options, please use the mapping table "streamin.tab". This will allow you to use your own mapping tables, instead of the mapping tables listed in the Table above.
2. Faraday suggests the following flow for Cadence DFII environment:



3.1.3.4. Synopsys Milkyway environment:

For Synopsys Milkyway environment, following stream-in/out tables are provided.

Table 8. Stream-in technology files for Milkyway

Target process	Technology file
8-metal-2-thick process	umc_013_1p8m2t_mk_tlu.tf
7-metal-2-thick process	umc_013_1p7m2t_mk_tlu.tf
7-metal-1-thick process	umc_013_1p7m1t_mk_tlu.tf
6-metal-2-thick process	umc_013_1p6m2t_mk_tlu.tf
6-metal-1-thick process	umc_013_1p6m1t_mk_tlu.tf
6-metal-0-thick process	umc_013_1p6m0t_mk_tlu.tf
5-metal-1-thick process	umc_013_1p5m1t_mk_tlu.tf
5-metal-0-thick process	umc_013_1p5m0t_mk_tlu.tf

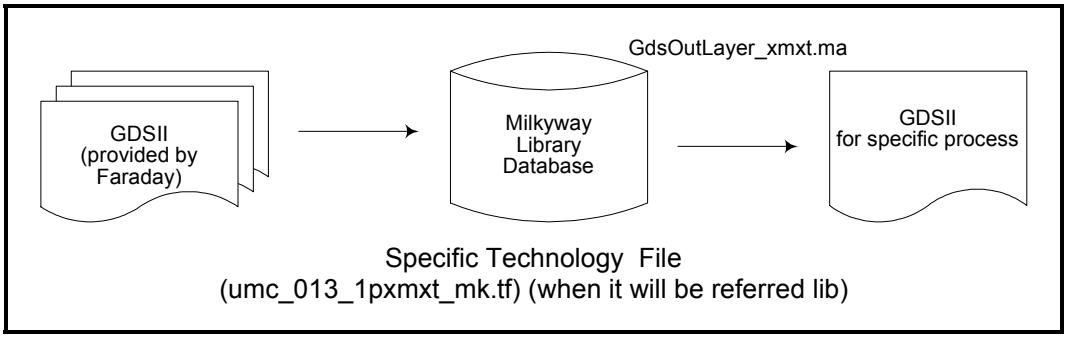
Notes:

1. After P&R, please choose the following layer-mapping table that matches your target process during the stream out phase in Synopsys Milkyway environment.

Table 9. Stream-out layer-mapping table lists Milkyway

Target process	Layer mapping table
8-metal-2-thick process	gdsOutLayer_1p8m2t.map
7-metal-2-thick process	gdsOutLayer_1p7m2t.map
7-metal-1-thick process	gdsOutLayer_1p7m1t.map
6-metal-2-thick process	gdsOutLayer_1p6m2t.map
6-metal-1-thick process	gdsOutLayer_1p6m1t.map
6-metal-0-thick process	gdsOutLayer_1p6m0t.map
5-metal-1-thick process	gdsOutLayer_1p5m1t.map
5-metal-0-thick process	gdsOutLayer_1p5m0t.map

2. Faraday suggests the follwing flow for Synopsys Milkyway environment:



3.1.4. Power / ground pad definitions:

Faraday provides two types of power/ground pads suitable for pad-limited and core-limited designs:

Table 10. Pad definitions for version A (pad-limited):

Cell names	Text labels	Descriptions
GND3IGA	GND	GND pad for 3.3V input driver / output
GNDKGA	GND	GND pad for internal cells
GNDOGA	GND	GND pad for all output buffer and input ESD protection
VCCKGA	VCC	VCC power pad for internal cells and 1.2V input
VCC3IGA	VCC3V	VCC power pad for 3.3V input receiver
VCC3OGA	VCC3V	VCC power pad for 3.3V output buffer

Table 11. Pad definitions for version B (core-limited):

Cell names	Text labels	Descriptions
GND3IGB	GND	GND pad for 3.3V input driver / output
GNDKGB	GND	GND pad for internal cells
GNDOGB	GND	GND pad for all output buffer and input ESD protection
VCCKGB	VCC	VCC power pad for internal cells and 1.2V input
VCC3IGB	VCC3V	VCC power pad for 3.3V input receiver
VCC3OGB	VCC3V	VCC power pad for 3.3V output buffer

3.1.5. P&R environment:

Faraday provides the environment for Cadence and Synopsys place and route tools. Currently, LEF header and technology file are provided respectively for Cadence and Synopsys tools in each UMC process option.

3.1.5.1. Cadence place and route tool environment:

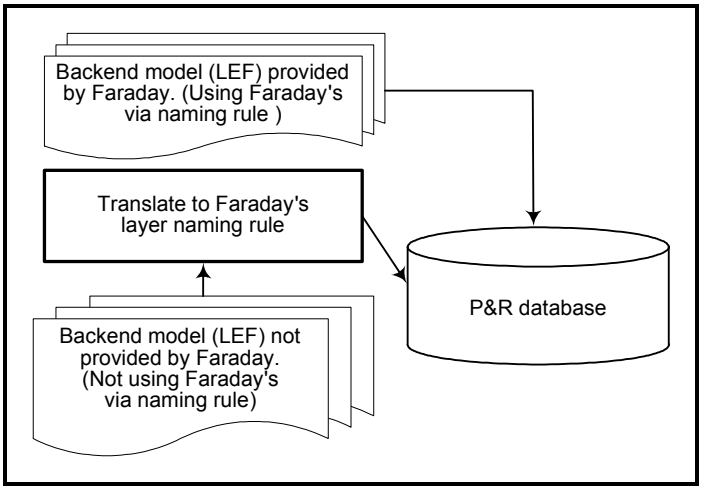
To input LEF files to Silicon Ensemble / First Encounter environment, please use one of the LEF header files listed in the Table below. Please ensure that the LEF-in environment you choose matches your target process.

Table 12. Available LEF headers for Silicon Ensemble / First Encounter:

Target process	SE / FE LEF header file
8-metal-2-thick process	header8m2t.lef
7-metal-2-thick process	header7m2t.lef
7-metal-1-thick process	header7m1t.lef
6-metal-2-thick process	header6m2t.lef
6-metal-1-thick process	header6m1t.lef
6-metal-0-thick process	header6m0t.lef
5-metal-1-thick process	header5m1t.lef
5-metal-0-thick process	header5m0t.lef

Notes:

1. All the back end model (LEF files), environment files, and GDSII files delivered by Faraday follow Faraday's via naming rule described in 3.1.3.2. If you plan to use Faraday's backend or environment to implement your chip design, all backend model /library used must follow Faraday's layer naming rule. Please refere to the following graph for more details.



3.1.5.2. Synopsys place and route environment:

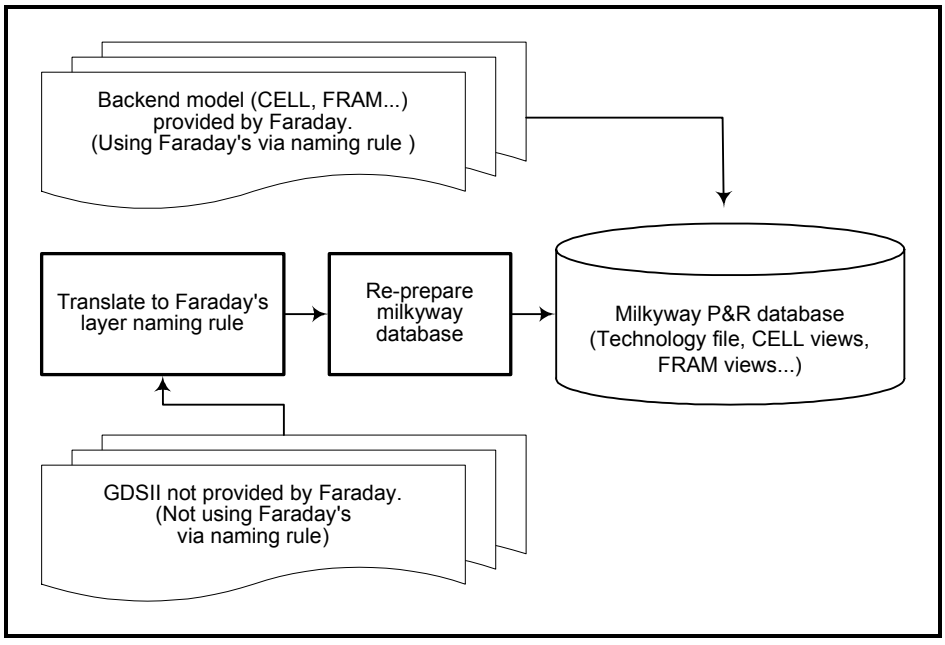
To create an Apollo / Astro environment, please use one of the technology files listed in the Table below. Please make sure that the Apollo / Astro environment you choose matches your target process.

Table 13. Available technology files for Apollo / Astro:

Target processes	Apollo / Astro technology files
8-metal-2-thick process	umc_013_1p8m2t_mk.tf
7-metal-2-thick process	umc_013_1p7m2t_mk.tf
7-metal-1-thick process	umc_013_1p7m1t_mk.tf
6-metal-2-thick process	umc_013_1p6m2t_mk.tf
6-metal-1-thick process	umc_013_1p6m1t_mk.tf
6-metal-0-thick process	umc_013_1p6m0t_mk.tf
5-metal-1-thick process	umc_013_1p5m1t_mk.tf
5-metal-0-thick process	umc_013_1p5m0t_mk.tf

Notes:

1. All the back end model (CELL and FRAM views), environment files, and GDSII files delivered by Faraday follow the Faraday's via naming rule described in 3.1.3.2. If you plan to use Faraday's technology file to implement your chip design, you must translate your own GDSII files by following Faraday's layer naming rule and re-prepare the CELL and FRAM views. Please refer to the followng graph for more details.



3.2. Placement rules

Faraday provides filler cells, empty cells, pad cells, and corner cells for you to use when you are placing your cells.

3.2.1. Filler cell for core cell:

Table 14 The filler cell list for core cell

Cell names	Descriptions
FILLER1GD	Does not include sub / well contact for one (1) grid
FILLER2GD	Includes sub / well contact for two (2) grids
FILLER3GD	Includes sub / well contact and decoupling capacitance for three (3) grids
FILLER4EGD	Includes sub / well contact and decoupling capacitance for four (4) grids
FILLER8EGD	Includes sub / well contact and decoupling capacitance for eight (8) grids
FILLER16EGD	Includes sub / well contact and decoupling capacitance for sixteen (16) grids
FILLER32EGD	Includes sub / well contact and decoupling capacitance for thirty-two (32) grids
FILLER64EGD	Includes sub / well contact and decoupling capacitance for sixty-four (64) grids

3.2.2. Filler cell for I/O cells:

Table 15. The filler cell list for Version A (pad limits):

Cell names	Descriptions
EMPTY1GA	For one (1) grid • This overlapped filler can only be used in Apollo environments.
EMPTY2GA	For two (2) grids
EMPTY4GA	For four (4) grids
EMPTY8GA	For eight (8) grids
EMPTY16GA	For sixteen (16) grids

Table 16. The filler cell list for Version B (core limits):

Cell names	Descriptions
EMPTY1GB	For one (1) grid • This overlapped filler can only be used in Apollo environments.
EMPTY2GB	For two (2) grids
EMPTY4GB	For four (4) grids
EMPTY8GB	For eight (8) grids
EMPTY16GB	For sixteen (16) grids

3.2.3. Bonding pad

The bonding pad is not included in the I/O cell. The pad placement and routing should be added in during the design flow.

Table 17. The cell list for bonding pad:

Target processes	Cell names
8-metal-2-thick process	PAD8MG
7-metal-2-thick process	PAD7MG
7-metal-1-thick process	PAD7MG
6-metal-2-thick process	PAD6MG
6-metal-1-thick process	PAD6MG
6-metal-0-thick process	PAD6MG
5-metal-1-thick process	PAD5MG
5-metal-0-thick process	PAD5MG

3.2.4. Corner cells:

- Version A (pad-limited):
  - CORNERGA
- Version B (core-limited):
  - CORNERGB
- Version A and B mixed:
  - CORNERGAB

3.2.5. Cell flipping (up / down) is allowed when row abutment is needed

This library provides maximum flexibility for either row separation or row abutment. This flexibility allows users to minimize the chip area or to achieve better noise immunity. In general, there are three (3) butting types: PP, NN, and PN. The Figure below illustrates row abutment.

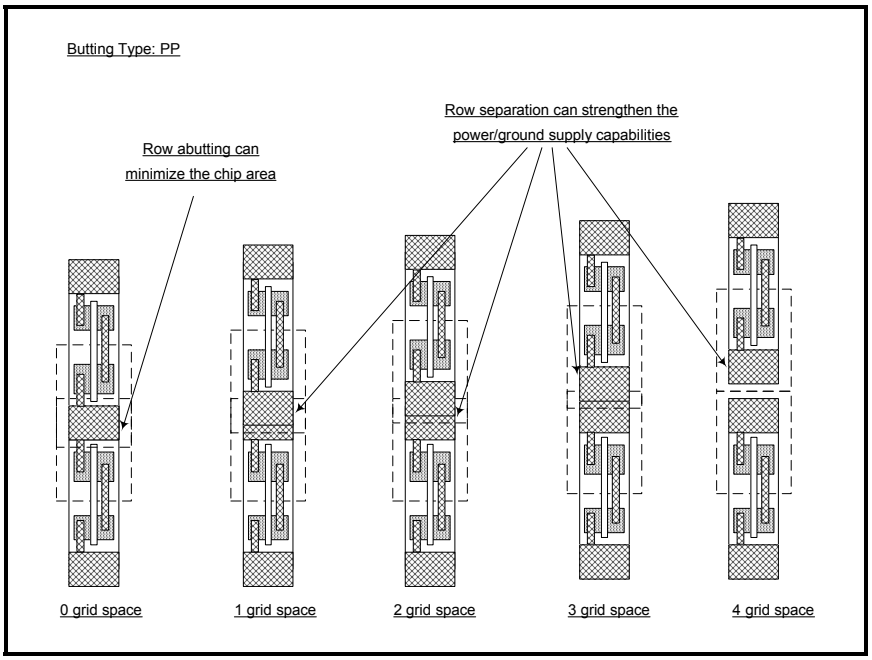


Figure 2. Three (3) butting types

The following tables (Table 18 and Table 19) provide the row-to-row spacing rules:

Table 18. Core cells row abutment - without dummy_block / slot_block layers (default)

Butting type	Grid space (grids)						
	0	1	2	3	4	5	> = 6
PP	O	X	O	O	O	X	O
NN	O	X	O	O	O	O	O
PN	X	X	X	O	O	O	O

Note:

By default, all FSC0G_D core cells are without dummy_block / slot_block layers.

Table 19. Core cells row abutment - with dummy_block / slot_block layers

Butting types	Grid spaces (grids)						
	0	1	2	3	4	5	>= 6
PP	O	X	O	O	O	X	O
NN	O	X	O	O	O	O	O
PN	X	X	X	O	O	O	O

Notes:

1. This table means users can add dummy_block layers and slot block layers for special reasons.
2. For more information about dummy_block and slot_block layers, please refer to UMC's "0.13μm, 1.2V / 3.3V, 1P8M, fusion logic process mask tooling information".

Dummy reminders:

1. If you add dummy_block layers, UMC will not add dummy metals.
2. If you add slot_block layers, UMC will not add slots.
3. Either case may cause a change in your design's electrical characteristics.

Optimization reminders:

1. To increase your routing channels and strengthen your power and ground supply capabilities:
   - Separate the row space.
2. You can minimize your chip area by abutting the power rails and ground rails.

3.3. Routing rule

UMC's 0.13µm logic process has special rule that was not implemented in previous UMC processes. This rule is as follows:

1. When a small net connects to a big wire, double-cut vias must be used (Figure 3).
2. A via-density check, called VIAFARM density check, must be applied to the Mvia-x array connecting Metal-x and Metal-x+1(x=1,2,3,4,5,6,7) when both the width and length of the intersection area >= 5um. The VIAFARM density must meet the criteria of <= 30%.

Note :

Please refer to UMC's "Process Topologic Layout Rule", for more detailed information.

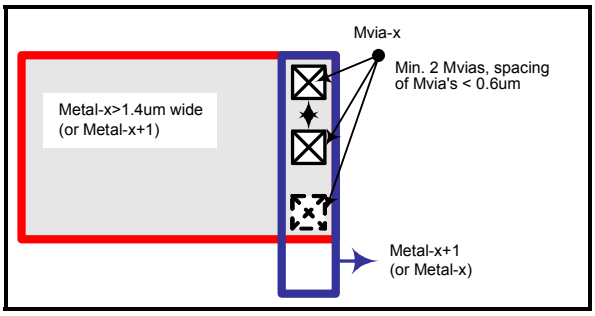


Figure 3. An example of double-cut vias for metal-x to metal-x+1 connection

3.3.1. Cadence silicon ensemble environment:

- Double via rule

  ➔ In LEF version LEF5.3

  This special rule cannot be defined in the P&R header file, because it is not currently supported in Cadence's Silicon Ensemble. For most of the cases, this special rule applies to nets that tie to either power or ground. A workable alternative solution is to use a non-default rule "TWOVIA", already defined in the header files provided by Faraday, to implement this special rule. Before warp routing or final routing, please add the following command to your command line:

  - change net "netName" rule.name TWOVIA ;
    Where netName is the net name that needs double-cut vias.

  For example:

  - change net "VCC" rule.name TWOVIA ;

  ➔ In and after LEF version 5.4

  The rule was described in LEF header already, user do not need to use any additional commands when P&R.

- VIAFARM rule

  Even convert LEF version 5.5 has no support for this rule.

3.3.2. Synopsys Apollo / Astro environment:

- Double via rule

  A simple and practical solution to increase the probability of continuity through a via is to perform the "via doubling". Via doubling is a Scheme function in Apollo and Astro. The command syntax to implement "via doubling" is as follows:

  Command Syntax:

  axSetIntParam "droute" "noOffsetFatVia" 0/1

  where

  0: fat-via can overlap with fat preroute or pin with any offset.

  1: fat-via has to completely inside fat preroute or pin

- VIAFARM rule

  Two commands have been added to Apollo and Astro to change via density in a via array. They are axSetContactArrayViaFarm and axResetContactArrayViaFarm.

  Command Syntax:

  1) axSetContactArrayViaFarm cellId contactName xMin yMin xArrNum yArrNum xInterval yInterval

     This command will convert a contact array to a via farm.

     For example,

     axSetContactArrayViaFarm (geGetEditCell ( )) "WVIA1HORZ" 5 5 4 4 3 3

     It will convert all contact arrays which are named "WVIA1HORZ" and have x-dir and y-dir min duplication of 5, to via farms, for which the array is 4x4, the x-dir interval is 3, and the y-dir interval is 3.

  2) axResetContactArrayViaFarm cellId contactName

     This command will reset contact arrays (which have been convered to via farms) to normal

     For example:

     axResetContactArrayViaFarm (geGetEditCell()) "WVIA1HORZ"

     It will convert all via farms named "WVIA1HORZ" to contact arrays.

  Note:

  This should be available in patch 9 of Apollo and patch 3 of Astro

3.3.3. Clock tree generation rules

Please choose the clock tree synthesis cell that is best suited to your environment.

Table 20. The cell list for clock tree synthesis:

Cell names	Descriptions
BUFCKEGD	Clock tree buffer X1
BUFCKGGD	Clock tree buffer X1.6
BUFCKHGD	Clock tree buffer X2
BUFCKIGD	Clock tree buffer X2.5
BUFCKJGD	Clock tree buffer X3
BUFCKKGD	Clock tree buffer X4
BUFCKLGD	Clock tree buffer X5
BUFCKMGD	Clock tree buffer X6
BUFCKNGD	Clock tree buffer X8
BUFCKQGD	Clock tree buffer X20
INVCKDGD	Clock tree inverter X1
INVCKGGD	Clock tree inverter X1.6
INVCKHGD	Clock tree inverter X2
INVCKIGD	Clock tree inverter X2.5
INVCKJGD	Clock tree inverter X3
INVCKKGD	Clock tree inverter X4
INVCKLGD	Clock tree inverter X5
INVCKMGD	Clock tree inverter X6
INVCKNGD	Clock tree inverter X8
INVCKQGD	Clock tree inverter X20