

Table 1: Testing Environment

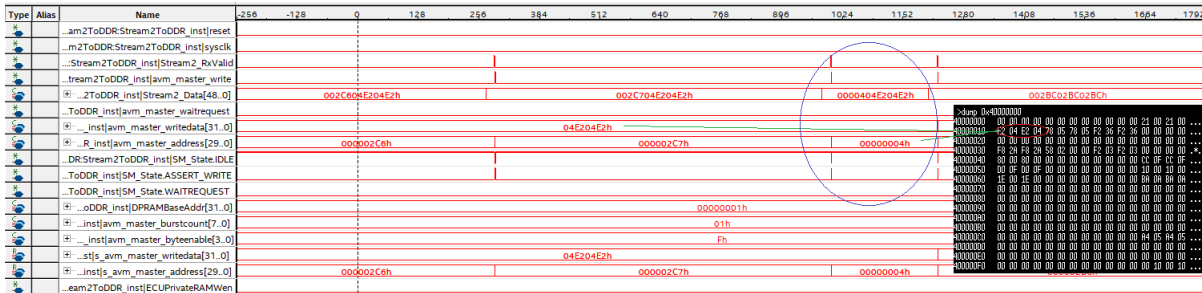


Figure 1: Correct writing DDR3 (position 04h – data inverted “04E204E2”)

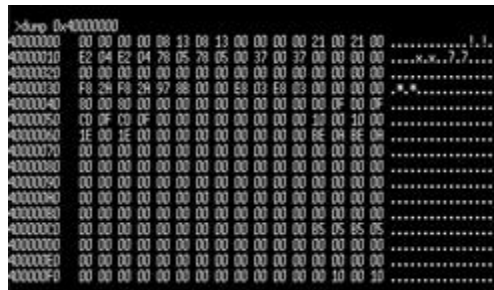


Figure 2: Correct data – Position 0/”00000000”, position 1/ inverted x”13D813D8”



Figure 3: Misalignment

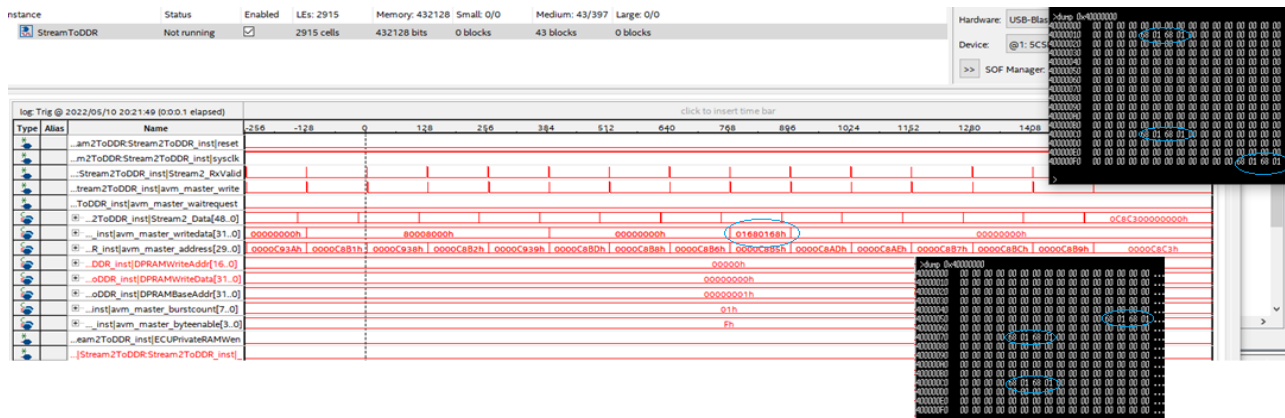


Figure 4: Frozen Data

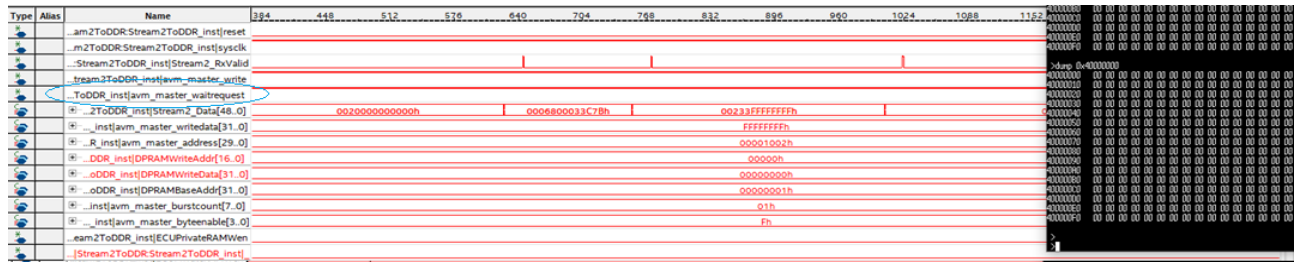


Figure 5: Zeros



Figure 6: SoC FPGA internal reset correction