INSTITUTO SUPERIOR TÉCNICO
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Fast ADC Static Testing

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Presentation Outline

- Introduction
- Static Specifications
- Static Characteristics
- Different Static Test Methods
- Ramp Vernier Static Test
- Conclusions

Introduction

- Static Testing is used to determine the ADC static characteristics
- Static characteristics quantify the behavior of an ADC with constant input signals
- It is important since 90% of ADCs are used with DC signals
- Quality of measurements made with ADC

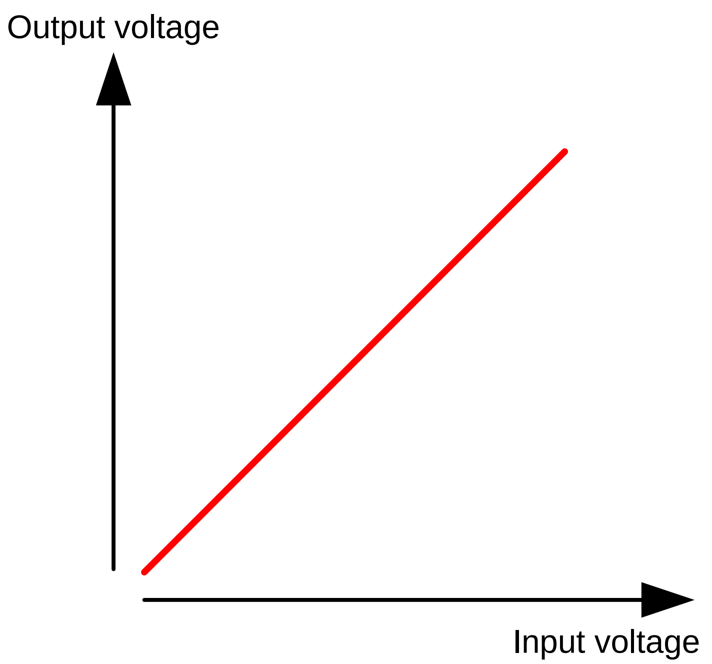
ADC Static Specifications

ADC Static Specifications

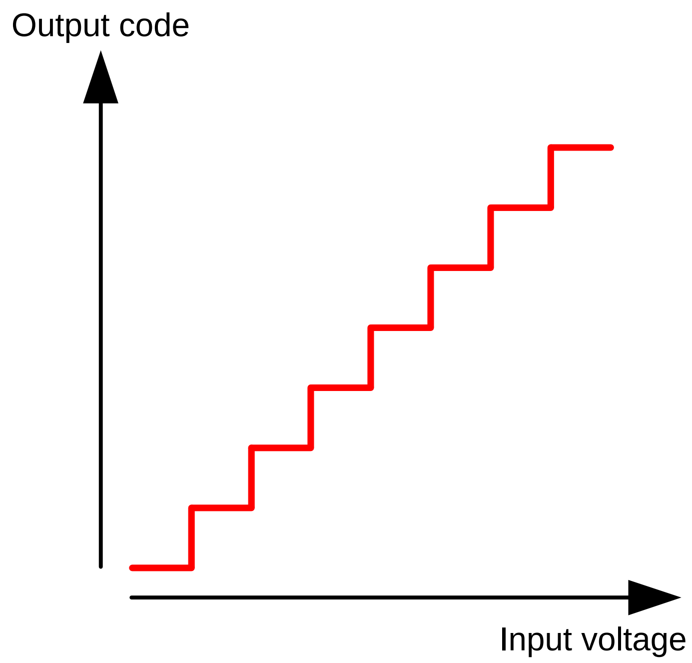
- Transfer Function
- Number of Bits
- Transition Voltages
- Code Bin Width
- Input Range
- Output Voltage

Transfer Function

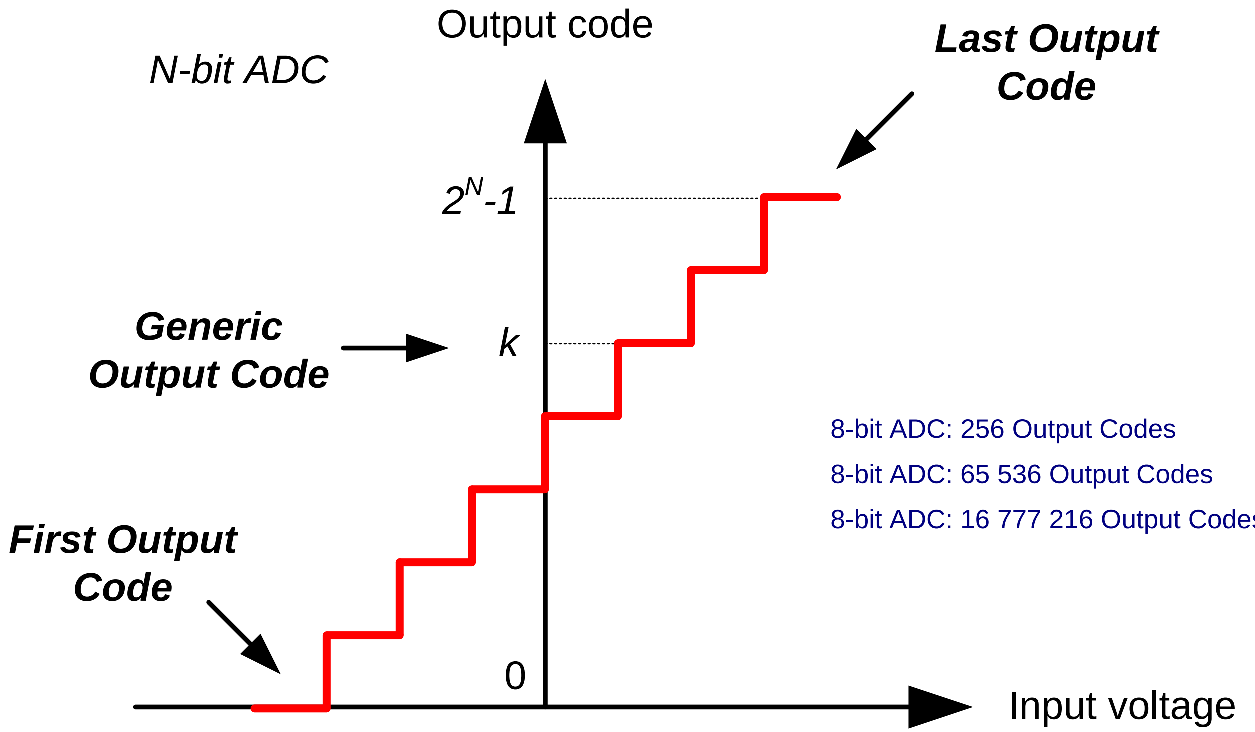
ANALOG CIRCUIT



ADC

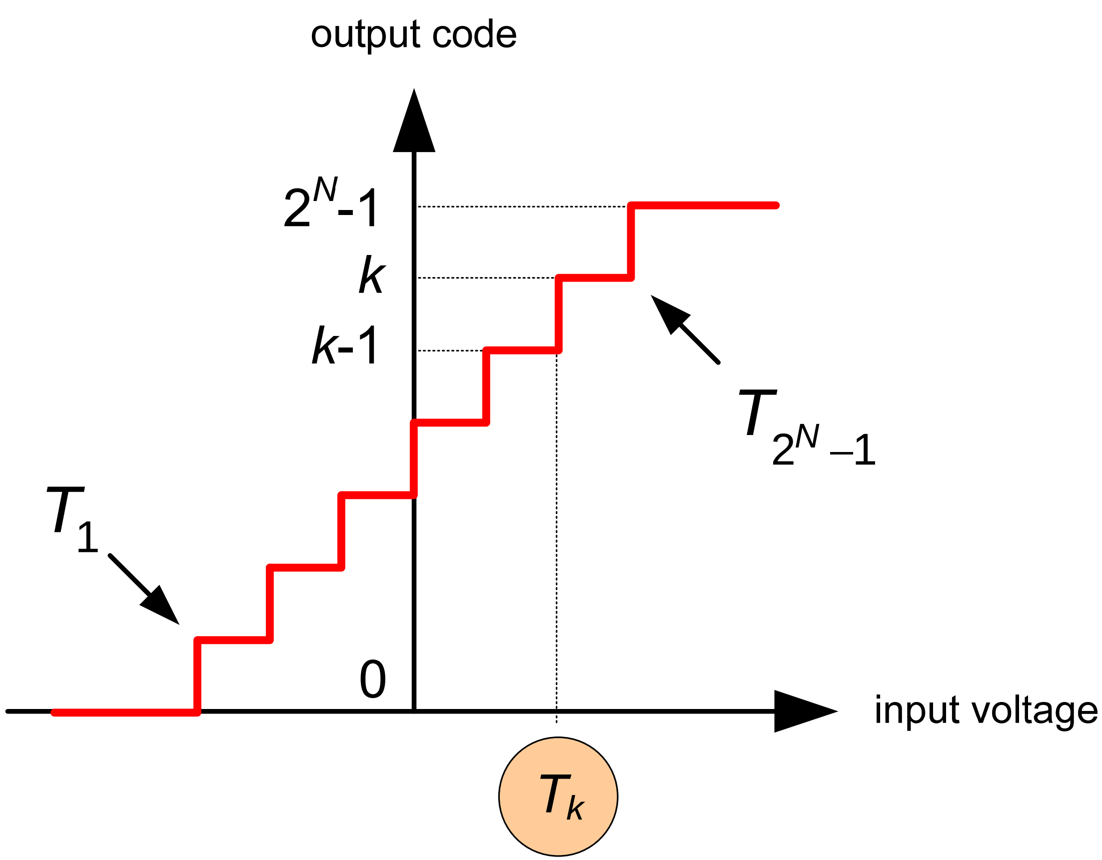


Number of Bits



8-bit ADC: 256 Output Codes
8-bit ADC: 65 536 Output Codes
8-bit ADC: 16 777 216 Output Codes

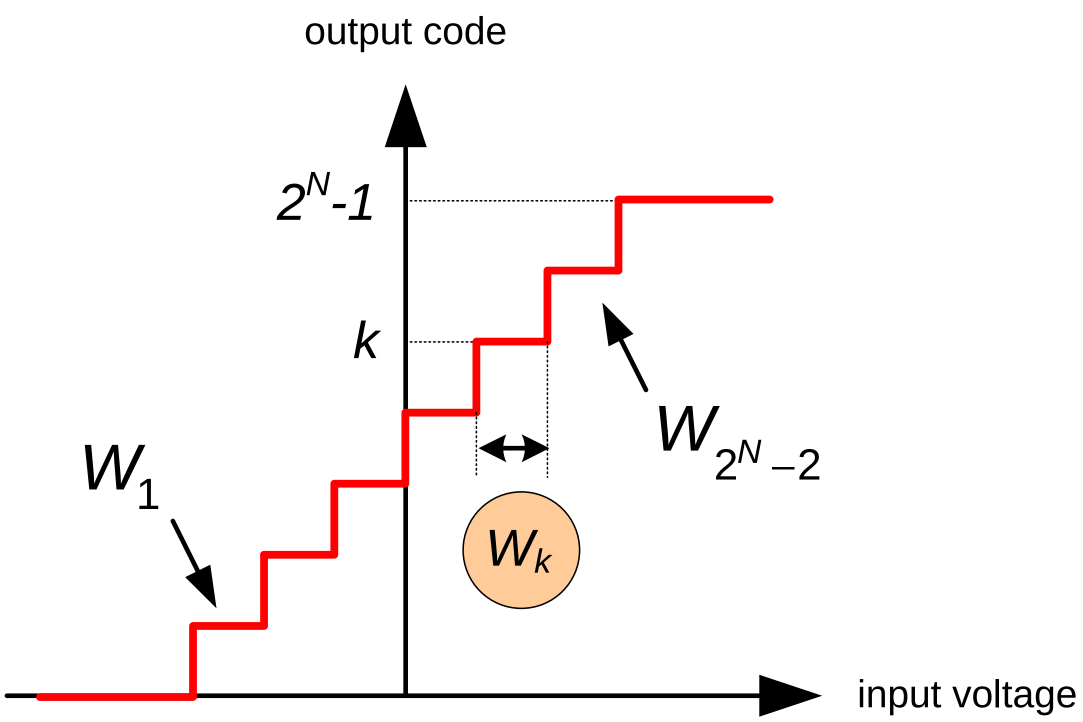
Transition Voltage



Transition Voltage

- *"**Transition Voltage k**: The value of the DC input signal that causes half the samples acquired to have output code k-1 or lower and the other half, output code k or higher"*

Code Bin Width



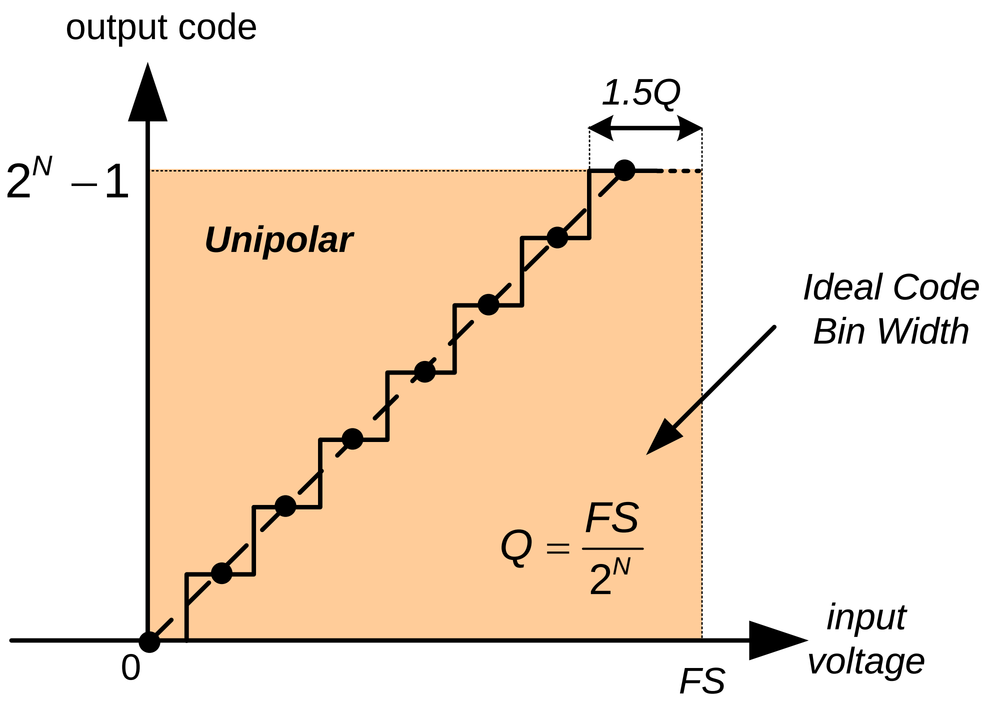
Code Bin Width

$$W_k = T_{k+1} - T_k$$

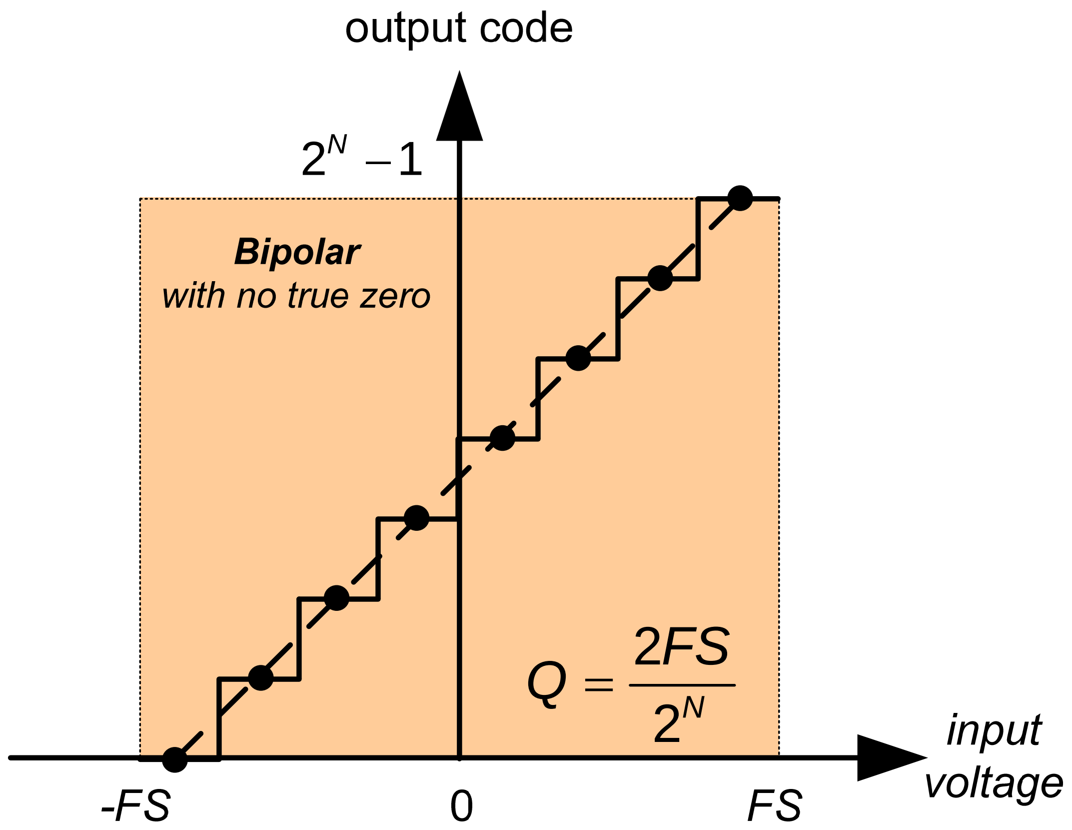
Input Range

- Unipolar
- Bipolar
  - With No True Zero (mid-riser)
  - With True Zero (mid-tread)

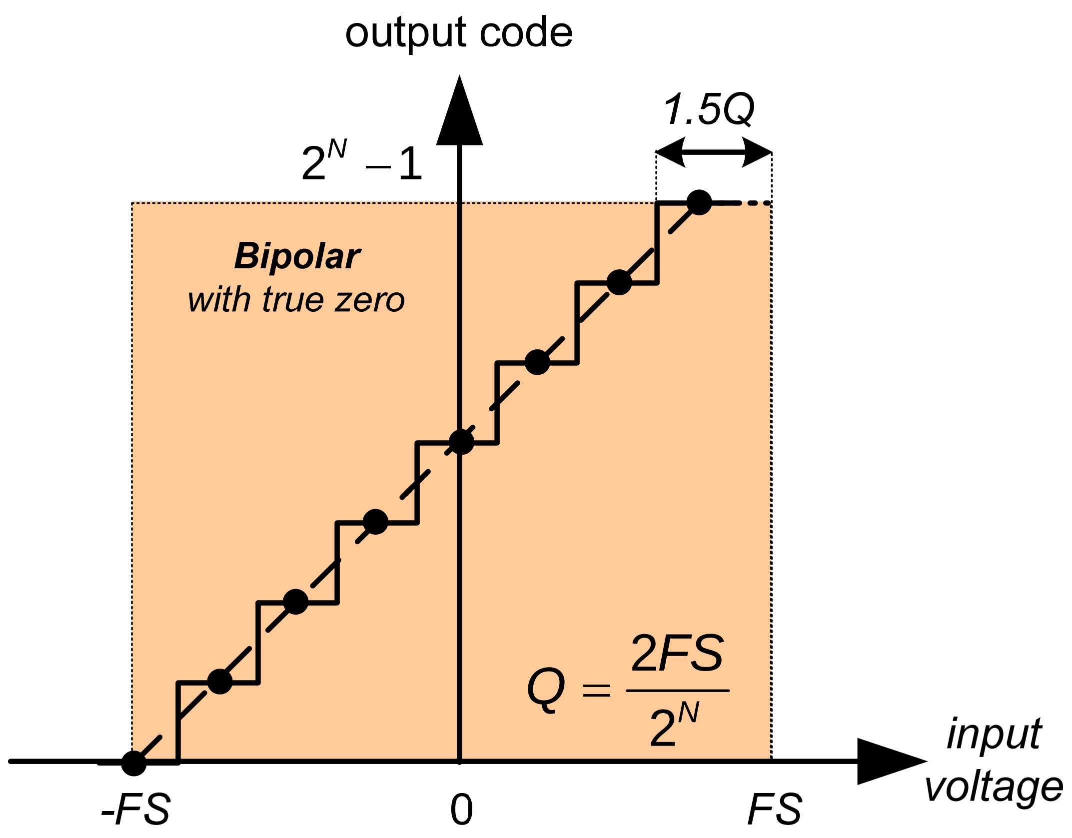
Unipolar Input Range



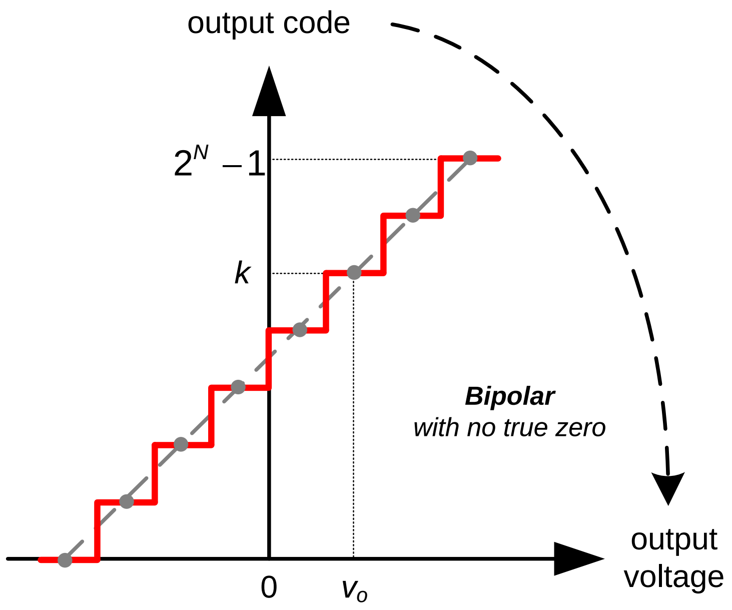
Bipolar Input Range



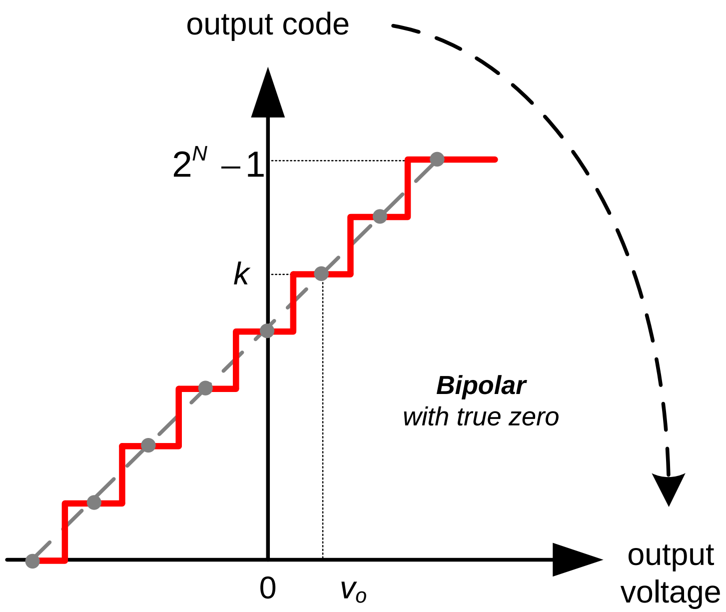
Bipolar Input Range



Output Voltage



$$v_o = -FS + \frac{Q}{2} + k \cdot Q$$



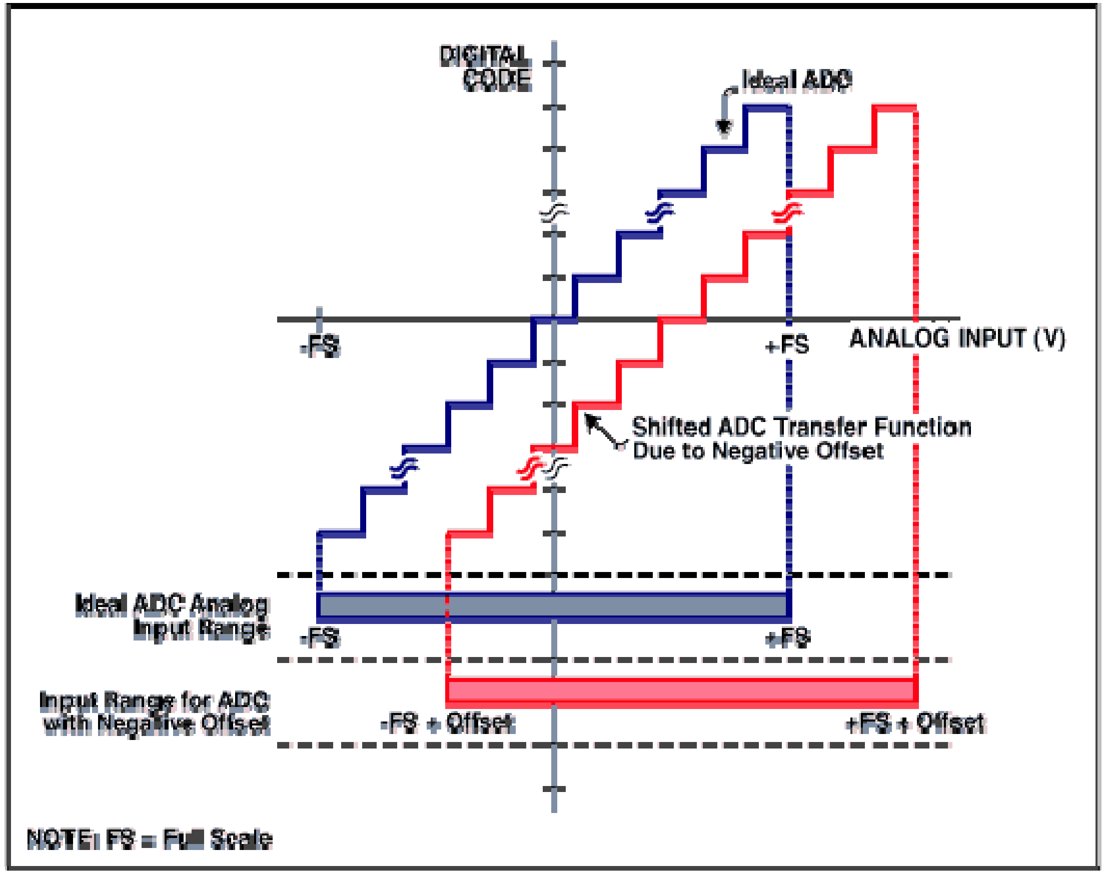
$$v_o = -FS + k \cdot Q$$

ADC Static Characteristics

ADC Static Characteristics

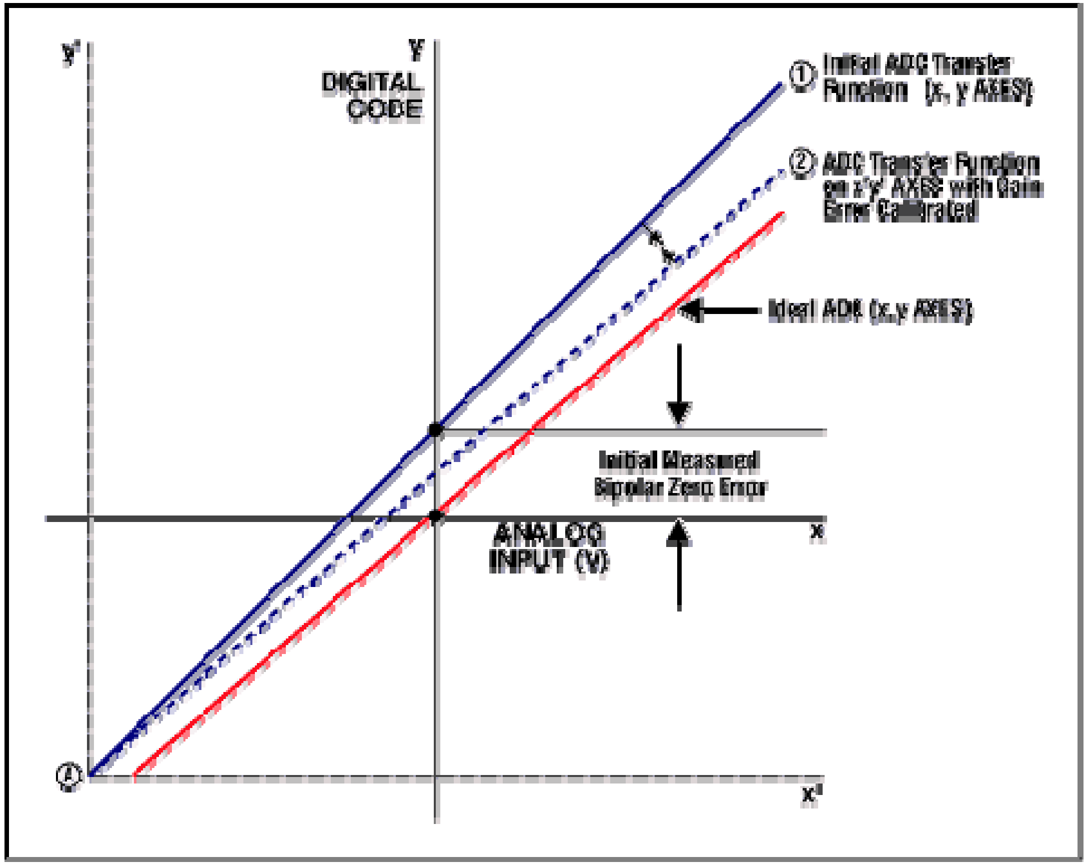
- Offset Error
- Gain Error
- Differential Nonlinearity
- Integral Nonlinearity
- Drift
- …

Offset Error

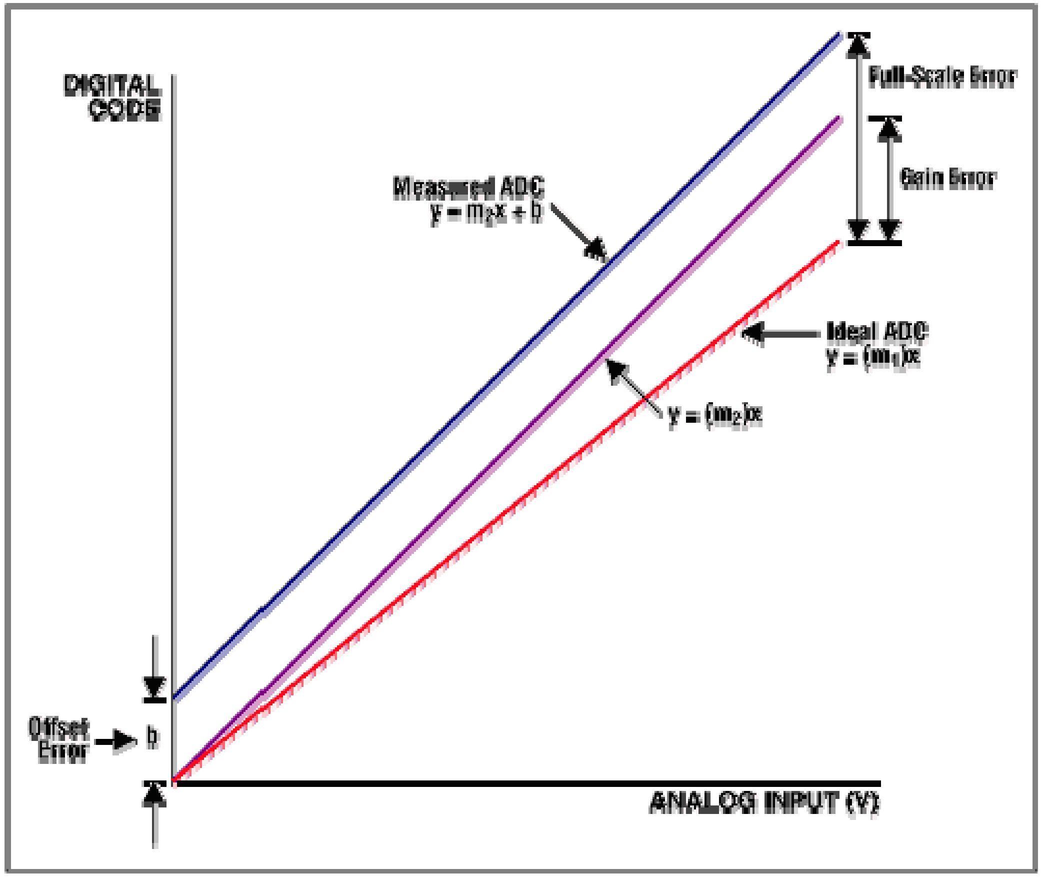


© Maxim

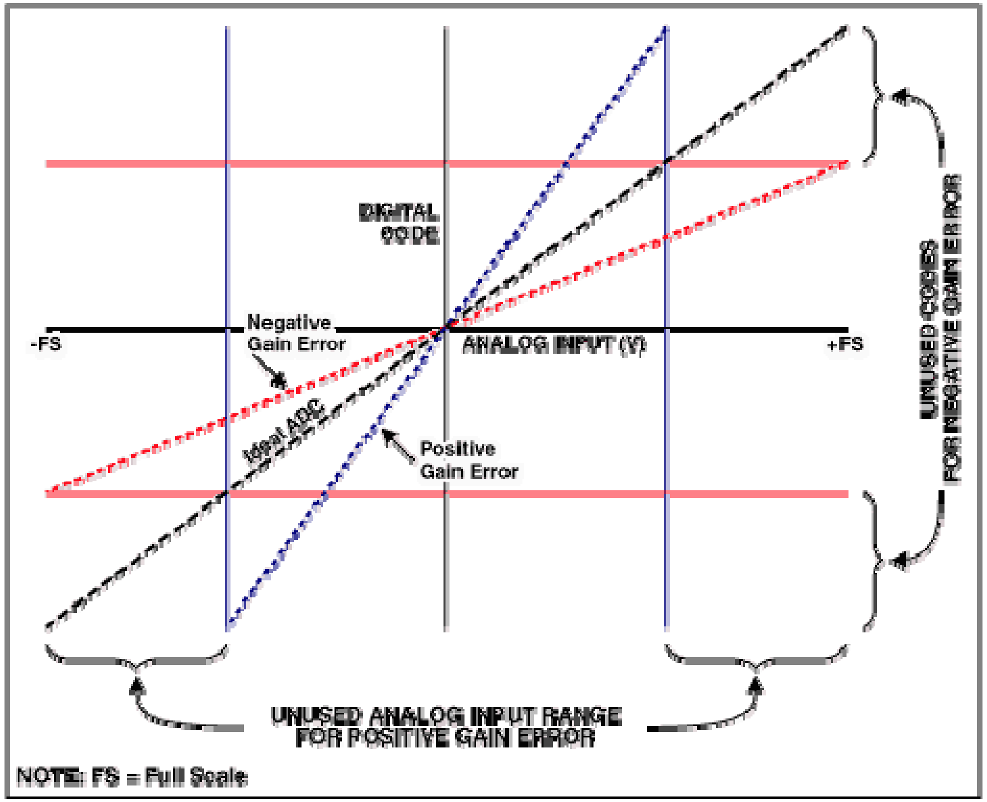
Gain Error


y'
y
DIGITAL
CODE
① Initial ADC Transfer
Function (x, y AXES)
② ADC Transfer Function
on x'y' AXES with Gain
Error Calibrated
Ideal ADC (x, y AXES)
Initial Measured
Bipolar Zero Error
ANALOG
INPUT (V)
x
A
x'

Full-scale Error



Gain Error Reduces Range



Definition

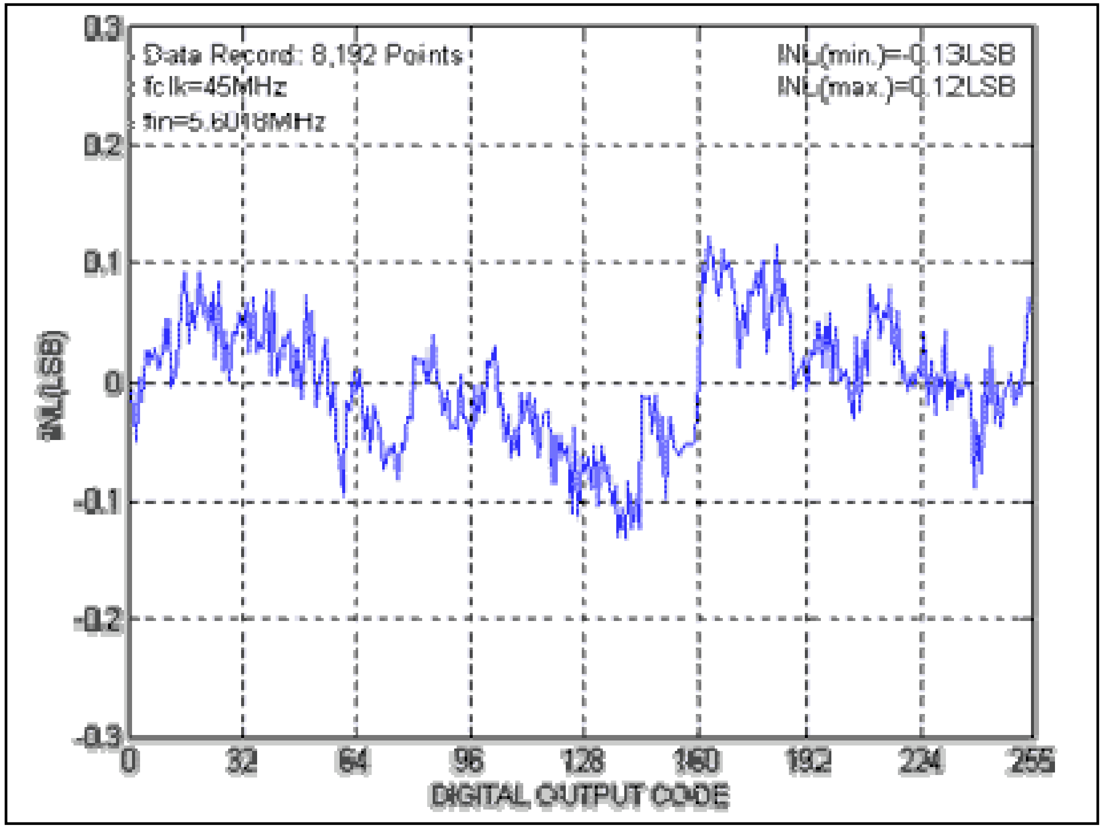
- ***Gain and Offset errors*** *are the values that the measured transition voltages must be multiplied by and then added to, in order to get the ideal transition voltages*

Integral Nonlinearity

- It is the difference between the real and the ideal Transition Voltages after Gain and Offset Error correction

$$INL_k = \frac{\left(G \cdot T_k + V_{os}\right) - T_k^{ideal}}{Q}$$

Integral Nonlinearity



Ideal Transition Voltages

$$T_k^{ideal} = -FS + k \cdot Q \quad , \quad k = 1 \ldots 2^N - 1$$

Bipolar with no true zero

$$T_k^{ideal} = -FS + \frac{Q}{2} + k \cdot Q \quad , \quad k = 1 \ldots 2^N - 1$$

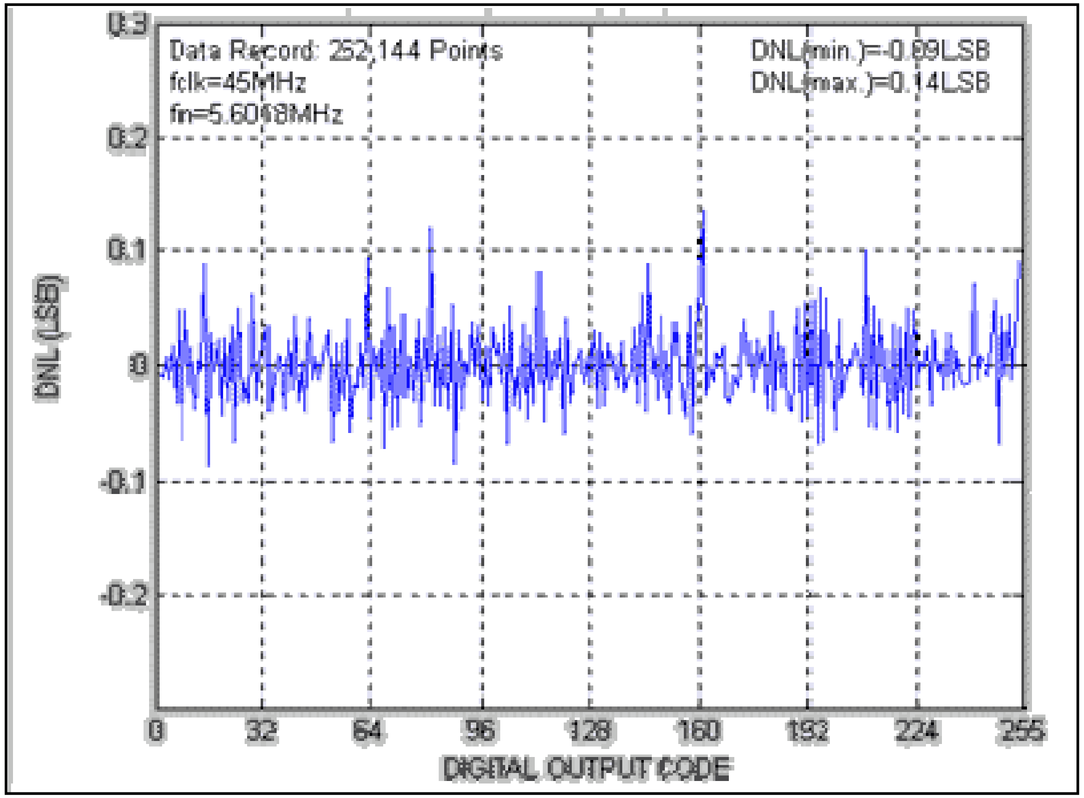
Bipolar with true zero

Differential Nonlinearity

- It is the difference between the real and the ideal Code Bin Widths after Gain correction

$$DNL_k = \frac{G \cdot W_k - Q}{Q}$$

Differential Nonlinearity



Different Static Test Methods

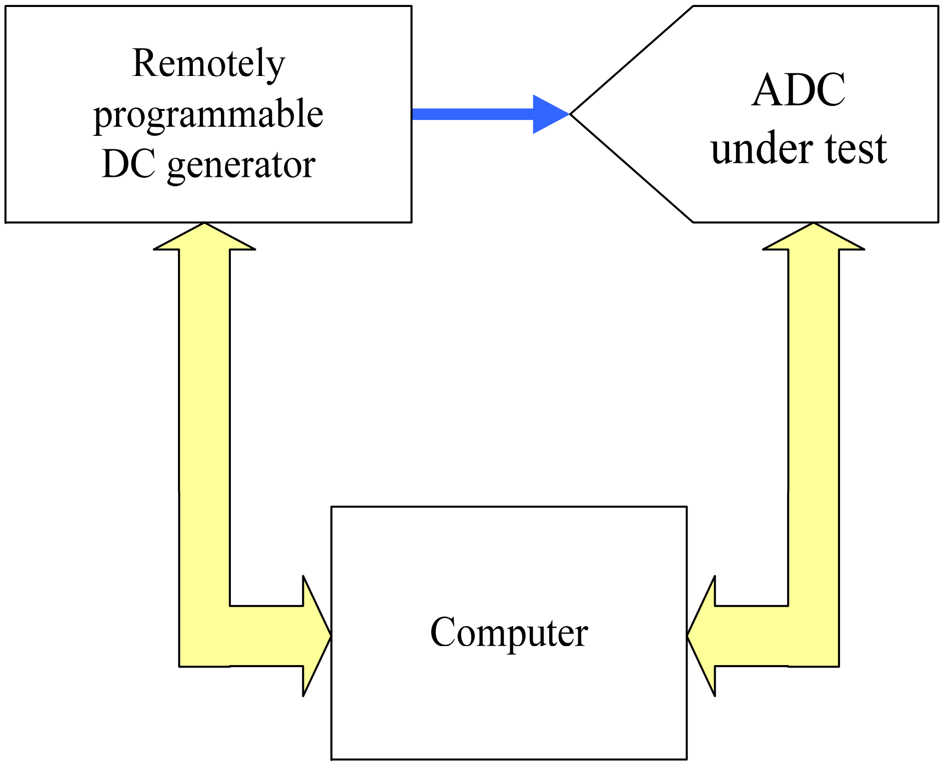
Different Static Test Methods

- Traditional Static Test Method
- Histogram Test Method

Traditional Static Test

- Apply a DC voltage to the ADC under test
- For each transition voltage *k*, search for the DC value that causes half of the output samples to have code *k* or lower
- The value of DC input found is, by definition, the transition voltage

Test Setup


Remotely programmable DC generator
ADC under test
Computer

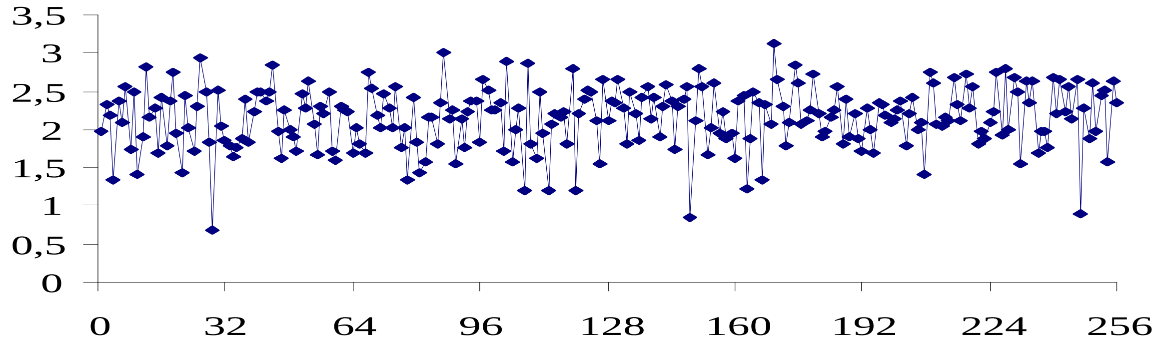
Procedure

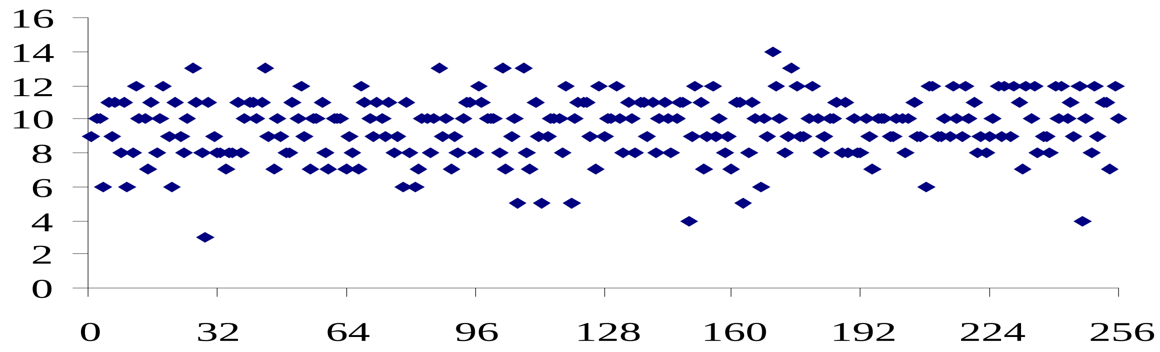
- Start with a DC voltage slightly lower then the ideal value of the first transition voltage.
- If the 50% condition is not met, increase the input voltage by the desired estimation accuracy (usually Q/4)

Procedure (cont)

- Repeat until the 50% condition is met.
- Interpolate between the values of the last 2 DC values used to get the transition voltage using the percentage of samples obtained.
- Repeat the procedure for the next transition voltage starting with the current DC voltage

Random Noise



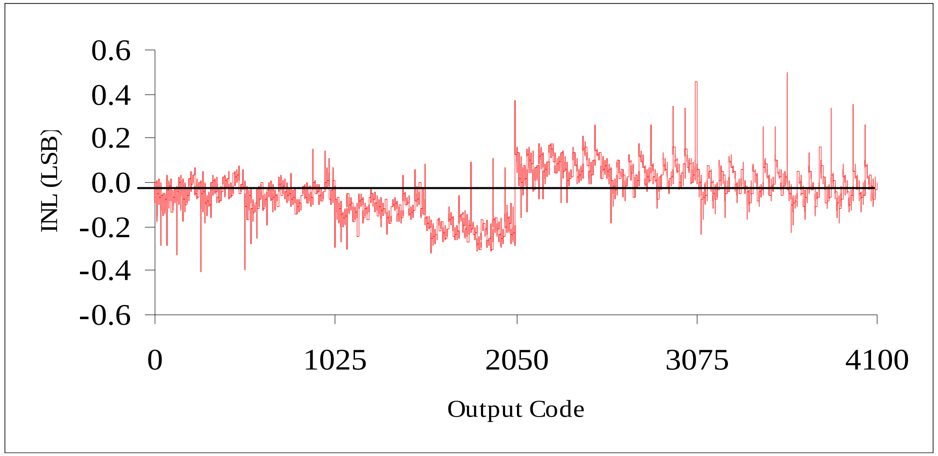


Estimation Uncertainty

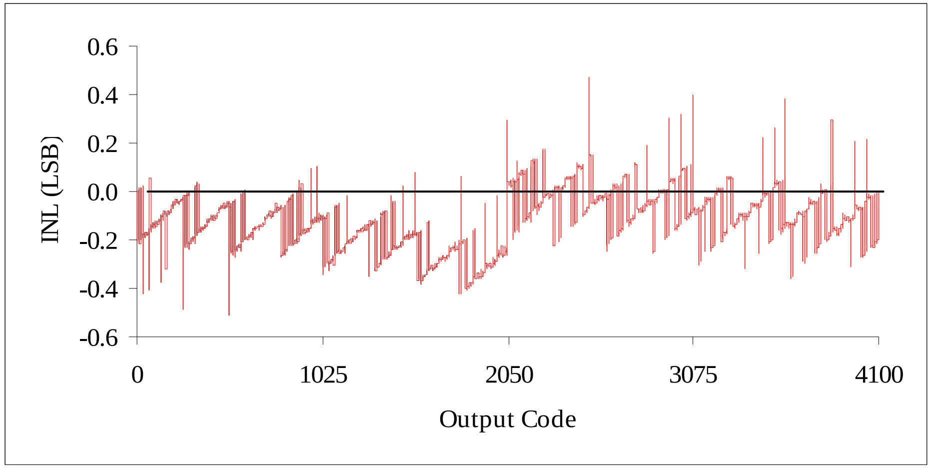
- The uncertainty can be reduced by increasing the number of acquired samples
- The table shows the measurement precision for a confidence level of 99.87%

Number of acquired samples(*M*)	64	256	1024	4096
Transition level measurement precision (% of noise standard deviation)	45%	23%	12%	6%

Effect of Resolution



Resolution
1/32 LSB



Resolution
1/4 LSB

Time Consuming!

- The **traditional static test** can be a very time consuming procedure especially for high resolution ADCs
  - 2^N-1 code transition levels must be found individually
  - the mean number of tries for each T_k is $Q/(2R)$
  - *M* samples must be taken after each DC voltage change
  - it is necessary to wait between changes in the input source at least for its settling time

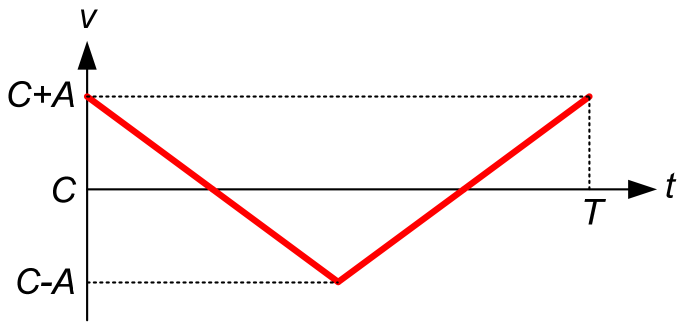
Example

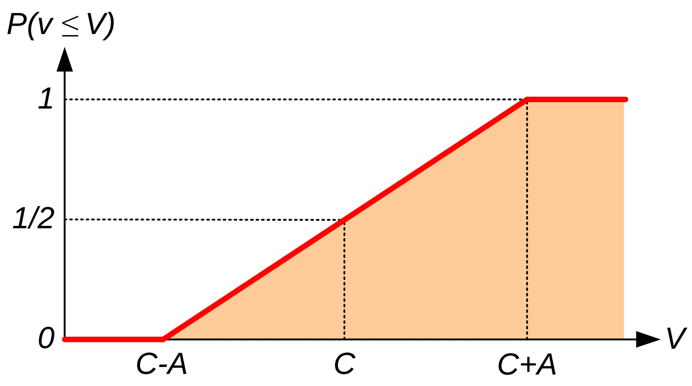
- Consider a 16-bit ADC, with R=Q/8, M = 1000, a source settling time of 100 ms and a sampling frequency of 10kHz
- The test will take 65535 x 4 x (0.1+1000 x 10^{-4}) s = **14,5 hours!**
- Even considering that the samples are transferred to the computer during the source settling time
- If the sampling frequency decreases to 1 kHz, or the source settling time increases to 1 s, the time duration will increase one order of magnitude!
- In any case is a prohibitive time interval. Of course that if a 12 bit converter was under test the duration would decrease 16 times.

Histogram Test

- Apply a low frequency triangular wave to the ADC input which spans its entire range
- Acquire a given number of samples *M*
- Make the Histogram: Compute the number of samples with each output code
- Compute the Cumulative Histogram *CH*
- Compare this with the expected value from an ideal ADC

Amplitude Distribution





$$v(t) = \begin{cases} C + A - 4A\dfrac{t}{T} & , \quad 0 \le t \le \dfrac{T}{2} \\ C - A + 4A\dfrac{t - T/2}{T} & , \quad \dfrac{T}{2} \le t \le T \end{cases}$$

$$P(v \le V) = \frac{V - C + A}{2A}$$

Estimate Transition Voltages

$$\frac{CH_{k-1}}{M} \xrightarrow[M\to\infty]{} P\left(v \le T_k\right)$$

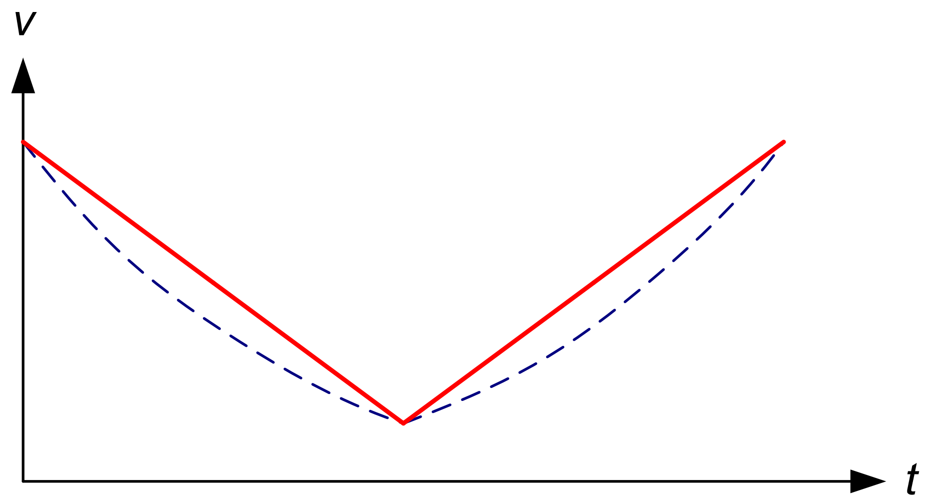
$$\frac{CH_{k-1}}{M} \xrightarrow[M\to\infty]{} \frac{T_k - C + A}{2A}$$

$$C - A + 2A\frac{CH_{k-1}}{M} \xrightarrow[M\to\infty]{} T_k$$

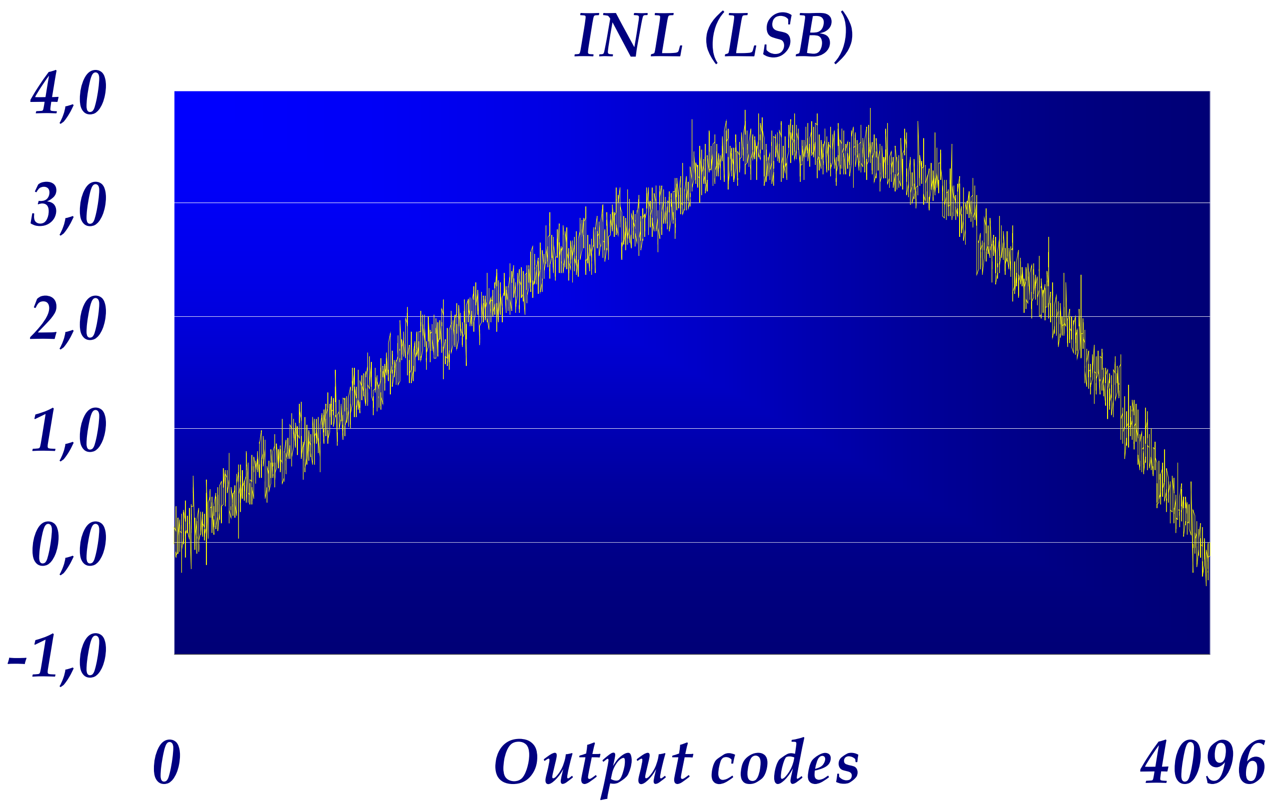
$$T_k^{est} = C - A + 2A\frac{CH_{k-1}}{M}$$

Triangular Wave Nonlinearity

- If the triangular wave used is not linear then the amplitude density function will not be uniform and the ADC transfer function will be estimated incorrectly



Triangular Wave Nonlinearity



Summary of Histogram Test

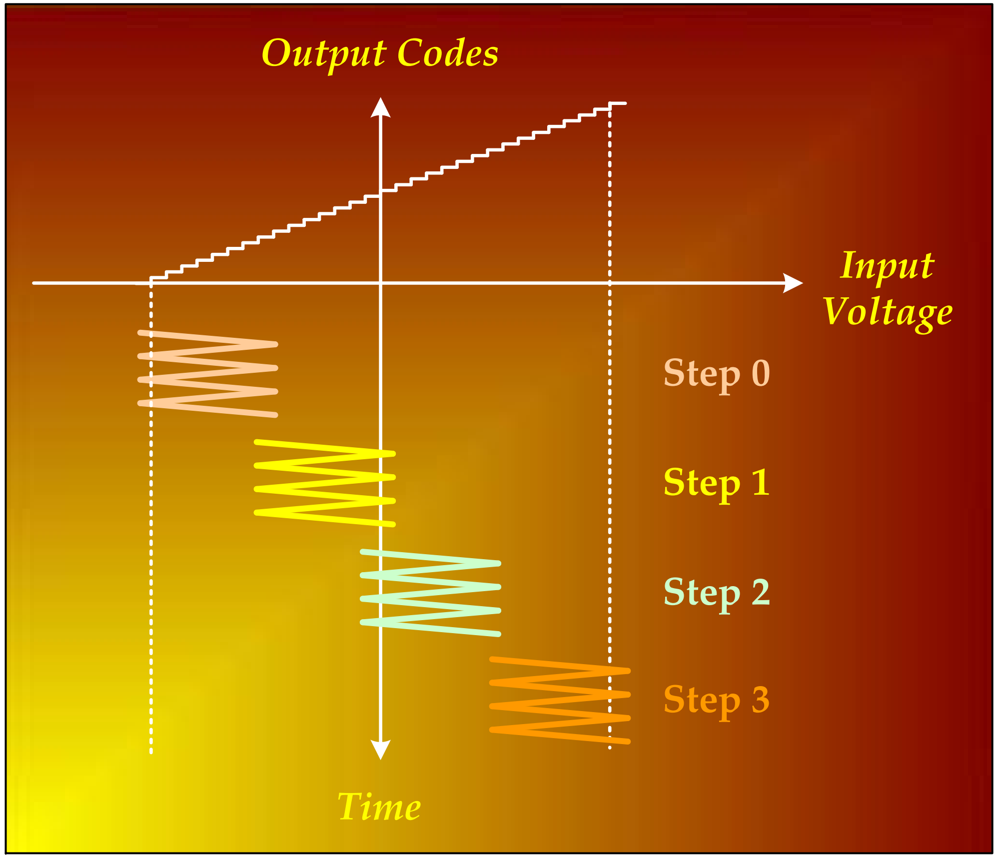
- All codes stimulated at once
- Faster than static test because there is no need to wait for the DC source to settle
- Needs a highly linear triangular wave

Ramp Vernier Test

Ramp Vernier Test

- Combines Traditional Static Test and Histogram Test
- Tries to use the best of both worlds
- Use of small amplitude triangular waves to relax the linearity requirements
- Use different offsets to cover all of the ADC input range

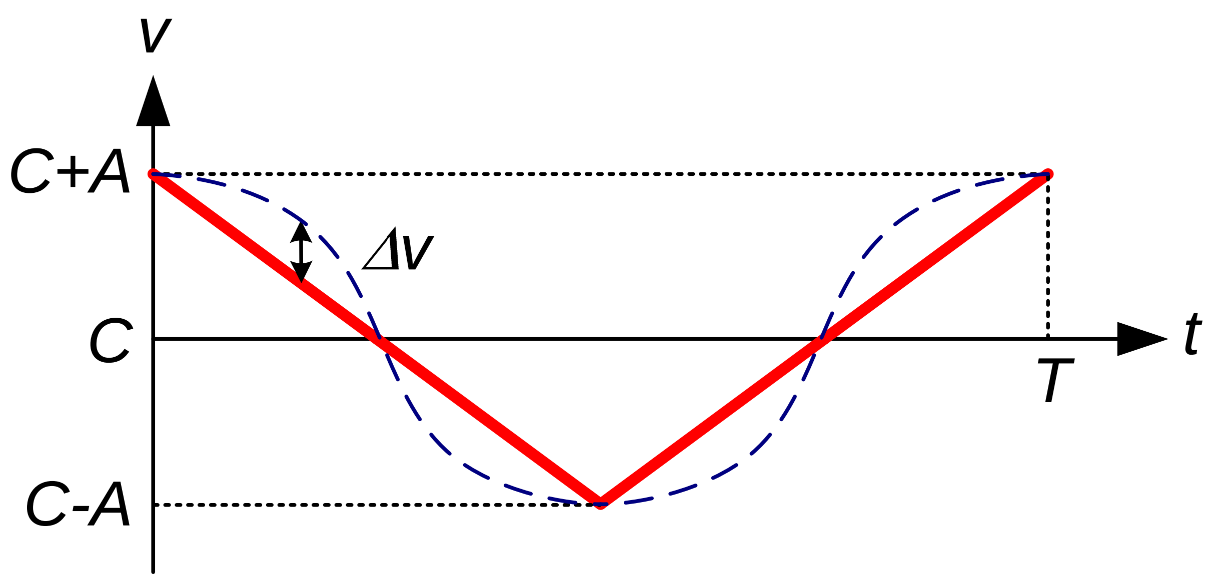
Ramp Vernier Test



Procedure

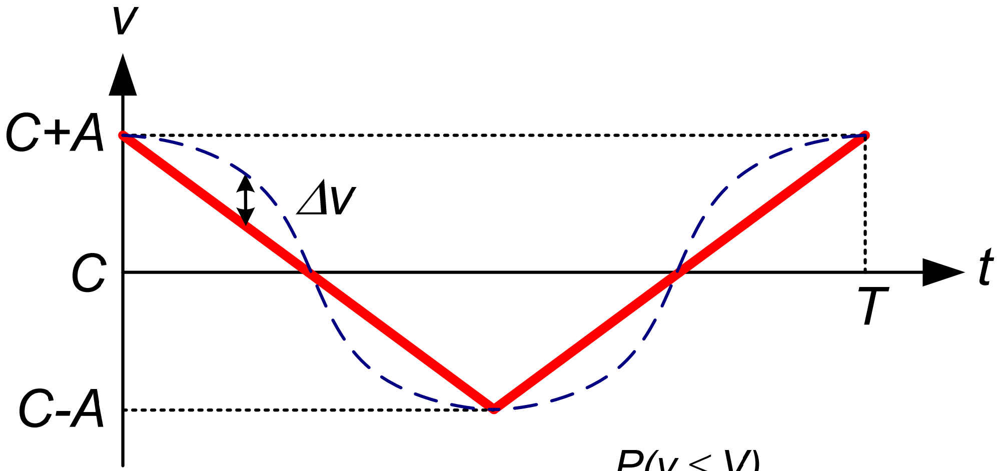
- In each step compute the code bin widths as in the Histogram Test
- Combine the code bin widths from different steps
- Compute the transition voltages, gain and offset error, INL and DNL

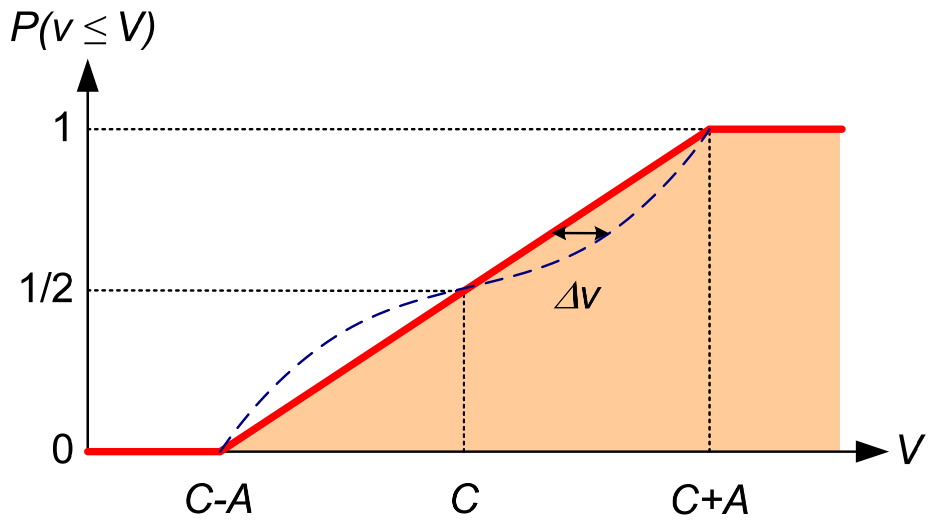
Error due to Nonlinearity



$$NL = \frac{\Delta v_{max}}{A}$$

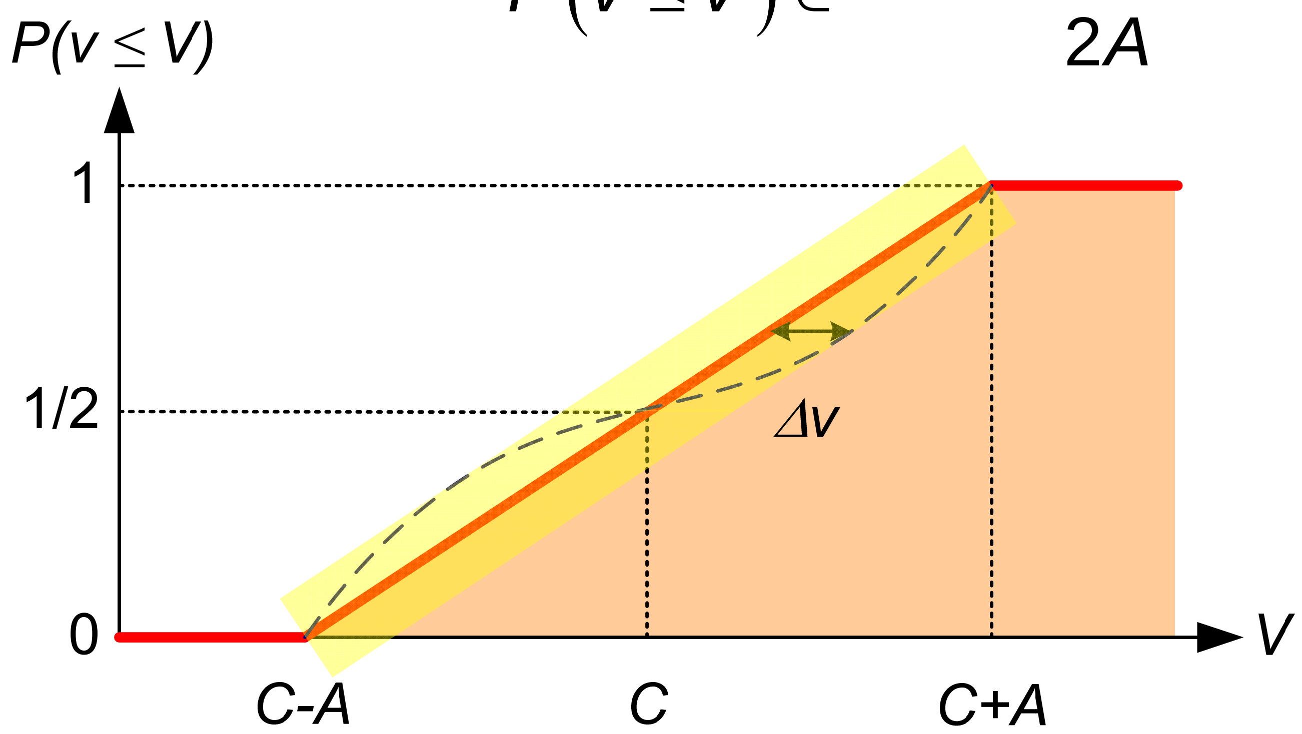
Error due to Nonlinearity





Error due to Nonlinearity

$$P\left(v \le V\right) \in \frac{V \pm \Delta v_{max} - C + A}{2A}$$



Estimate Transition Voltages

$$\frac{CH_{k-1}}{M} \xrightarrow[M\to\infty]{} P\left(v \le T_k\right)$$

$$\frac{CH_{k-1}}{M} \xrightarrow[M\to\infty]{} \frac{T_k \pm \Delta v_{\max} - C + A}{2A}$$

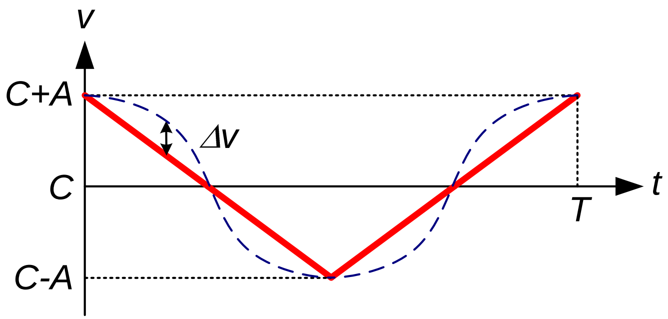
$$C - A + 2A\frac{CH_{k-1}}{M} \pm \Delta v_{\max} \xrightarrow[M\to\infty]{} T_k$$

$$T_k^{est} = C - A + 2A\frac{CH_{k-1}}{M} \pm \Delta v_{\max}$$

Estimation Error

$$T_k^{est} = C - A + 2A\frac{CH_{k-1}}{M} \pm \Delta v_{max}$$

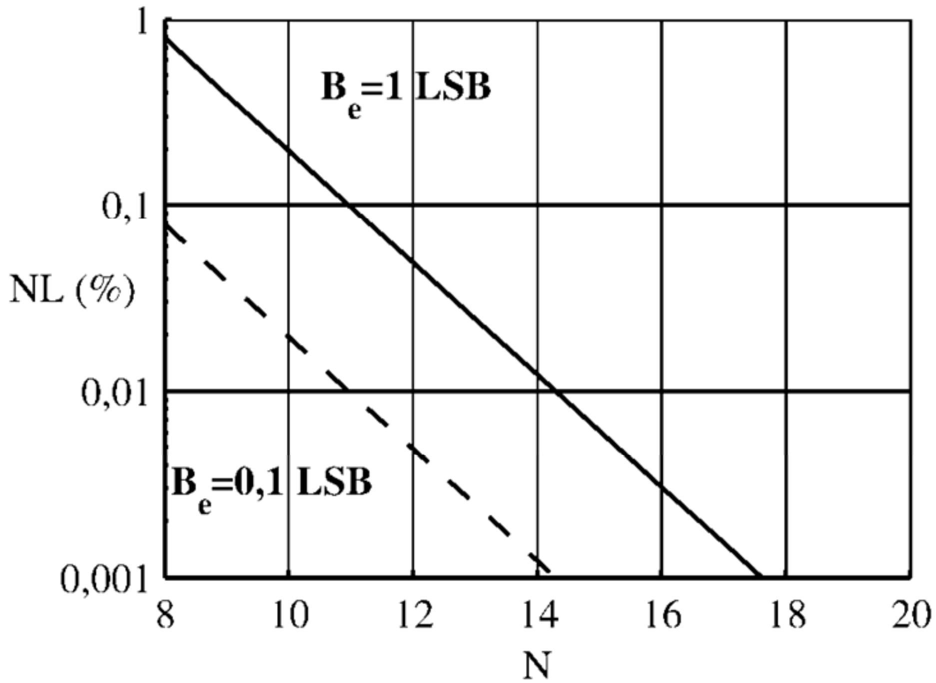
$$NL = \frac{\Delta v_{max}}{A}$$



$$\left|e_{T_k}\right| \leq \Delta v_{max} = NL \cdot A$$

$$\left|e_{T_k}\right| \leq B_i \cdot Q \Rightarrow A \leq \frac{B_i \cdot Q}{NL}$$

Required Nonlinearity

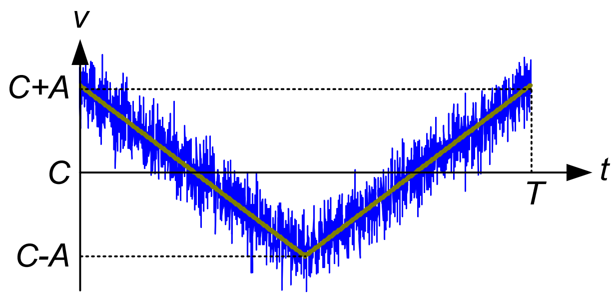


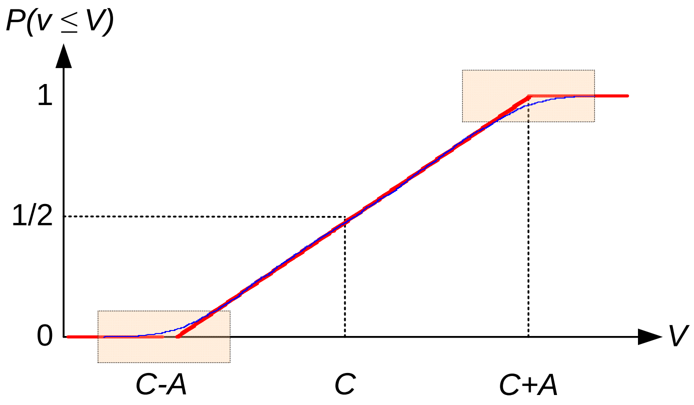
Amplitude Choice

- To guarantee an error in the estimated transition voltages lower than B_i LSBs we need to use a triangular wave amplitude given by:

$$A \leq \frac{B_i \cdot Q}{NL} = A_{\max}$$

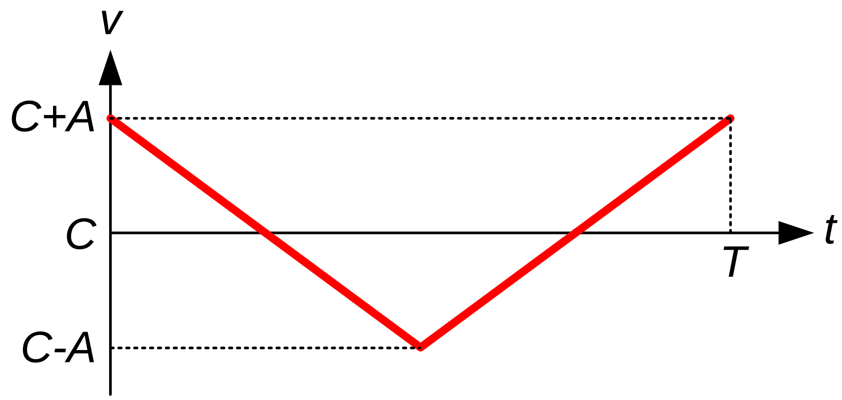
Influence of Additive Noise





- Additive noise causes an error in the amplitude distribution of the triangular wave

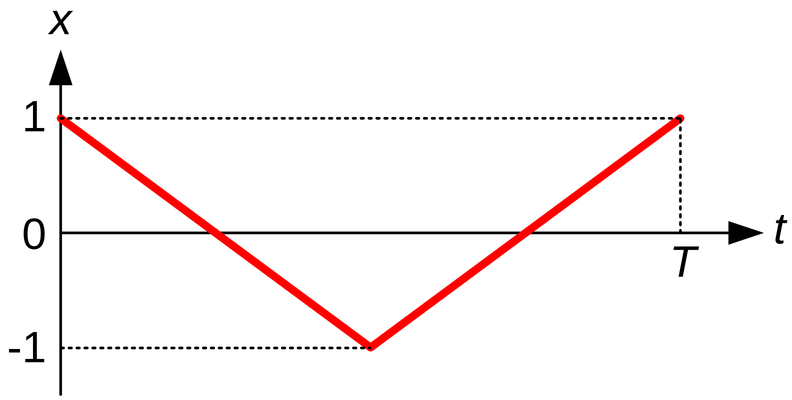
Triangular Stimulus Signal



$$v(t) = C - A \cdot tri(2\pi \cdot f \cdot t + \varphi)$$

$$tri(\beta) = \begin{cases} 1 - 4\left\langle \frac{\beta}{2\pi} \right\rangle & , \quad 0 \le \left\langle \frac{\beta}{2\pi} \right\rangle \le \frac{1}{2} \\ 4\left\langle \frac{\beta}{2\pi} \right\rangle - 3 & , \quad \frac{1}{2} < \left\langle \frac{\beta}{2\pi} \right\rangle < 1 \end{cases}$$

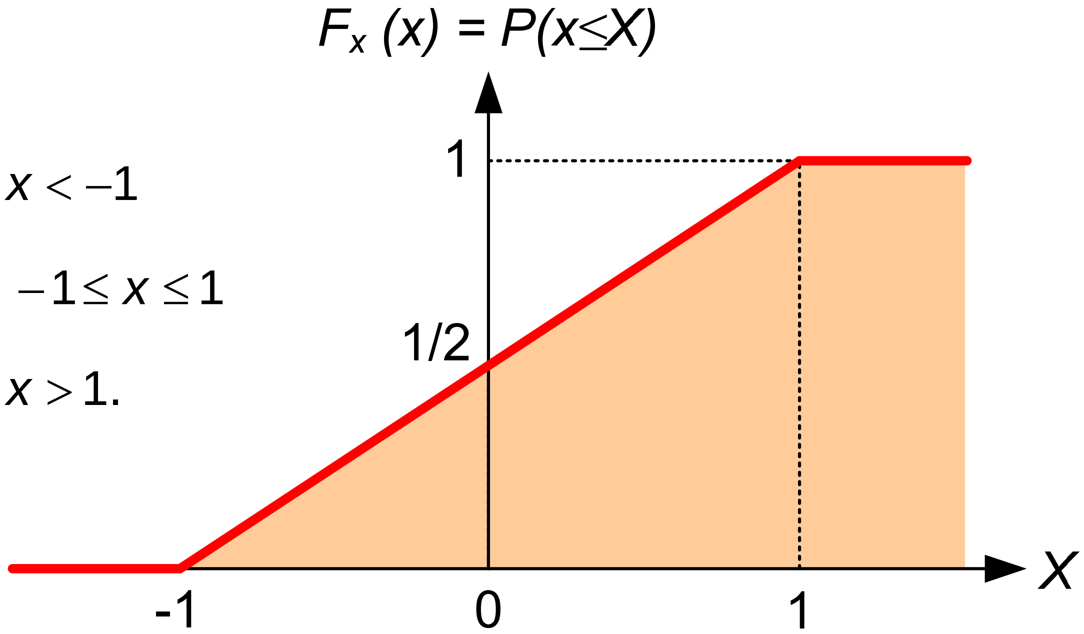
Normalization



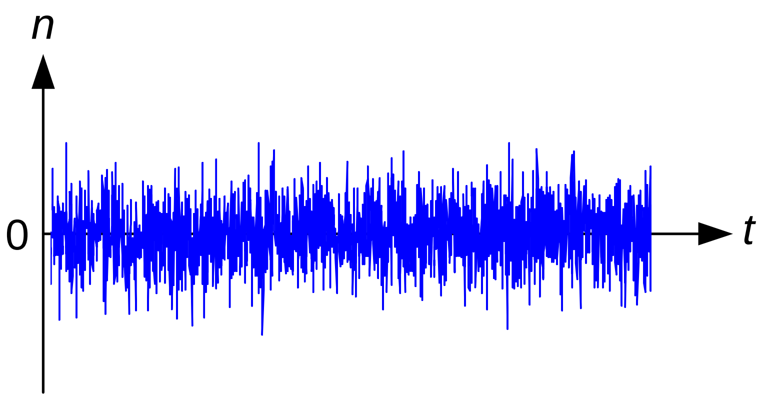
$$x(t) = tri(2\pi \cdot f \cdot t + \varphi)$$

Cumulative Density Function

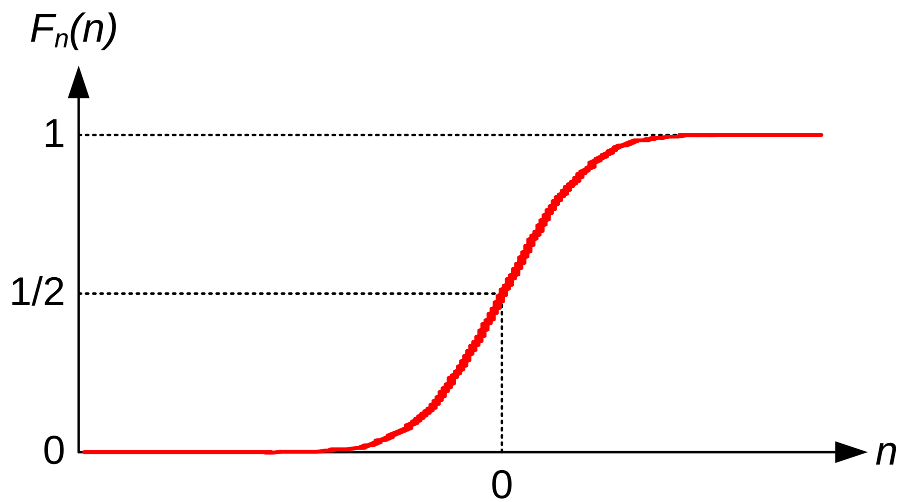
$$F_x(x) = \begin{cases} 0 & , \quad x < -1 \\ \dfrac{x+1}{2} & , \quad -1 \le x \le 1 \\ 1 & , \quad x > 1. \end{cases}$$



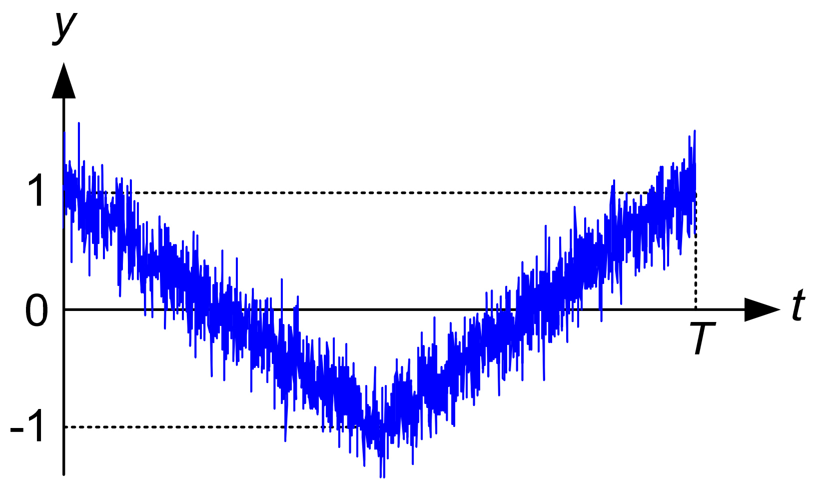
Additive Noise



$$f_n(n) = \frac{1}{\sqrt{2\pi\sigma}} e^{\frac{-n^2}{2\sigma_n^2}}$$



Triangular Wave + Noise



$$F_y\left(y\right) = F_x * f_n\left(y\right) = \int_{-\infty}^{\infty} F_x(z) f_n\left(y - z\right) dz$$

Combining Distributions

$$F_y(y) = F_x * f_n(y) = \int_{-\infty}^{\infty} F_x(z) f_n(y-z)\,dz$$

$$F_x(x) = \begin{cases} 0 & , \quad x < -1 \\ \dfrac{x+1}{2} & , \quad -1 \le x \le 1 \\ 1 & , \quad x > 1. \end{cases}$$

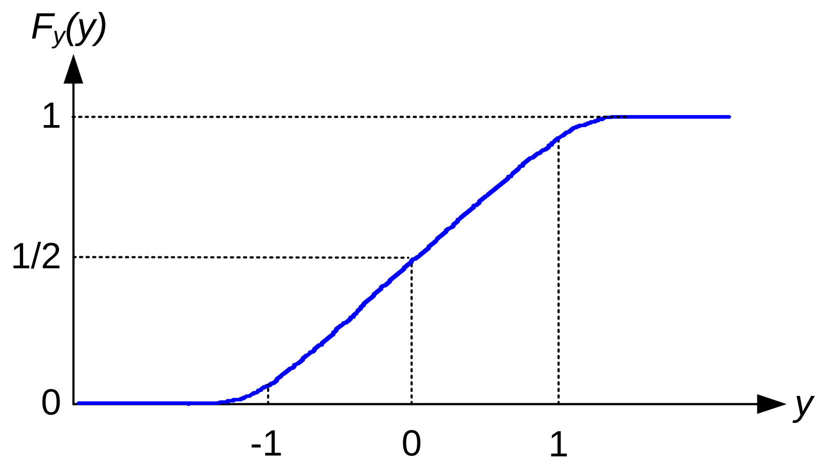
$$f_n(n) = \frac{1}{\sqrt{2\pi\sigma}} e^{\frac{-n^2}{2\sigma_n^2}}$$

$$F_y(y) = \int_{-1}^{1} \frac{z+1}{2} \frac{1}{\sqrt{2\pi\sigma_n}} e^{\frac{-(y-z)^2}{2\sigma_n^2}} dz + \int_{1}^{\infty} \frac{1}{\sqrt{2\pi\sigma_n}} e^{\frac{-(y-z)^2}{2\sigma_n^2}} dz$$

End Result

$$F_y(y) = \frac{1+y}{4}\left[erf\left(\frac{y+1}{\sqrt{2}\sigma_n}\right) - erf\left(\frac{y-1}{\sqrt{2}\sigma_n}\right)\right] +$$

$$+\frac{\sigma_n}{2\sqrt{2\pi}}\left[e^{\frac{-(y+1)^2}{2\sigma_n^2}} - e^{\frac{-(y-1)^2}{2\sigma_n^2}}\right] + \frac{1}{2} - \frac{1}{2}erf\left(\frac{1-y}{\sqrt{2}\sigma_n}\right).$$



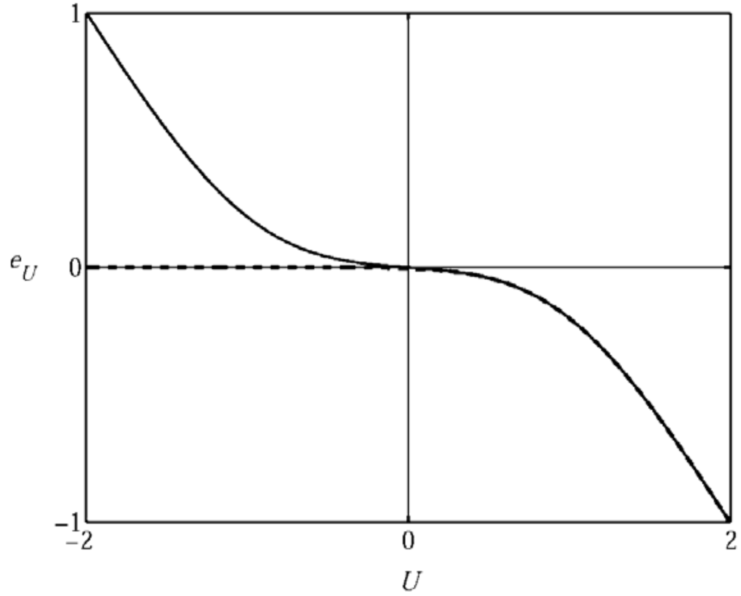
Estimated Transition Voltages

$$U = \frac{T - C}{A}$$

$$U_{est} = 2 \cdot F_y(U) - 1$$

Estimation Error

$$e_U = U_{est} - U = \frac{U+1}{2} erf\left(\frac{U+1}{\sqrt{2}\sigma_n}\right) - \frac{U-1}{2} erf\left(\frac{U-1}{\sqrt{2}\sigma_n}\right) + $$
$$+ \frac{\sigma_n}{\sqrt{2\pi}}\left[e^{\frac{-(U+1)^2}{2\sigma_n^2}} - e^{\frac{-(U-1)^2}{2\sigma_n^2}}\right] - U,$$



Approximate Expression

$$erf\left(\frac{x}{\sqrt{2}\sigma_n}\right) \approx 1 \quad , \quad x > 3 \cdot \sigma_n$$

$$erf\left(\frac{x}{\sqrt{2}\sigma_n}\right) \approx -1 \quad , \quad x < -3 \cdot \sigma_n .$$

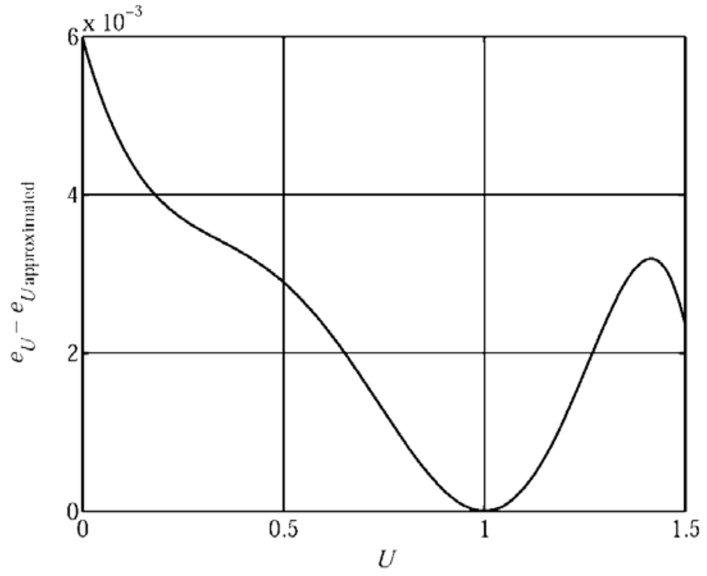
$$e_U \approx -\frac{U-1}{2}\left[erf\left(\frac{U-1}{\sqrt{2}\sigma_n}\right)+1\right]-\frac{\sigma_n}{\sqrt{2\pi}}e^{-\frac{(U-1)^2}{2\sigma_n^2}} \quad , \quad U > 0 \quad \wedge \quad \sigma_n < \frac{1}{3} .$$

Approximate Expression II

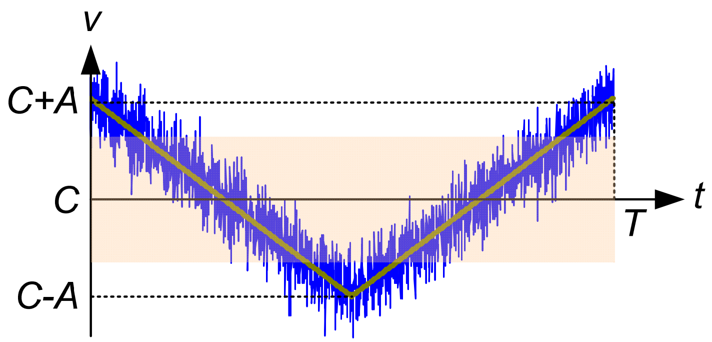
$$e_U \approx -\frac{\sigma_n}{\sqrt{2\pi}} e^{a_0 w + a_1 w^2} \quad \text{with} \quad w = \frac{U-1}{\sqrt{2}\cdot\sigma_n}$$

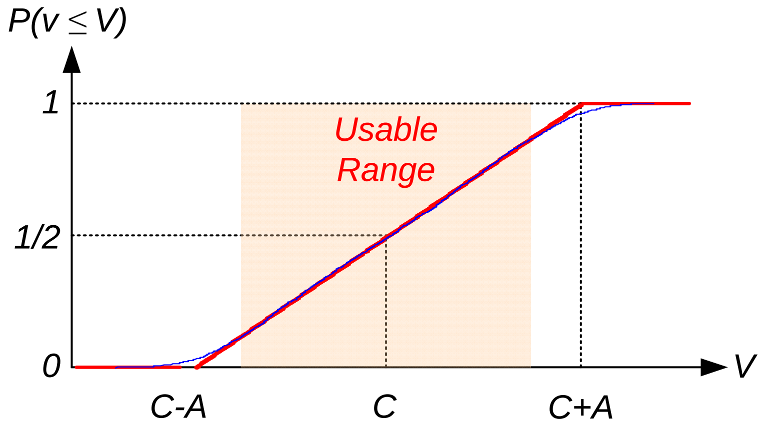
$$e_U \approx -\frac{\sigma_n}{\sqrt{2\pi}} e^{-\sqrt{\pi}\frac{U-1}{\sqrt{2}\sigma_n} - \frac{(U-1)^2}{4\sigma_n^2}}$$

for $U > 0$



Overdrive





- The triangular wave peaks should not be used - *Overdrive*

Amount of Overdrive

- Given a certain amount of additive noise, σ_n, the triangular wave amplitude should be an extra V_{OD} greater than required to guarantee an error lower than B_i

$$V_{OD} = \sigma_n \cdot \left[\sqrt{2\pi - 4 \cdot \ln\left(\sqrt{2\pi} \frac{B_i \cdot Q}{\sigma_n} \right)} - \sqrt{2\pi} \right], \ B_i < \frac{\sigma_n}{Q\sqrt{2\pi}}$$

Range Covered in Each Step

- Taking into account both triangular wave nonlinearity and the presence of additive noise the maximum range covered in each step should be:

$$\Delta s_{\max} = 2 \cdot \left(A_{\max} - V_{OD} \right)$$

Number of Steps

$$N_s = \left\lfloor \frac{2 \cdot FS}{\Delta s_{\max}} \right\rfloor = \left\lfloor \frac{FS}{A_{\max} - V_{OD}} \right\rfloor$$

$$\Delta s = \frac{2 \cdot FS}{N_s}$$

Offset to Use in Each Step

$$C^j = T_1 + \left(j + \frac{1}{2} \right) \cdot \Delta s \quad , \quad j = 0,1,\ldots,N_s - 1$$

Summary of Parameters

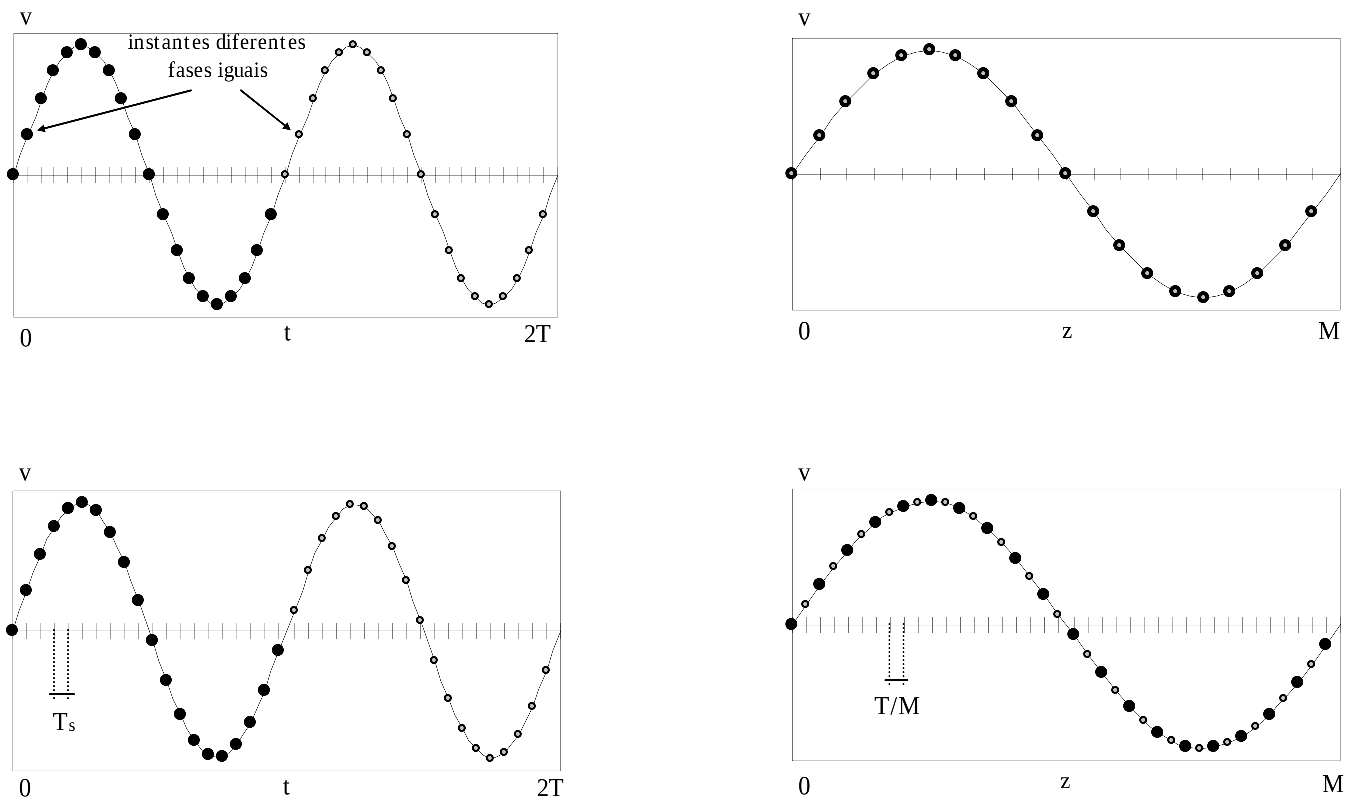
- Maximum allowable error $\rightarrow$ $\boldsymbol{B_i}$
- Triangular wave nonlinearity $\rightarrow$ ***NL***
- Presence of additive noise $\rightarrow$ $\boldsymbol{\sigma_n}$

$$V_{OD} = \sigma_n \cdot \left[\sqrt{2\pi - 4 \cdot \ln\left(\sqrt{2\pi} \frac{B_i \cdot Q}{\sigma_n} \right)} - \sqrt{2\pi} \right]$$

$$A = \frac{B_i \cdot Q}{NL} \qquad N_s = \left\lfloor \frac{FS}{A - V_{OD}} \right\rfloor \qquad \Delta s = \frac{2 \cdot FS}{N_s}$$

$$C^j = T_1 + \left(j + \frac{1}{2} \right) \cdot \Delta s \quad , \quad j = 0,1,\ldots,N_s - 1$$

Coherent Sampling



Coherent Sampling

$$\rho = \frac{f}{f_s} = \frac{D}{M} \quad , \quad D \text{ and } M \text{ mutually prime}$$

Frequency Error

$$\Delta\rho \leq \frac{1}{2M^2}$$

$$\Delta\rho = \left|\rho_{ideal} - \rho\right|$$

$$\Delta\rho = \left|\frac{f_{ideal}}{f_{s\ ideal}} - \frac{f}{f_s}\right|$$

$$\Delta\rho = \left|\frac{f_{ideal}}{f_{s\ ideal}} - \frac{f_{ideal}\cdot\left(1\pm\varepsilon_f\right)}{f_{s\ ideal}\cdot\left(1\pm\varepsilon_{f_s}\right)}\right|$$

Number of Samples

$$M \leq \sqrt{\frac{1}{2}\frac{f_s}{f}\frac{\left|1-\varepsilon_{f_s}\right|}{\left(\varepsilon_{f_s}+\varepsilon_f\right)}} = M_{\max}$$

Number of Samples

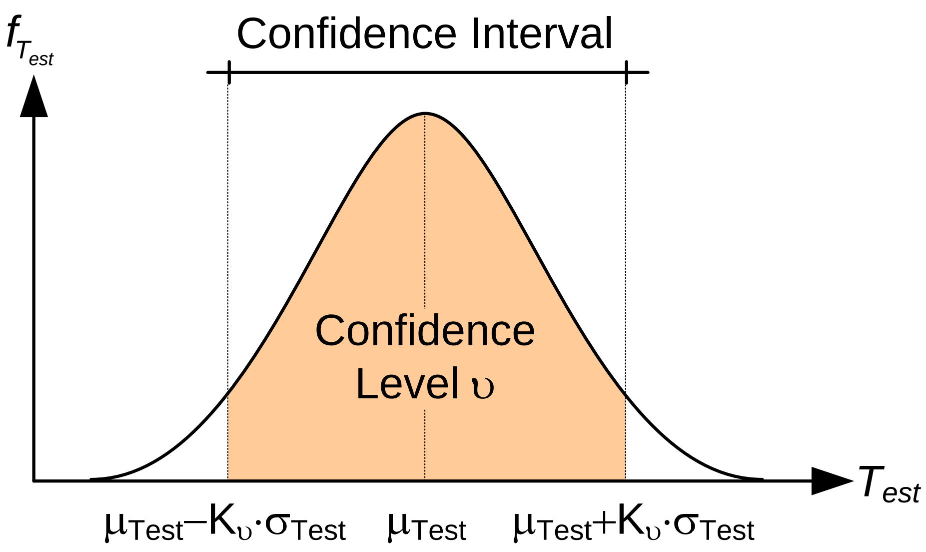
- The more samples are acquired more precise is the estimation but longer will be the test
- Both the presence of additive noise and of uncertainty in the sampling instant (jitter) affect the precision

Number of Records

- Generally the maximum number of consecutive samples is not enough to guarantee a certain level of precision B_u

$$R_{\min} = \left(\frac{K_\nu}{B_u} \frac{2A}{Q} \right)^2 \left(\frac{\sigma_n}{2\sqrt{\pi} AM} + \frac{\sigma_\phi}{\pi\sqrt{\pi} M} + \frac{1}{4M^2} \right)$$

Confidence Interval



ν	K_{ν}
95.4%	2
99.0%	2.58
99.9%	3.29

Computing Code Bin Widths

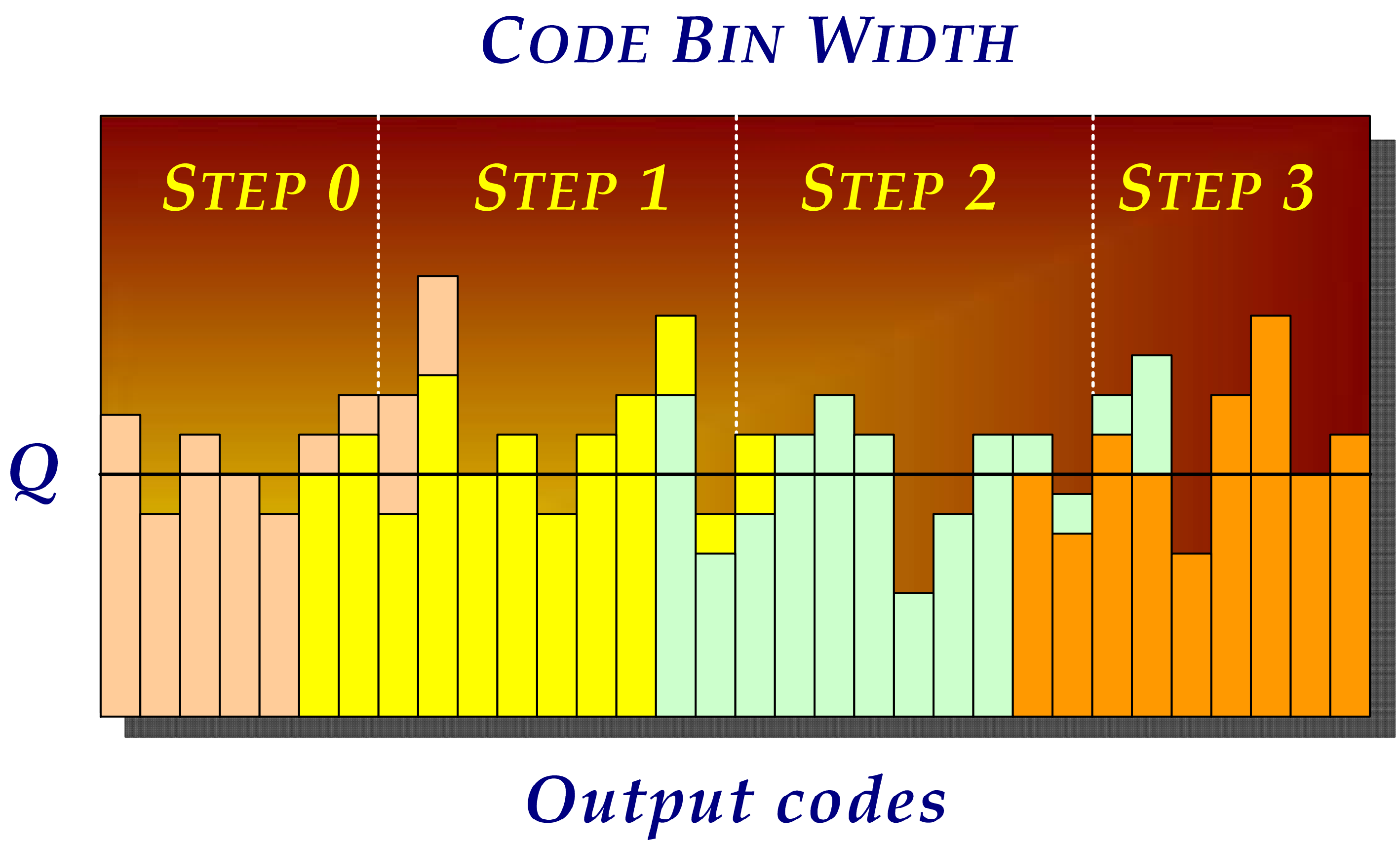
$$T_k^j = C^j + A \cdot \left(2 \cdot \frac{CH_{k-1}^j}{M} - 1 \right)$$

$$k = 1, 2, \ldots, 2^N - 1 \;\; , \; j = 0, 1, \ldots, N_s - 1$$

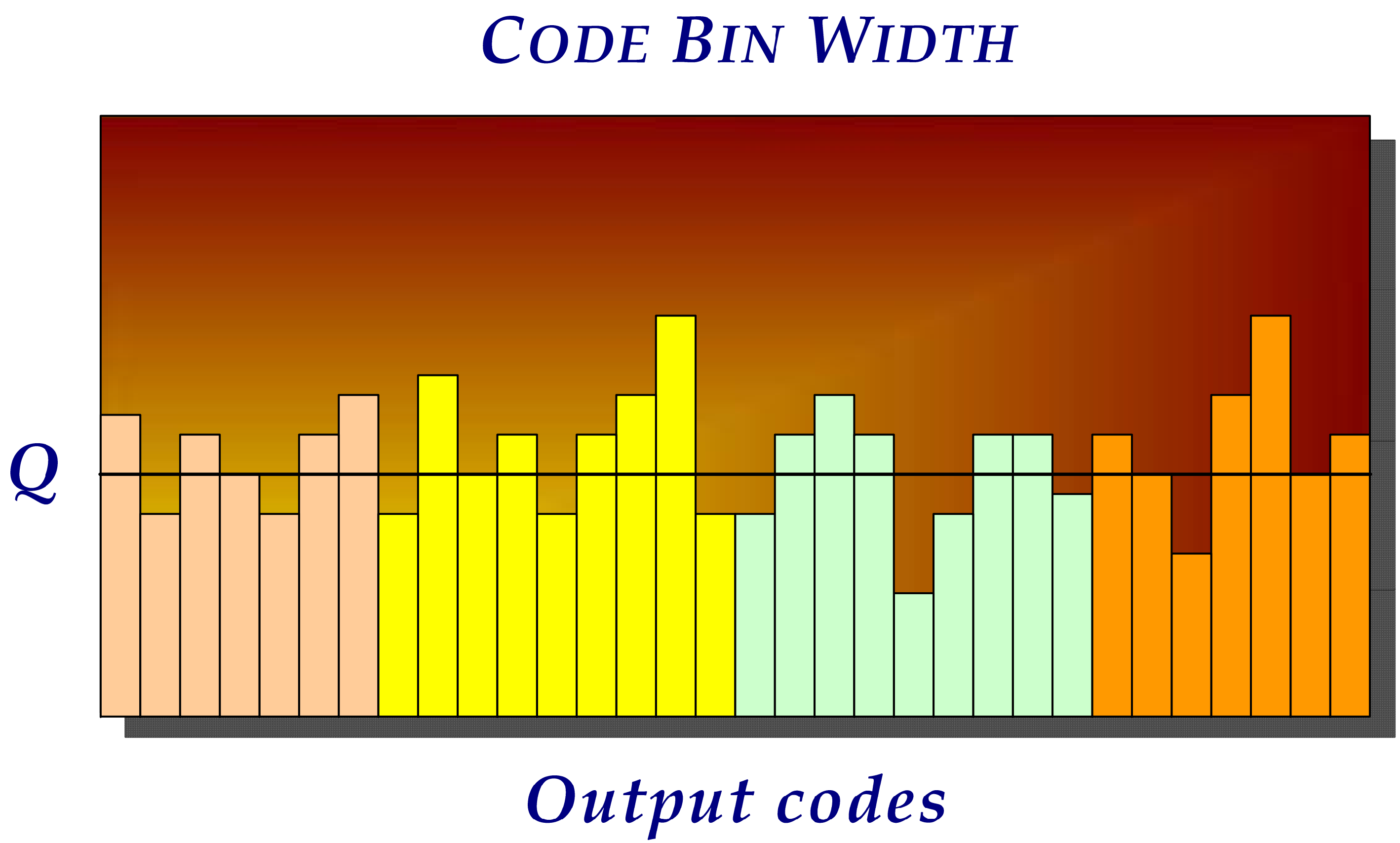
$$W_k^j = T_{k-1}^j - T_k^j$$

$$k = 1, 2, \ldots, 2^N - 2 \;\; , \; j = 0, 1, \ldots, N_s - 1$$

Combining the Steps



Combining the Steps

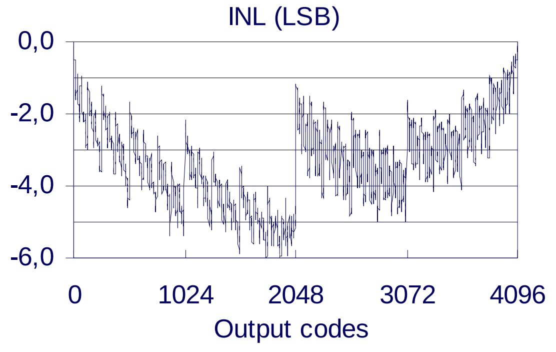


Transition Voltages

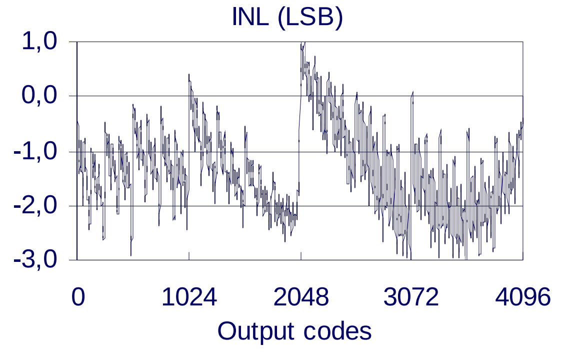
$$T_k = \begin{cases} T_1^0 & , \quad k = 1 \\ T_{k-1} + W_k & , \quad k = 2,3,\ldots,2^N - 1 \end{cases}$$

Example - INL Estimation

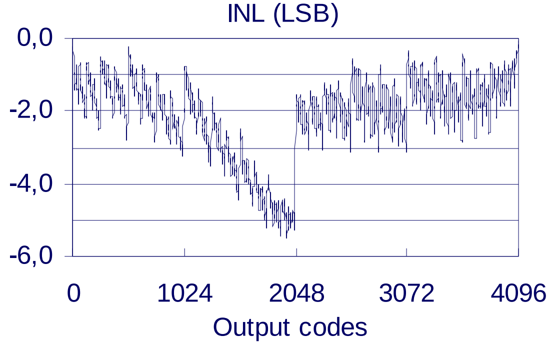
Traditional Static Test



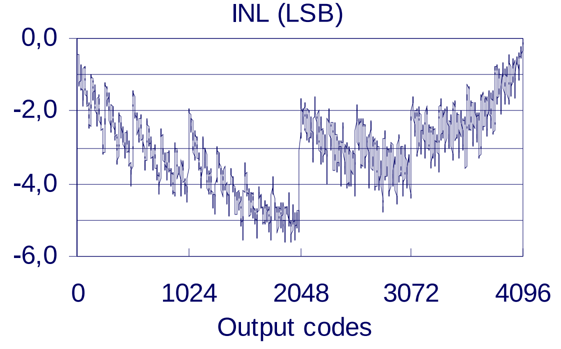
Ramp Vernier Test (1 Step)



Ramp Vernier Test (2 Steps)

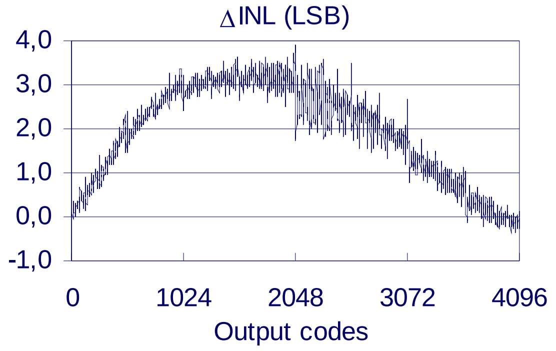


Ramp Vernier Test (10 Steps)

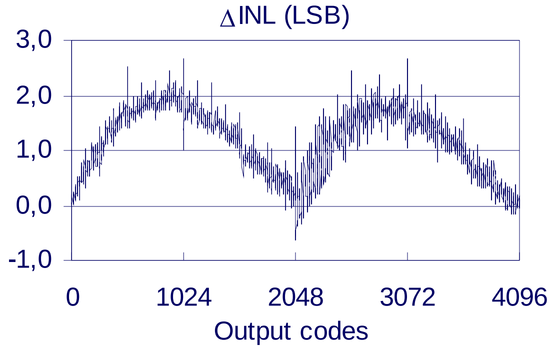


INL Estimation Error

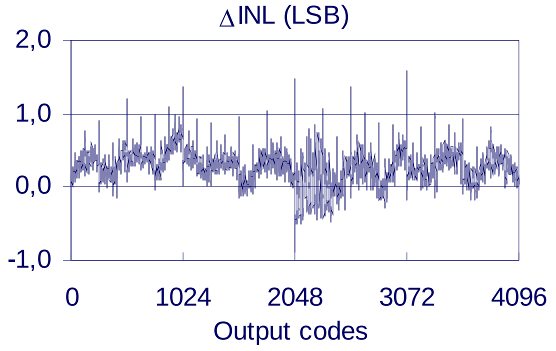
Ramp Vernier Test (1 Step)



Ramp Vernier Test (2 Steps)

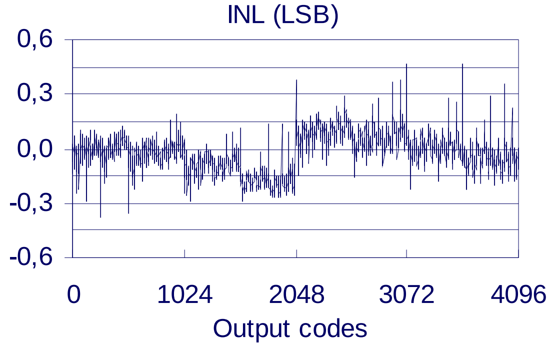


Ramp Vernier Test (10 Steps)

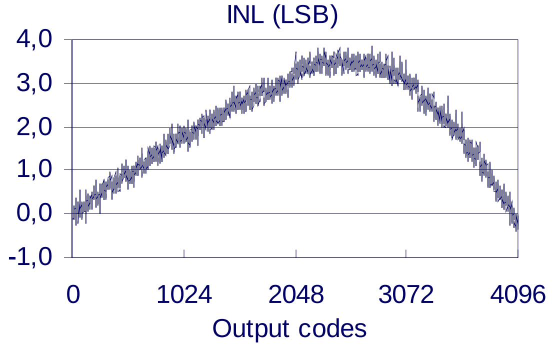


Another Example

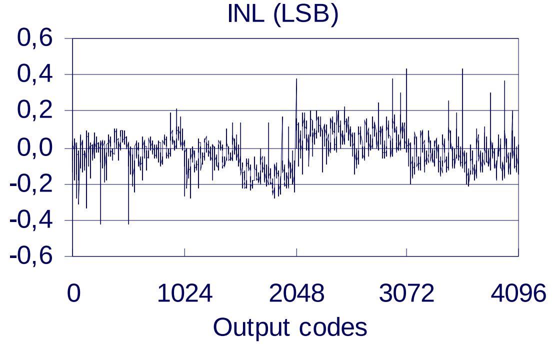
Traditional Static Test



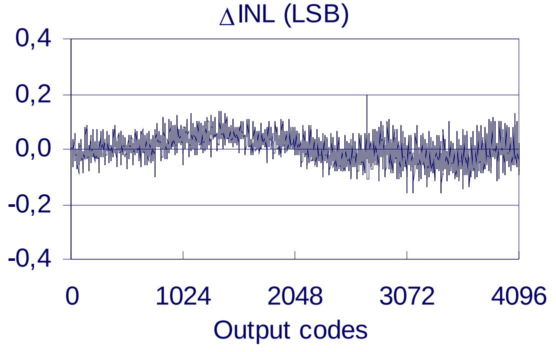
Ramp Vernier Test (1 Step)



Ramp Vernier Test (80 Steps)



Ramp Vernier Test (80 Steps)



Static Test Duration

- Number of steps per ADC code → N_T
- DC source settling Time → T_{SL}
- Communication time per sample → T_C

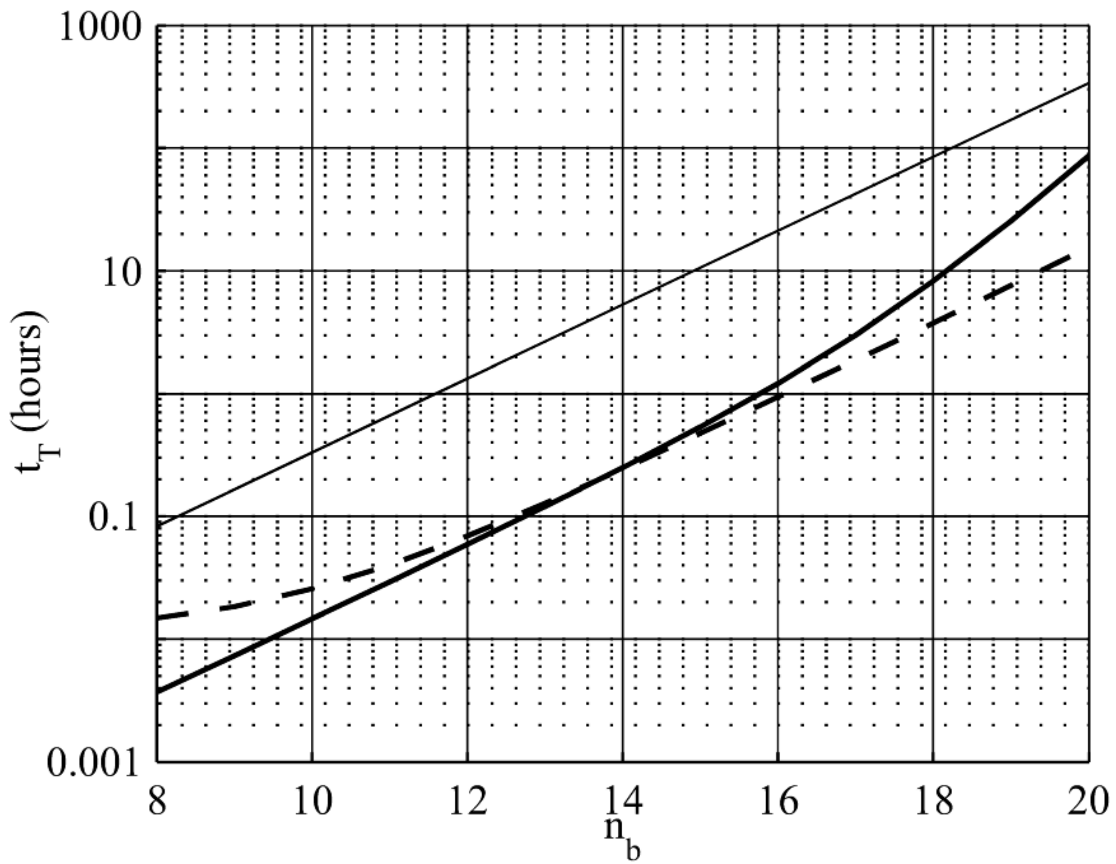
$$t_T = N_T \cdot \left(2^{n_b} - 1\right) \cdot \left[T_{SL} + \left(T_C + \frac{1}{f_s} \right) \cdot M \right]$$

Ramp Vernier Test Duration

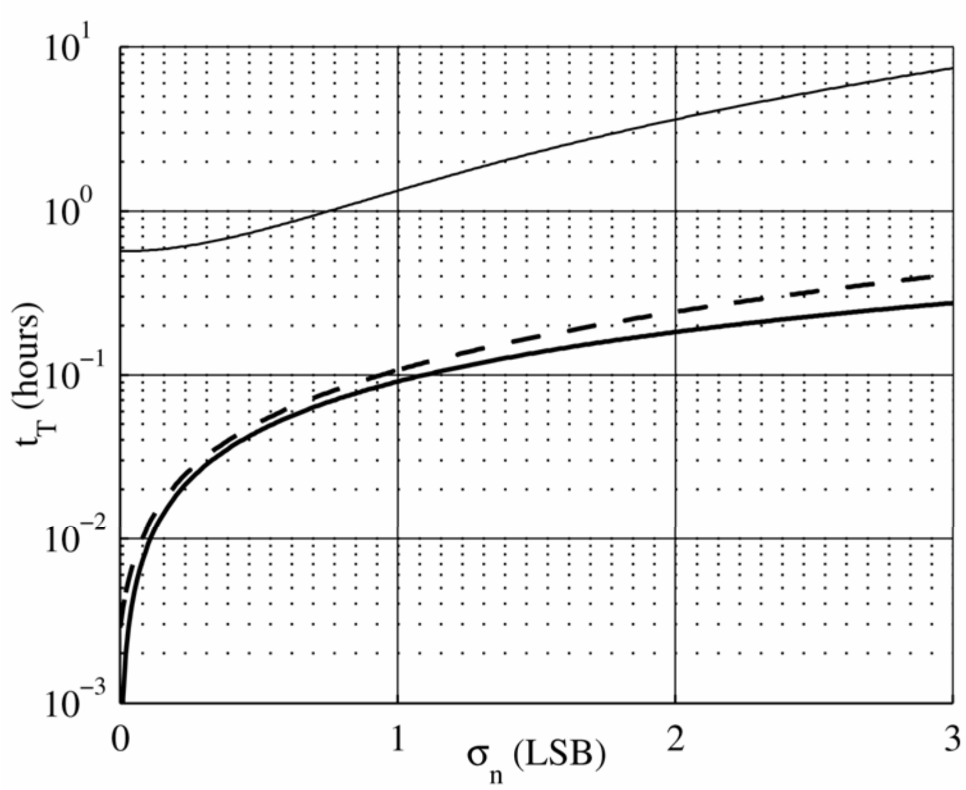
- Number of Vernier steps $\rightarrow N_S$
- DC source settling Time $\rightarrow T_{SL}$
- Communication time per sample $\rightarrow T_C$

$$t_T = N_s \cdot \left[T_{SL} + \left(T_C + \frac{1}{f_s} \right) \cdot R \cdot M \right]$$

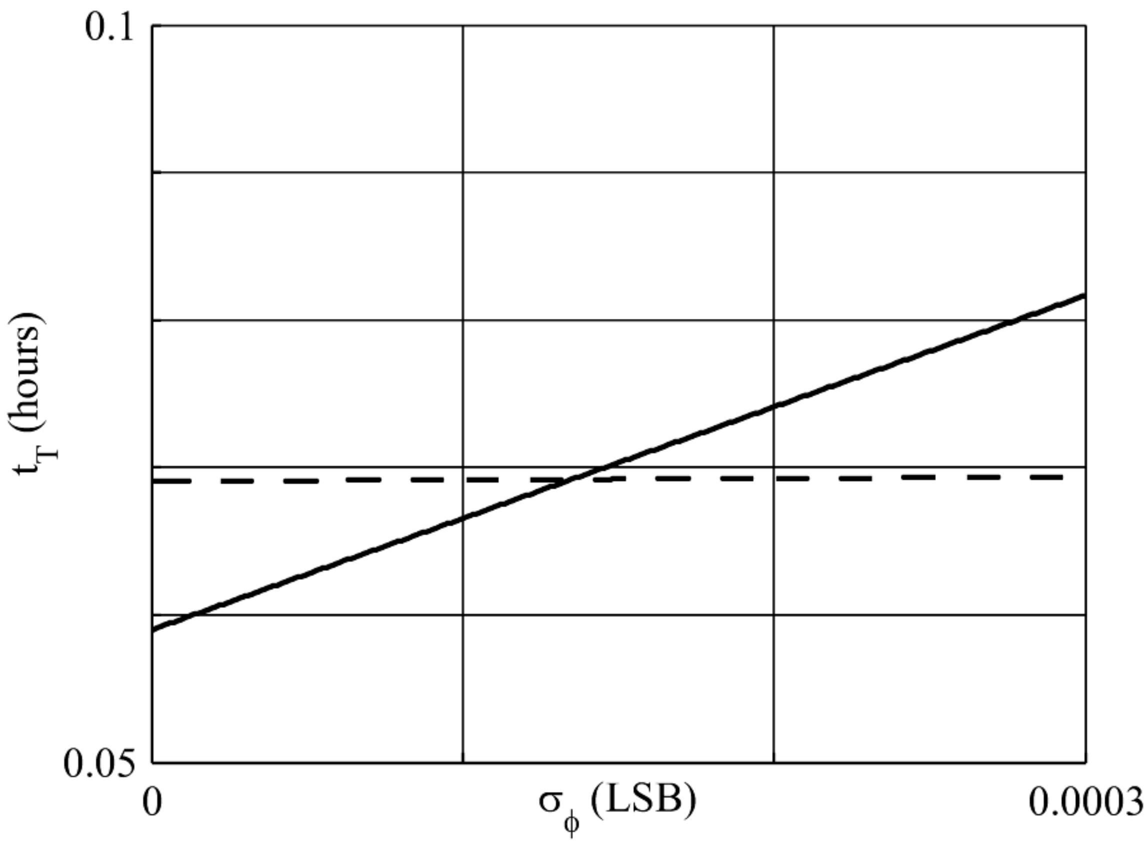
Duration vs. Number of Bits



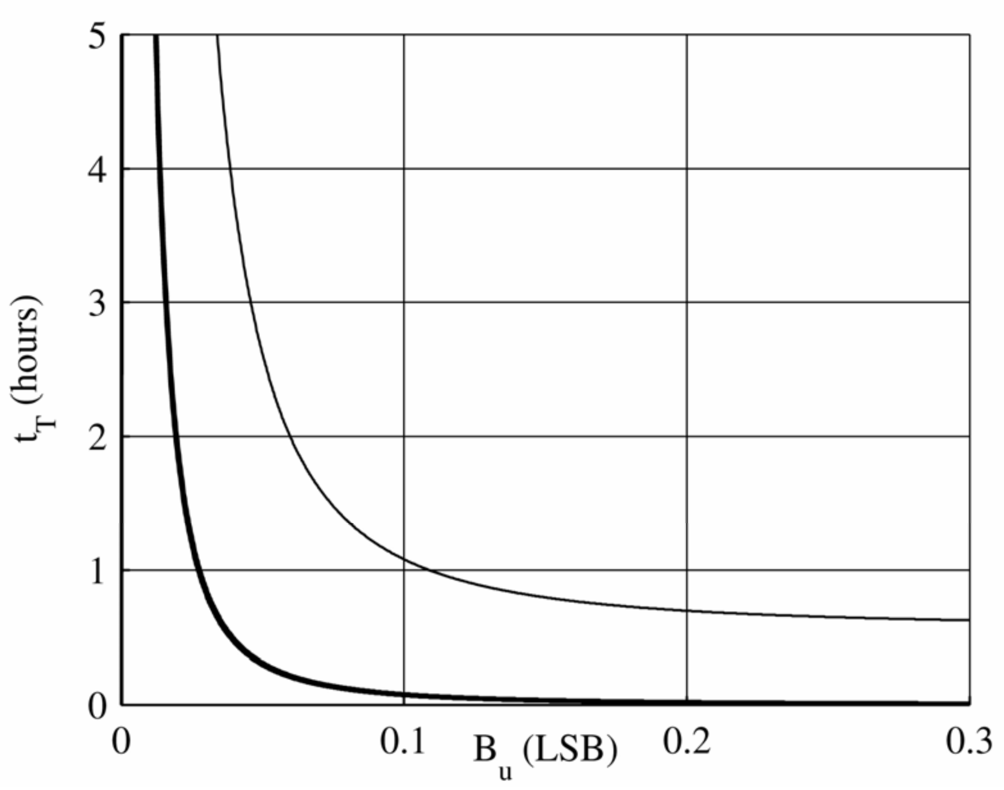
Duration vs. Additive Noise



Duration vs. Phase Noise



Duration vs. Required Uncertainty



Efficiency Comparison

	Standard Test	Proposed Test
Duration of the test	6 hours	5 minutes
Number of samples required	83,865,600	23,999,760

Conclusion

- Static Test is Important
- Ramp Vernier Test
  - Faster than Traditional Static Test
  - Low cost function generator required
- Additive Noise and Jitter affect the precision of the results