

# **CHAPTER 13 OUTPUT STAGES AND POWER AMPLIFIERS**

## **Chapter Outline**

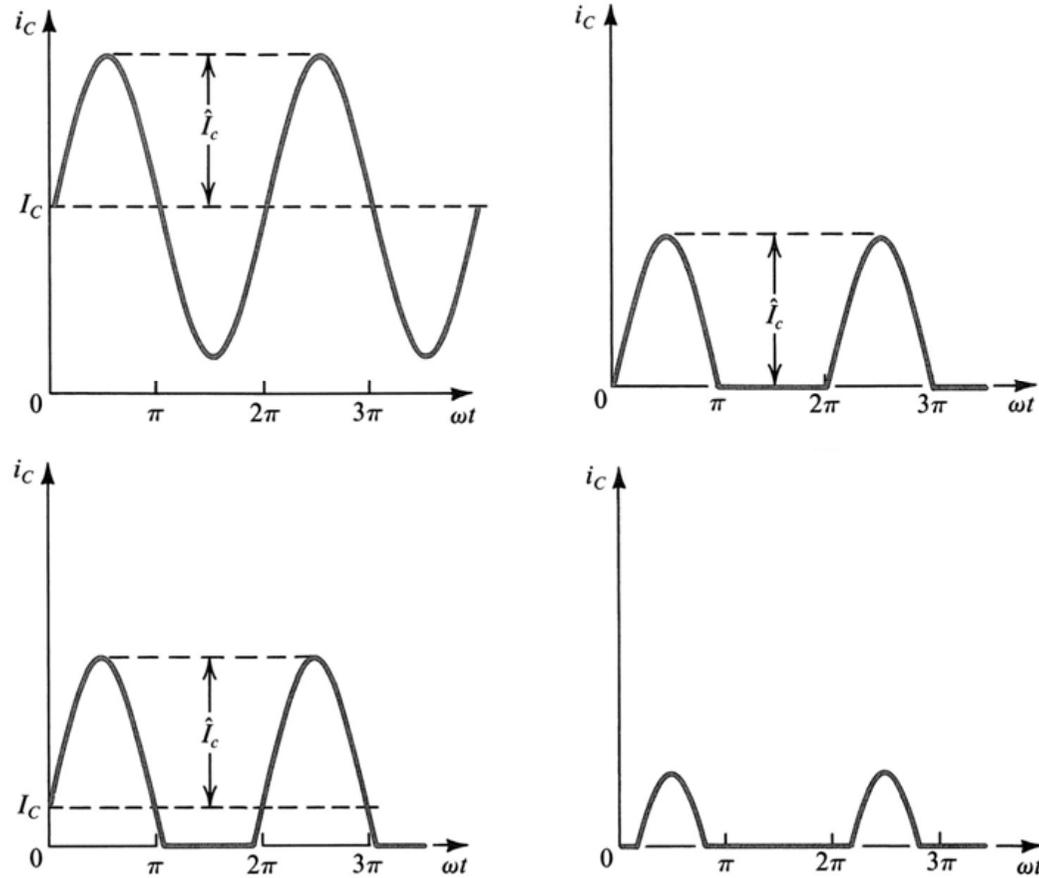
- 13.1 Classification of Output Stages
- 13.2 Class A Output Stage
- 13.3 Class B Output Stage
- 13.4 Class AB Output Stage
- 13.5 Biasing the Class AB Circuit
- 13.6 CMOS Class AB Output Stages

## 13.1 CLASSIFICATIONS OF OUTPUT STAGES

### Output Stages

- Class A output stage:
  - Bias current is greater than the magnitude of the signal current
  - Conduction angle is  $360^\circ$
- Class B output stage:
  - Biased at zero dc current
  - Conduction angle is  $180^\circ$
  - Another transistor conducts during the alternate half-cycle
- Class AB output stage:
  - An intermediate class between A and B
  - Biased at a nonzero dc current much smaller than the peak current of the signal
  - Conduction angle is greater than  $180^\circ$  but much smaller than  $360^\circ$
  - Two transistors are used and currents are combined at the load
- Class C output stage:
  - Conduction angle is smaller than  $180^\circ$
  - The current is passed through a parallel  $LC$  network to obtain the output signal
- Class A, B and AB are used as output stage of op amps
- Class AB amplifiers are preferred for audio power amplifier
- Class C amplifiers are usually used at higher frequencies

- ❑ Collector current waveforms for the transistors operating in different classes
- ❑ The classification also applies for output stages with MOSFETs



## 13.2 CLASS A OUTPUT STAGE

### Transfer Characteristics

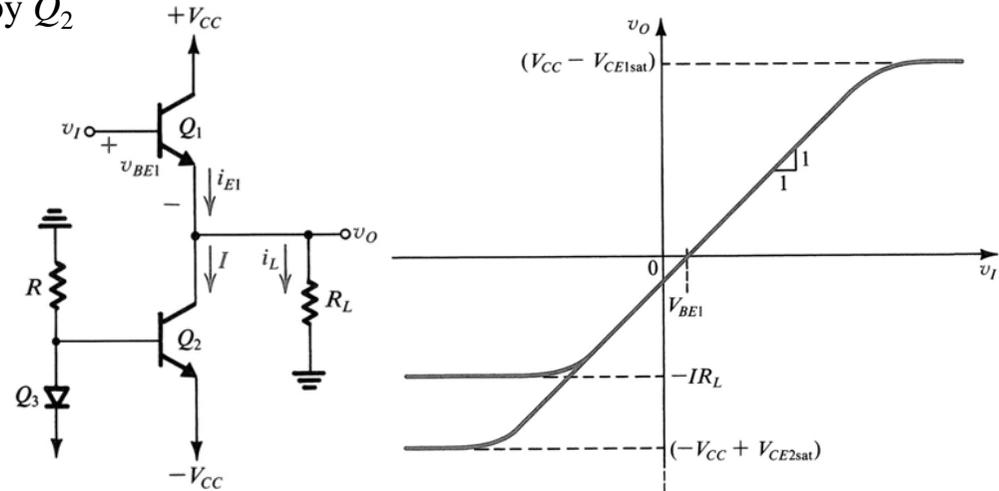
- $Q_1$  biased with a constant current  $I$  supplied by  $Q_2$

$$v_O = v_I - v_{BE1}$$

$$v_{Omax} = V_{CC} - V_{CE1sat}$$

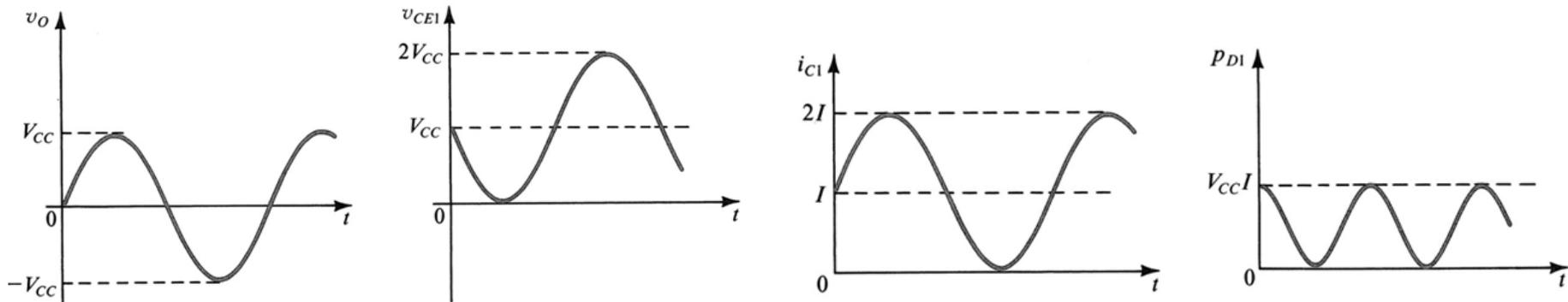
$$v_{Omin} = -IR_L \text{ or } v_{Omin} = -V_{CC} + V_{CE2sat}$$

$$I \geq \frac{|-V_{CC} + V_{CE2sat}|}{R_L}$$



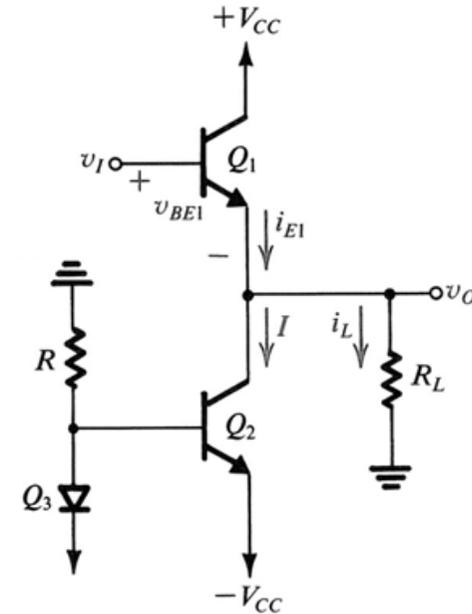
### Signal Waveforms

- The output swing from  $-V_{CC}$  to  $V_{CC}$  for  $I = V_{CC}/R_L$
- The instantaneous power dissipation in  $Q_1$ :  $P_{D1} = v_{CE1}i_{C1}$



## Power Dissipation

- ❑ Power dissipation for  $R_L = V_{CC}/I$ :
  - The maximum instantaneous power dissipation in  $Q_1$  is  $V_{CC}I$
  - This is equal to the power dissipation in  $Q_1$  with no input signal applied (quiescent power dissipation)
  - The transistor  $Q_1$  must be able to withstand a continuous power dissipation of  $V_{CC}I$
- ❑ Power dissipation for unloaded case:
  - Maximum power dissipation occurs when  $v_O = -V_{CC}$
  - The maximum power dissipation in  $Q_1$  is  $2V_{CC}I$
- ❑ Power dissipation for an output short circuit:
  - A positive input may lead to an infinite load current
  - The output stages are usually equipped with short-circuit protection to guard against such a situation
- ❑ Power dissipation in  $Q_2$ :
  - $Q_2$  conducts a constant current  $I$
  - Maximum voltage across the collector and the emitter is  $2V_{CC}$
  - Maximum instantaneous power dissipation in  $Q_2$  is  $2V_{CC}I$
  - A more significant quantity for design purposes is the average power dissipation of  $V_{CC}I$



## **Power Conversion Efficiency**

- ❑ The power conversion efficiency is defined as  $\eta \equiv P_L(\text{load power}) / P_S(\text{supply power})$
- ❑ The load power ( $P_L$ ) with an sinusoid output with a peak value of  $\hat{V}_o$  is

$$P_L = \frac{(\hat{V}_o / \sqrt{2})^2}{R_L} = \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

- ❑ The total average supply power is  $P_S = 2V_{CC}I$
- ❑ The conversion efficiency is given by

$$\eta = \frac{1}{4} \frac{\hat{V}_o^2}{IR_L V_{CC}} = \frac{1}{4} \left( \frac{\hat{V}_o}{IR_L} \right) \left( \frac{\hat{V}_o}{V_{CC}} \right)$$

- ❑ Maximum efficiency (25%) is obtained when  $\hat{V}_o = V_{CC} = IR_L$
- ❑ Class A output stage is rarely used in high-power applications
- ❑ The efficiency achieved in practice is usually in the range of 10% to 20%

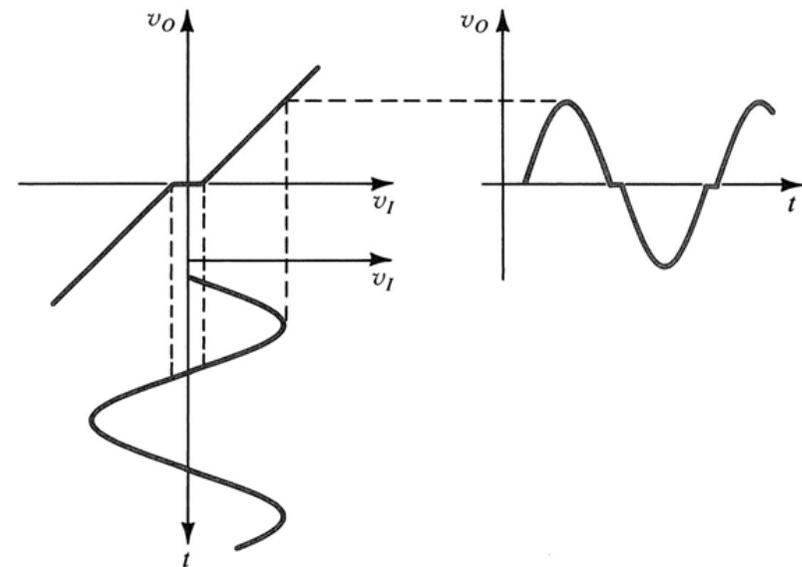
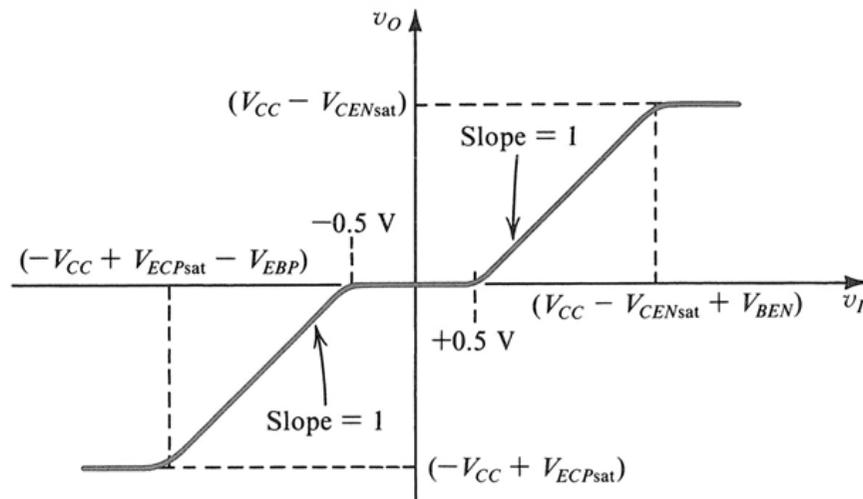
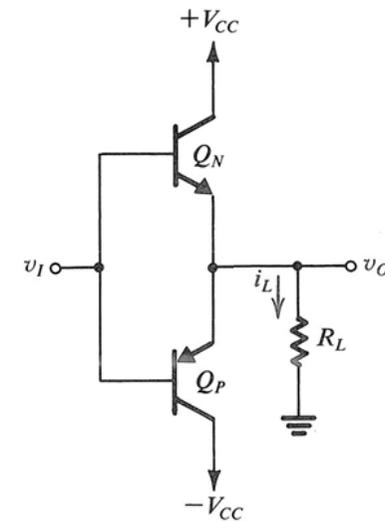
## 13.3 CLASS B OUTPUT STAGE

### Circuit Operation

- ❑ Both transistors are cut off when  $v_I$  is zero  $\rightarrow v_O$  is zero
- ❑ One of the transistor turns on as  $v_I$  exceeds  $\pm 0.5$  V  $\rightarrow v_O$  follows  $v_I$
- ❑ The circuit operates in a push-pull fashion
- ❑ The class B stage is biased at zero current and conducts only when the input signal is present

### Transfer Characteristic

- ❑ There exists a range of input centered around zero where both  $Q_N$  and  $Q_P$  are off
- ❑ The transfer characteristic shows a dead band which results in the crossover distortion at the output



## Power Conversion Efficiency

- ❑ The average load power by neglecting the cross-over distortion is

$$P_L = \frac{1}{2} \frac{\widehat{V}_o^2}{R_L}$$

- ❑ The current drawn from each supply consists of half-sine waves of peak amplitude  $\widehat{V}_o / R_L$

- ❑ The average power drawn from each of the two power supply is

$$P_{S+} = P_{S-} = \frac{1}{\pi} \frac{\widehat{V}_o}{R_L} V_{CC}$$

- ❑ The total supply power is

$$P_S = \frac{2}{\pi} \frac{\widehat{V}_o}{R_L} V_{CC}$$

- ❑ The efficiency is given by

$$\eta = \frac{\pi}{4} \frac{\widehat{V}_o}{V_{CC}}$$

- ❑ Maximum efficiency is obtained when the output swing is maximized ( $\cong V_{CC}$ ):

$$\eta = \frac{\pi}{4} = 78.5\%$$

- ❑ The maximum average power available from a class B stage is

$$P_L = \frac{1}{2} \frac{\widehat{V}_o^2}{R_L}$$

## Power Dissipation

- ❑ The quiescent power dissipation of the class B stage is zero (unlike class A)
- ❑ The average power dissipation of the class B stage is given by  $P_D = P_S - P_L$

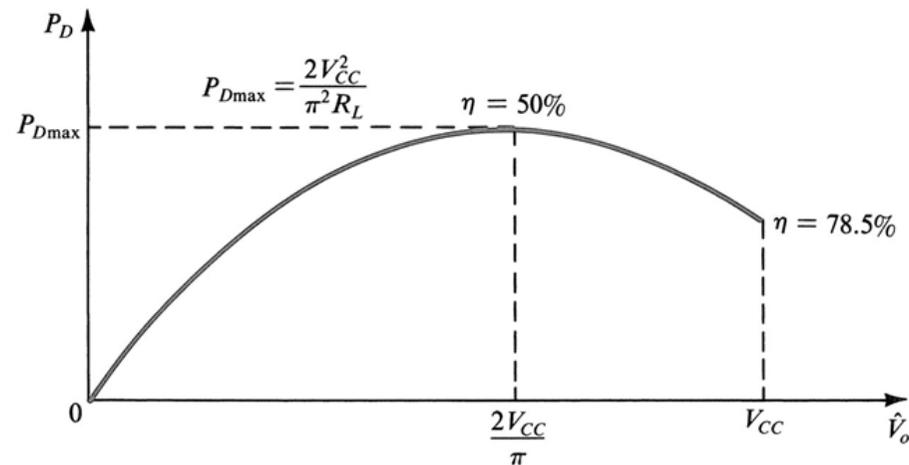
$$P_D = \frac{2 \hat{V}_o}{\pi R_L} V_{CC} - \frac{1 \hat{V}_o^2}{2 R_L}$$

- ❑  $Q_N$  and  $Q_P$  must be capable of safely dissipating half of  $P_D$
- ❑  $P_D$  depends on the output swing and the worst-case power dissipation is given by

$$\hat{V}_o|_{P_{D\max}} = \frac{2}{\pi} V_{CC} \rightarrow P_{D\max} = \frac{2 V_{CC}^2}{\pi R_L}$$

- ❑ The maximum power dissipation of  $Q_N$  and  $Q_P$  occurs at  $\eta = 50\%$ :

$$P_{DN\max} = P_{DP\max} = \frac{1}{\pi} \frac{V_{CC}^2}{R_L}$$

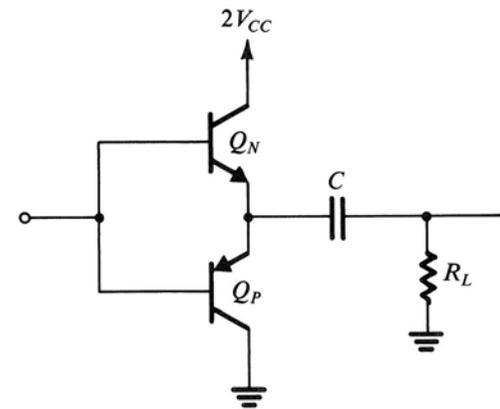
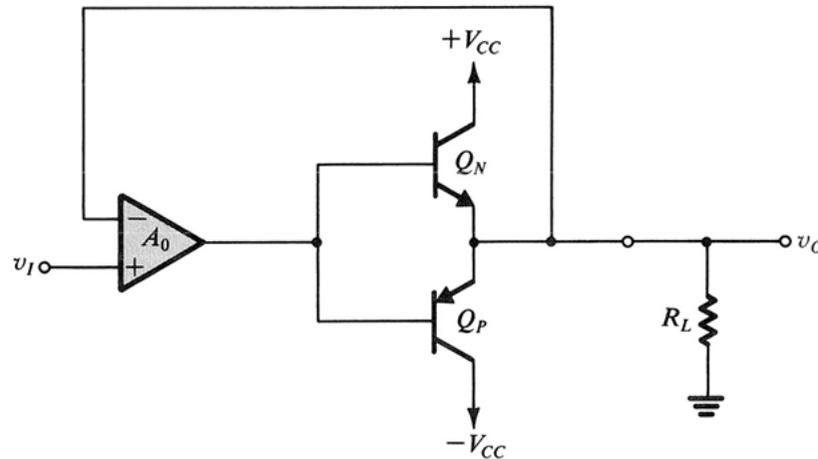


## Reducing Crossover Distortion

- ❑ The distortion can be reduced by employing a high-gain op amp and overall negative feedback
- ❑ The  $\pm 0.7\text{V}$  dead band is reduced by a factor of the dc gain of the op amp
- ❑ The slew rate limitation of the op amp may cause the alternate turning on and off to be noticeable

## Single-Supply Operation

- ❑ The class B stage can be operated from a single supply
- ❑ The load is capacitively coupled
- ❑ The derivations are directly applicable with supply of  $2V_{CC}$



## 13.4 CLASS AB OUTPUT STAGE

### Circuit Operation

❑ Cross-over distortion can be eliminated by biasing  $Q_N$  and  $Q_P$  at a small nonzero current

❑ The bias current  $i_N = i_P = I_Q = I_S \exp(V_{BB}/2V_T)$

❑ When  $v_I$  goes positive by a certain amount:

$$v_O = v_I + V_{BB}/2 - v_{BEN}$$

$$v_{BEN} + v_{BEP} = V_{BB}$$

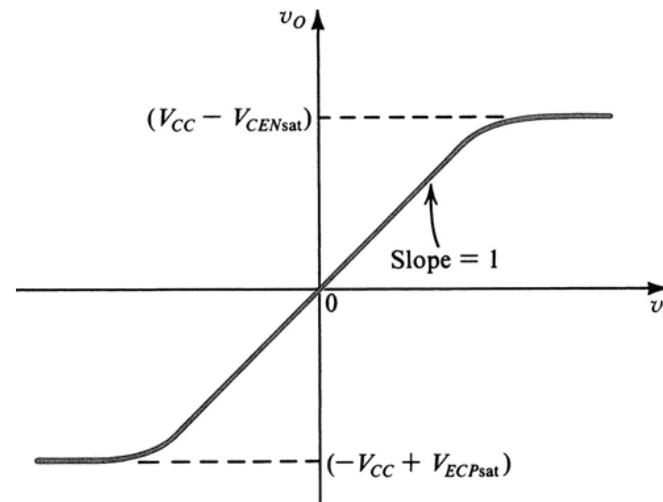
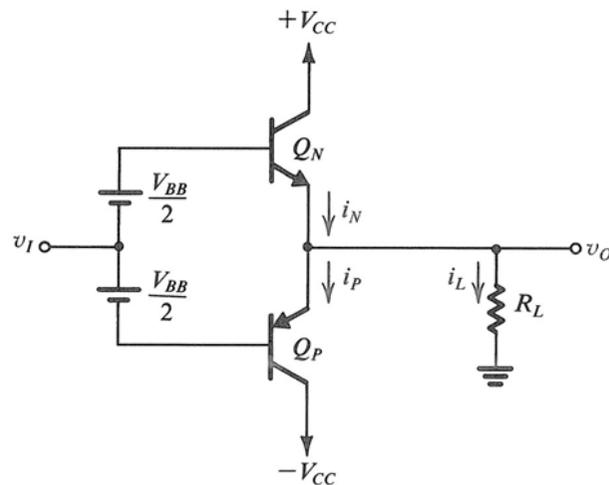
$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S} \rightarrow i_N i_P = I_Q^2 \rightarrow i_N^2 - i_N i_L - I_Q^2 = 0$$

■ The load current is supplied by  $Q_N$  which acts as the output emitter follower

■  $Q_P$  will be conducting a current that decreases as  $v_O$  increases (negligible for large  $v_O$ )

❑  $Q_P$  acts as the output emitter follower when  $v_I$  goes negative

❑ The power properties are almost identical to those derived for the class B stage

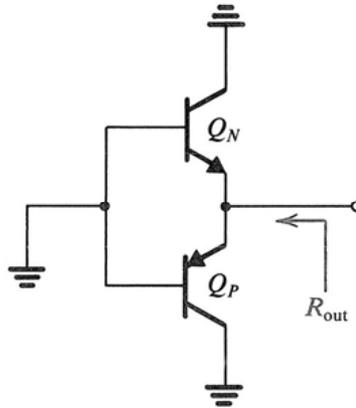


## Output Resistance

- ❑ The output resistance is estimated by assuming the source supply  $v_I$  ideal

$$R_{out} = r_{eN} \parallel r_{eP} = \frac{V_T}{i_N} \parallel \frac{V_T}{i_P} = \frac{V_T}{i_N + i_P}$$

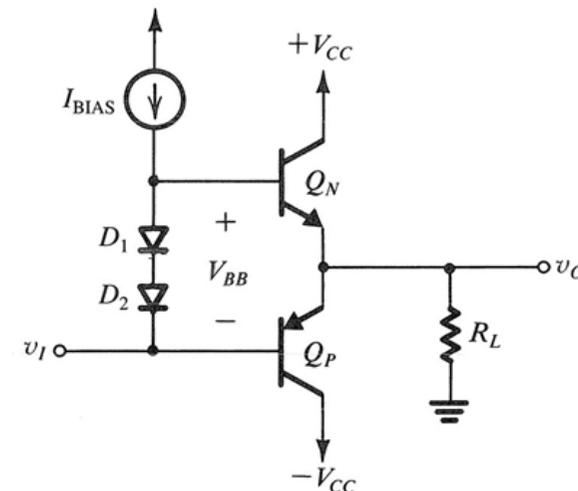
- ❑ The output resistance remains approximately constant in the region around  $v_I = 0$
- ❑ The output resistance decreases at larger load currents



## 13.5 BIASING THE CLASS AB CIRCUIT

### Biasing Using Diodes

- ❑ The bias voltage  $V_{BB}$  is generated by passing a constant current  $I_{BIAS}$  through a pair of diodes
- ❑ The diodes need not to be large devices
- ❑ Quiescent current  $I_Q$  in  $Q_N$  and  $Q_P$  will be  $I_Q = nI_{BIAS}$  where  $n$  is the ratio of the areas of the emitter junction of the BJT and the junction area of the diodes
- ❑  $I_{BN}$  increases from  $I_Q/\beta_N$  to  $I_L/\beta_N$  for a positive  $v_O$
- ❑  $I_{BIAS}$  has to be greater than the  $I_{BN}$  for maximum  $I_L$  case
- ❑ The ratio  $n$  cannot be a large number as  $n = I_Q/I_{BIAS}$
- ❑ This biasing arrangement provides thermal stabilization of the quiescent current in the output stage
  - Collector current increases with temperature for a fixed  $V_{BE}$
  - Heat from power dissipation increases with current
  - Positive feedback may cause thermal runaway
  - $V_{BB}$  decreases at the same rate of  $V_{BEN} + V_{EBP}$
  - Thermal runaway is alleviated with close thermal contact



## Biasing Using the Voltage Multiplier

- The class AB stage can be biased by  $V_{BE}$  multiplier

$$I_R = V_{BE1} / R_1$$

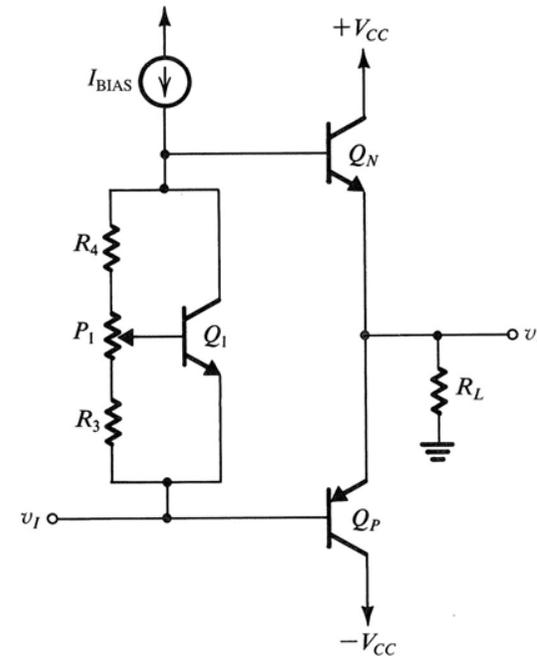
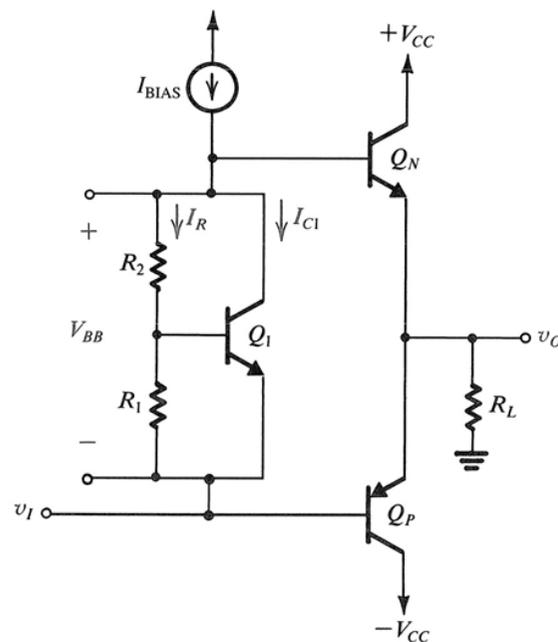
$$V_{BB} = V_{BE1} (1 + R_2 / R_1)$$

- The value of  $V_{BE1}$  is determined by the portion of  $I_{BIAS}$  that flows through the collector of  $Q_1$

$$I_{C1} = I_{BIAS} - I_R$$

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_S} = V_T \ln \frac{I_{C1}}{I_{BIAS} - I_R}$$

- The quiescent current can be adjusted by the resistance value



## 13.6 CMOS CLASS AB OUTPUT STAGES

### The Classical Configuration

- Circuit operation

$$V_{GG} = V_{GS1} + V_{SG2} = V_m + |V_{tp}| + \sqrt{2I_{BIAS}} \left( \frac{1}{\sqrt{k'_n(W/L)_1}} + \frac{1}{\sqrt{k'_p(W/L)_2}} \right)$$

$$V_{GG} = V_{GSN} + V_{SGP} = V_m + |V_{tp}| + \sqrt{2I_Q} \left( \frac{1}{\sqrt{k'_n(W/L)_n}} + \frac{1}{\sqrt{k'_p(W/L)_p}} \right)$$

$$I_Q = I_{BIAS} \left( \frac{1/\sqrt{k'_n(W/L)_1}}{1/\sqrt{k'_n(W/L)_n}} + \frac{1/\sqrt{k'_p(W/L)_2}}{1/\sqrt{k'_p(W/L)_p}} \right)^2$$

- For the case  $Q_1$  and  $Q_2$  are matched and  $Q_P$  and  $Q_N$  are matched:

$$I_Q = I_{BIAS} \frac{(W/L)_n}{(W/L)_1}$$

- A drawback of the CMOS class AB circuit is the restricted range of output voltage swing

$$v_{Omax} = V_{DD} - V_{OV|BIAS} - V_m - v_{OVN}$$

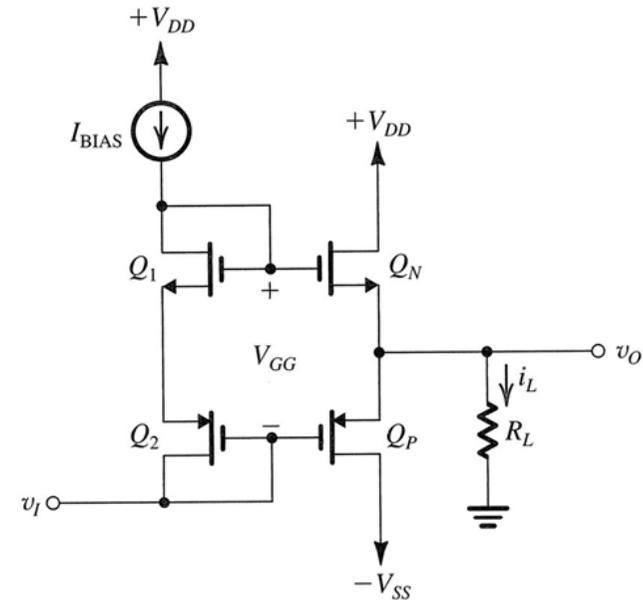
$$v_{Omin} = -V_{SS} + V_{OV|I} + |V_{tp}| + |v_{OVP}|$$

where

$v_{OVN}$  is the overdrive voltage of  $Q_N$  when it is supplying  $i_{Lmax}$

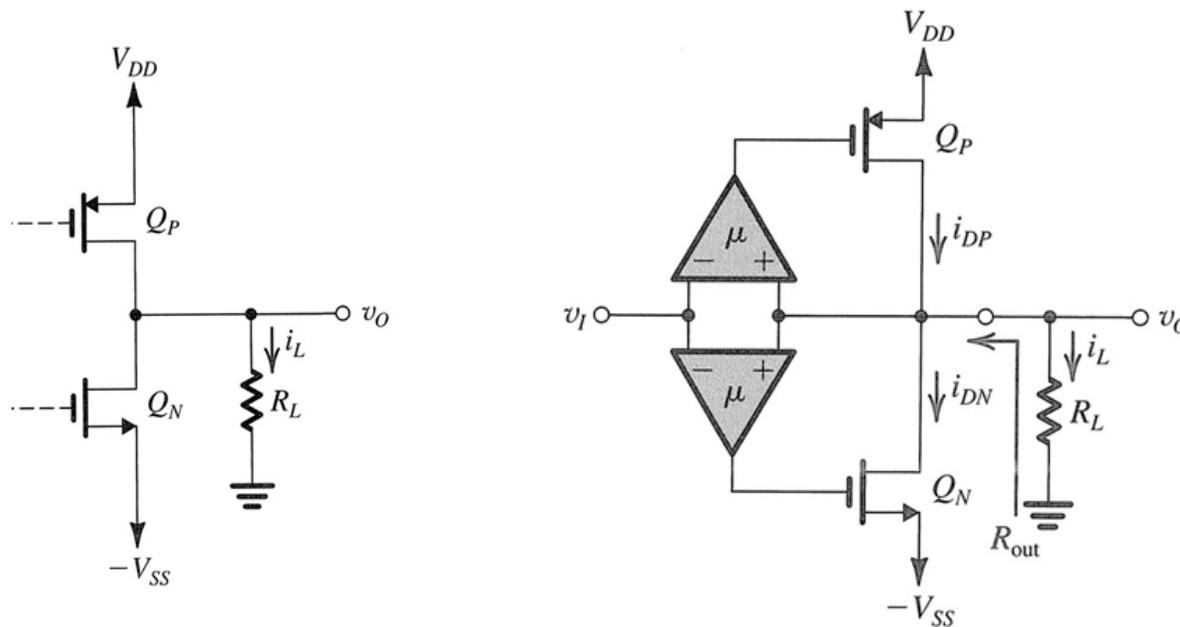
and

$|v_{OVP}|$  is the overdrive voltage of  $Q_P$  when sinking the maximum negative value of  $i_L$



## An Alternative Circuit Using Common-Source Transistors

- ❑ The allowable output range can be increased by replacing the source followers with a pair of complementary transistors in the common-source configuration
- ❑  $Q_P$  supplies the load current when  $v_O$  is positive, allowing an output as high as  $V_{DD} - |v_{OVLP}|$
- ❑  $Q_N$  sinks the load current when  $v_O$  is negative, allowing an output as low as  $-V_{SS} + v_{OVN}$
- ❑ The disadvantage is its high output resistance  $R_{out} = r_{on} || r_{op}$
- ❑ Negative feedback (**error amplifiers**) is employed to reduce the output resistance

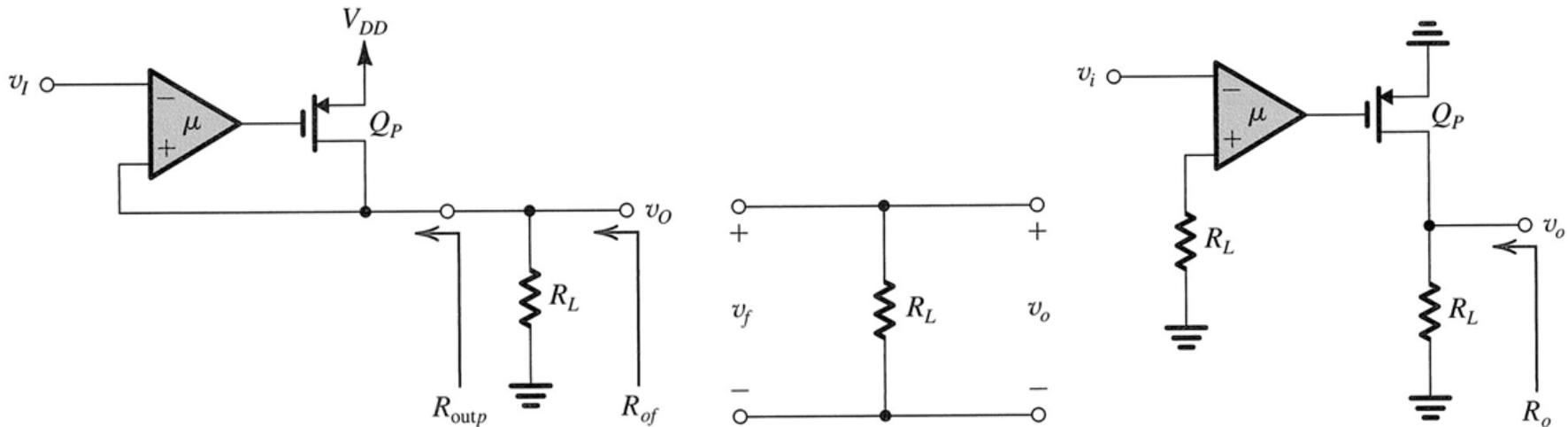


## Output Resistance

- ❑ The output resistance is derived by two half circuits:  $R_{out} = R_{outn} \parallel R_{outp}$
- ❑ The analysis techniques for feedback (shunt-series feedback) is utilized:

$$\beta = 1 \quad \text{and} \quad A \equiv \frac{v_o}{v_i} = \mu g_{mp} (r_{op} \parallel R_L)$$

- ❑ The open-loop output resistance:  $R_o = R_L \parallel r_{op}$
- ❑ The output resistance with feedback:  $R_{of} = R_o / (1 + \beta A) = (R_L \parallel r_{op}) / [1 + \mu g_m (R_L \parallel r_{op})]$
- ❑ The output resistance excluding  $R_L$ :  $R_{outp} = 1 / (1 / R_{of} - 1 / R_L) = r_{op} \parallel \frac{1}{\mu g_{mp}} \approx \frac{1}{\mu g_{mp}}$
- ❑ Overall output resistance:  $R_{out} \approx 1 / \mu (g_{mp} + g_{mn})$



## The Voltage Transfer Characteristics

- ❑ For the case where  $Q_N$  and  $Q_P$  are matched:  $I_Q = \frac{1}{2}kV_{OV}^2$
- ❑ Drain currents:  $i_{DN} = I_Q \left(1 + \mu \frac{v_O - v_I}{V_{OV}}\right)^2$  and  $i_{DP} = I_Q \left(1 - \mu \frac{v_O - v_I}{V_{OV}}\right)^2$
- ❑ Load current:  $i_L = i_{DP} - i_{DN}$
- ❑ Output voltage:  $v_O = v_I / \left(1 + \frac{V_{OV}}{4\mu I_Q R_L}\right) \approx v_I \left(1 - \frac{V_{OV}}{4\mu I_Q R_L}\right)$
- ❑ Gain error:  $v_O - v_I = -\frac{V_{OV}}{4\mu I_Q R_L} = -\frac{V_{OV}}{2\mu g_m R_L}$

