UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Homework #1 Solutions** **EECS 240**
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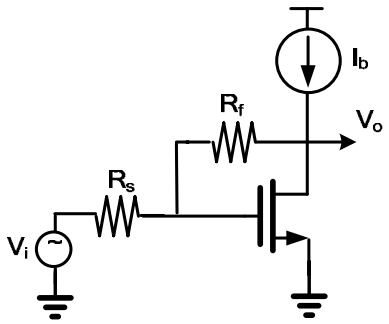
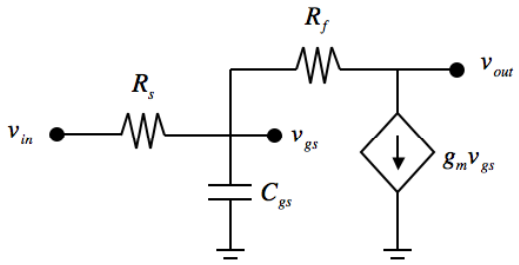
Use the EECS240 90nm CMOS process in all homeworks and projects unless otherwise noted. The SPICE model and instructions for running the simulator are available on the course website.

1. As a brief review of some of the basic analysis you learned in EE140, in this problem we will analyze the simple amplifier circuit shown below. You can assume that the small signal output resistance (r_o) of the transistor is infinite, and that the only parasitic capacitance associated with the transistor is its C_{gs}.



a. Draw the small signal model of this amplifier.

Solution:



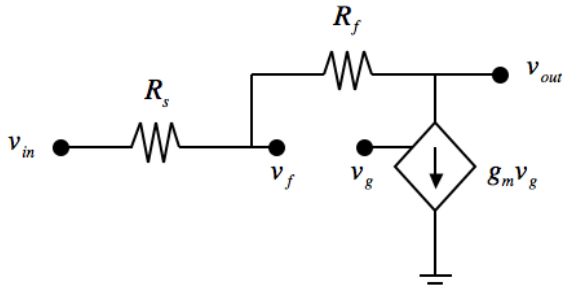
b. As a function of the transistor's g_m and the resistor values R_s and R_f, what is the small signal gain (V_o/V_i) of the amplifier?

Solution:

There are obviously an infinite number of methods you can use to solve this problem. We will describe a method based on feedback analysis below, but any correct approach will receive full credit.

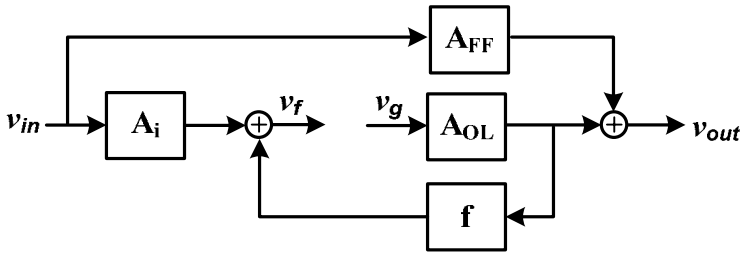
Using feedback analysis:

To find the gain terms we will use in a feedback block diagram analysis we first break the loop at the gate of the transistor to the right of the resistances:



Having broken the feedback at the gate, there are two key things to realize about this circuit: first, that there is a direct path from the input to the output independent of the amplifier itself, and second, that the input of the circuit (v_{in}) is not necessarily identical to the feedback input (v_f).

Using these two observations, we can represent the circuit with the following block diagram:



Here, A_{FF} represents the feedforward gain directly from v_{in} to v_{out}, A_i is the gain from v_{in} to v_f, A_{OL} is the open-loop voltage gain of the amplifier, and f is the feedback gain. Note that as implied by the block diagram, all of these gains are open-loop quantities, so when we evaluate them we can short out the other "input" (i.e., either v_g or v_{in}) that doesn't impact that part of the block diagram.

Let's start with the open-loop gain of the amplifier. With the input grounded we basically just have a common-source device with a resistive load, so:

$$A_{OL} = \frac{v_{out}}{v_g} = -g_m(R_f + R_s)$$

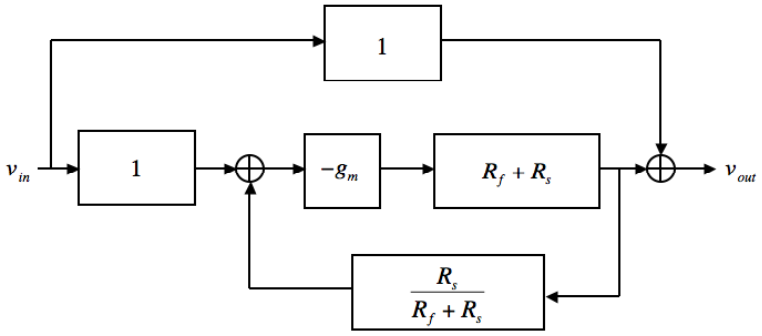
Similarly, the feedback gain is:

$$f = \frac{v_f}{v_o} = \frac{R_s}{R_s + R_f}$$

Now all we need to do is find the feedforward gain and relationship between v_f and v_{in}. For both of these we can ground v_g, so we're basically left with only the two resistors in series driving an open circuit (at least from a DC standpoint – we'll come back to the AC behavior in part c). Therefore:

$$A_i = \frac{v_f}{v_{in}} = 1 \text{ and } A_{FF} = \frac{v_{out}}{v_{in}} = 1$$

Plugging these gains back in to the block diagram:



Now the block diagram can be reduced using Black's formula:

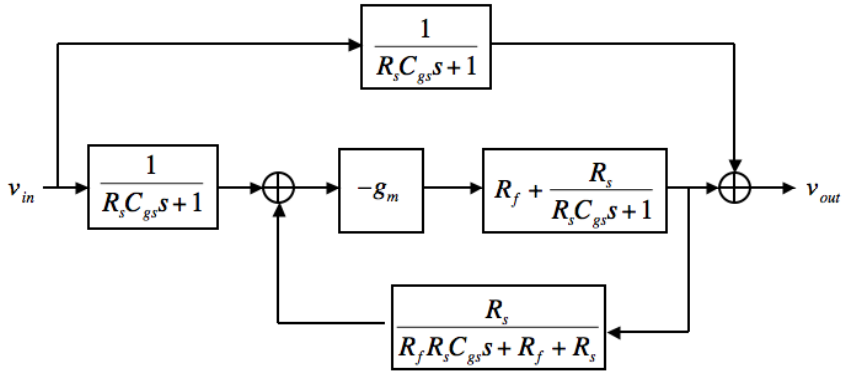
$$\frac{v_{out}}{v_{in}} = \frac{-g_m(R_f + R_s)}{1 + g_m(R_f + R_s)\left(\frac{R_s}{R_f + R_s}\right)} + 1 = \frac{-g_m(R_f + R_s)}{1 + g_m R_s} + 1$$

$$\frac{v_{out}}{v_{in}} = \frac{-g_m(R_f + R_s) + 1 + g_m R_s}{1 + g_m R_s} = \frac{1 - g_m R_f}{1 + g_m R_s}$$

c. What is the 3dB bandwidth of this amplifier?

Solution:

We can follow the exact same procedure we used in part b) to include the effect of Cgs; the resulting block diagram is:



$$\frac{v_{out}}{v_{in}} = \frac{-g_m\left(R_f + \frac{R_s}{R_s C_{gs} s + 1}\right)}{1 + g_m\left(R_f + \frac{R_s}{R_s C_{gs} s + 1}\right)\left(\frac{R_s}{R_f R_s C_{gs} s + R_f + R_s}\right)} \frac{1}{R_s C_{gs} s + 1} + \frac{1}{R_s C_{gs} s + 1}$$

$$= \frac{-g_m(R_f R_s C_{gs} s + R_f + R_s)}{R_s C_{gs} s + 1 + g_m R_s} \frac{1}{R_s C_{gs} s + 1} + \frac{1}{R_s C_{gs} s + 1}$$

$$= \frac{-g_m(R_f R_s C_{gs} s + R_f + R_s) + (R_s C_{gs} s + 1 + g_m R_s)}{(R_s C_{gs} s + 1 + g_m R_s)(R_s C_{gs} s + 1)}$$

$$= \frac{-g_m(R_f R_s C_{gs} s + R_f) + (R_s C_{gs} s + 1)}{(R_s C_{gs} s + 1 + g_m R_s)(R_s C_{gs} s + 1)} = \frac{-g_m R_f (R_s C_{gs} s + 1) + (R_s C_{gs} s + 1)}{(R_s C_{gs} s + 1 + g_m R_s)(R_s C_{gs} s + 1)}$$

$$= \frac{-g_m R_f + 1}{R_s C_{gs} s + 1 + g_m R_s}$$

Of course, the -3dB bandwidth is just the pole of the first-order transfer function:

$$f_{-3dB} = \frac{1 + g_m R_s}{2\pi R_s C_{gs}} \approx \frac{g_m}{2\pi C_{gs}}$$

As an alternative (and in this case easier) method, since this circuit has only one capacitor in it, we can find the 3dB bandwidth simply by calculating the resistance seen by C_{gs} with the input grounded. Looking at the small signal model from part a), this resistance is just $R_s||(1/g_m)$, leading to exactly the same 3dB bandwidth.

2. In this problem we will look at the design of MOM capacitors in our 7-level metal process. Unless otherwise noted, you should assume that all metal layers have a thickness T = 0.2μm, minimum width W = 0.14μm, minimum horizontal spacing S = 0.14μm, vertical spacing H = 0.2μm, and that the insulator is SiO_2. You can assume that the separation of the lowest layer of metal from the substrate is also H = 0.2μm, and that the inter-layer vias have the same width as the wires they are connected to. For simplicity, you can ignore fringing fields in all of these calculations.

   a. What is the maximum capacitance density (in $fF/\mu m^2$) you can achieve with a simple horizontal parallel plate? What is the ratio of capacitance to bottom plate parasitic?

   Solution:

   Define N as the number of layers (7 in our case).
   $C_{HPP} = (N-1)\varepsilon_{ox}/H = (6 \cdot 3.9 \cdot 8.85pF/m)/0.2\mu m = 1.035 fF/\mu m^2$
   $C_{bot,HPP} = \varepsilon_{ox}/H$
   $C_{HPP}/C_{bot,HPP} = 6$

   b. What is the maximum capacitance density (still in $fF/\mu m^2$) you can achieve with a vertical parallel plate? Now what is the ratio of capacitance to bottom plate parasitic?

   Solution:

   $$C_{VPP} = \varepsilon_{ox} \frac{NT + (N-1)H}{S(W+S)} = 3.9 \cdot 8.85\, pF/m * \frac{7 \cdot 0.2\mu m + 6 \cdot 0.2\mu m}{0.14\mu m(0.14\mu m + 0.14\mu m)} = 2.289\, fF/\mu m^2$$

   $$C_{bot,VPP} = \varepsilon_{ox} \frac{W}{H(W+S)} = 3.9 \cdot 8.85\, pF/m * \frac{0.14\mu m}{0.2\mu m(0.14\mu m + 0.14\mu m)} = .0863\, fF/\mu m^2$$

   $C_{VPP}/C_{bot,VPP} = 26.53$

   c. In some processes, placing an inter-layer via requires the metal line to be wider than the minimum allowed. For this problem, let's assume that a metal line with a via must be at least 0.21μm wide. In this case (and still ignoring fringing fields), what structure gives you the highest capacitance density, and what is that density?

   Solution:

   Let us compare the new vertical structure, and a "hybrid" capacitor like the one described in lecture that uses no vias (hence allowing minimal width) but alternates the terminals of the capacitor in both the vertical and horizontal directions in order to use both of those fields.

   First, let's recalculate the density of the vertical parallel plate with the wider metal lines:

   $$C_{VPP} = \varepsilon_{ox} \frac{NT + (N-1)H}{S(W+S)} = 3.9 \cdot 8.85\, pF/m * \frac{7 \cdot 0.2\mu m + 6 \cdot 0.2\mu m}{0.14\mu m(0.21\mu m + 0.14\mu m)} = 1.831\, fF/\mu m^2$$

   The hybrid capacitor has a density of:

   $$C_{hyb} = \varepsilon_{ox}\left(\frac{NT/S}{(W+S)} + \frac{(N-1)W/H}{(W+S)}\right) = 3.9 \cdot 8.85\, pF/m * \frac{7 \cdot 0.2/0.14 + 6 \cdot 0.14/0.2}{0.14\mu m + 0.14\mu m} = 1.75\, fF/\mu m^2$$

Note that although our simplified calculation seems to indicate that the pure vertical parallel plate with the wider metal lines has slightly higher density than the hybrid structure, if we were to include fringing fields the hybrid structure would almost certainly have higher density.

3. In this problem you will need to run HSPICE (or whatever your favorite simulator is). For some of the problems you should access internal device parameters such as g_m or V_{TH} – in HSPICE, you can access these with a statement like:

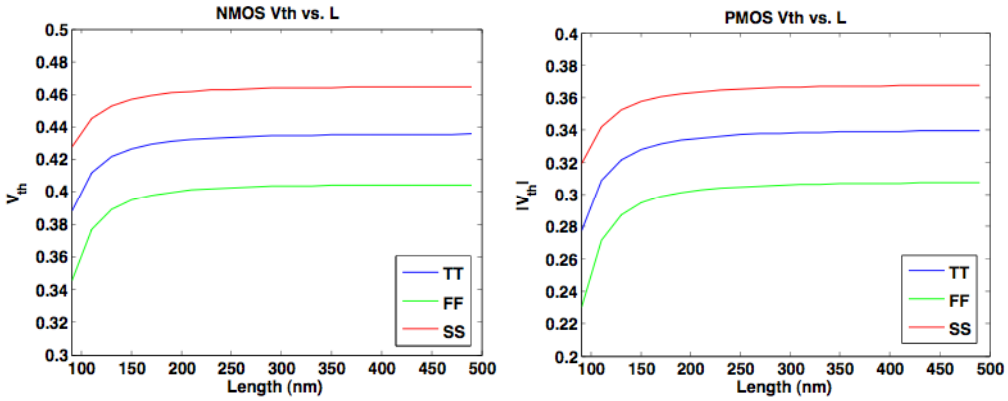
   .print m1_vth=par('lv9(m1)')

   (You can find the names of the various transistor parameters you might want to look at in the HSPICE manual, which can be accessed from the instructional machines – see the link on the course website.)

   For this problem, you should plot the results for all of the process corners provided in the library (i.e. *SS, TT, FF*). Unless otherwise specified, use minimum length transistors with $W=1\mu m$ and a maximum $|V_{GS}|$ and $|V_{DS}|$ of 1.2V.

   a. Plot the magnitude of the threshold voltage of an NFET and PFET as a function of channel length *L*. You should sweep *L* from 90nm to 500nm – be sure to use a step size small enough to measure a smooth curve.

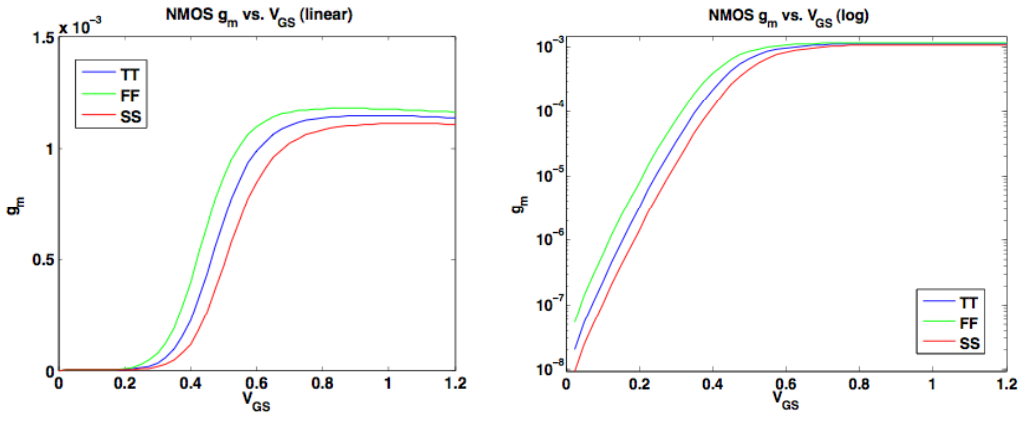
   Solution:



   Note that you may get a different shape for this curve depending on the V_{ds} you applied to the transistor – at lower Vds, the drop in threshold voltage at lower L is less pronounced.

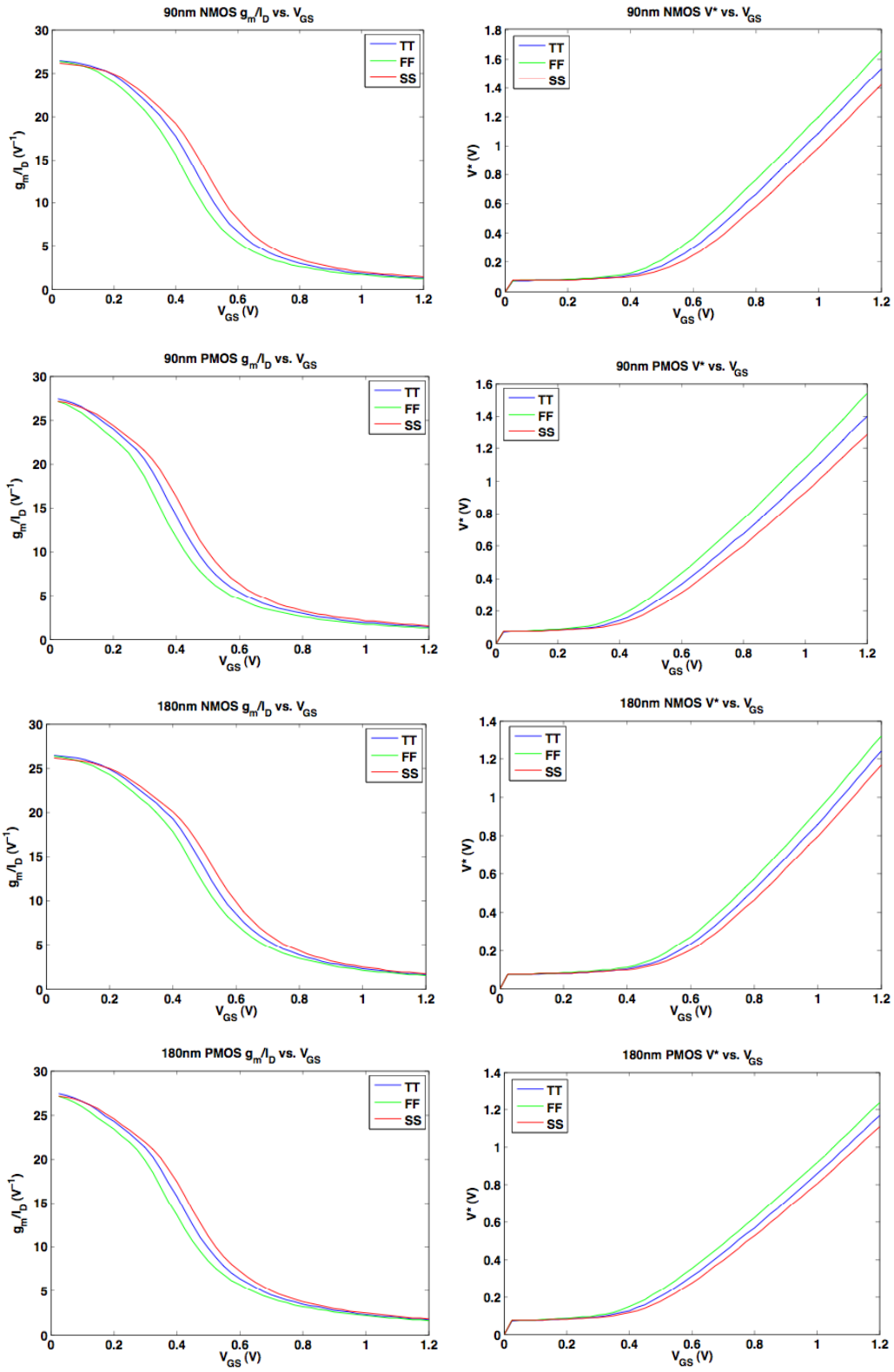
   b. Plot the g_m versus V_{GS} of an NFET on a linear and log scale, biasing the transistor with $V_{GS} = V_{DS}$.

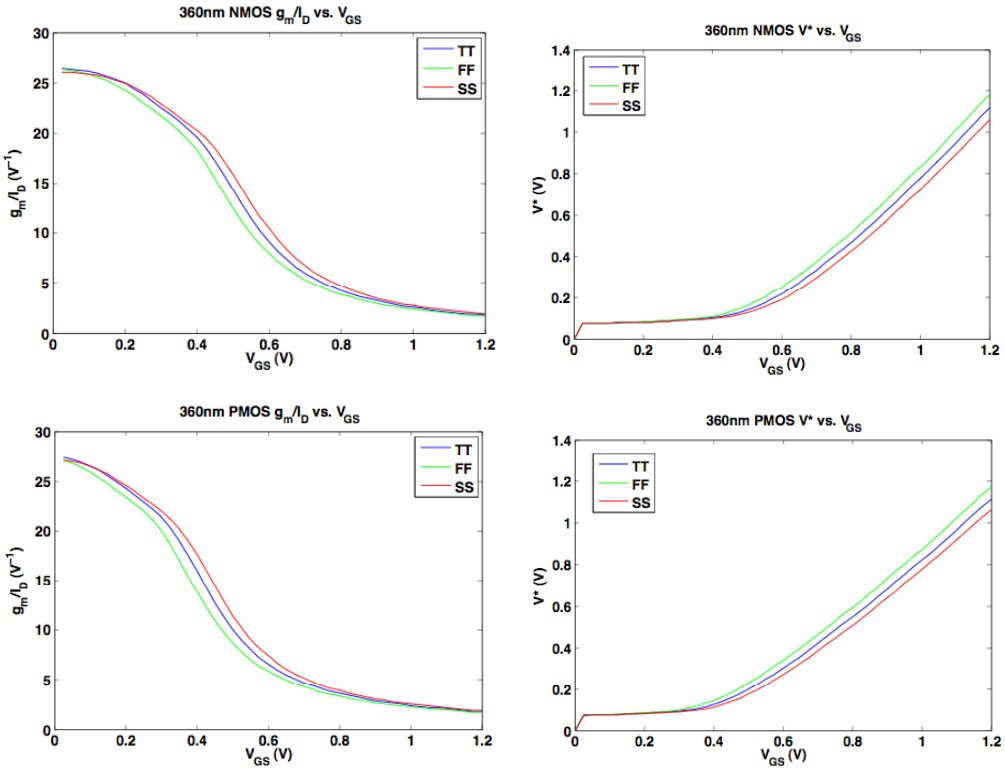
   Solution:



c. Plot g_m/I_D as a function of $|V_{GS}|$ (still with $V_{GS} = V_{DS}$) for an NFET and PFET with L=90nm, 180nm, and 360nm. Then, use this data to plot $V^* = 2I_D/g_m$ as a function of $|V_{GS}|$.

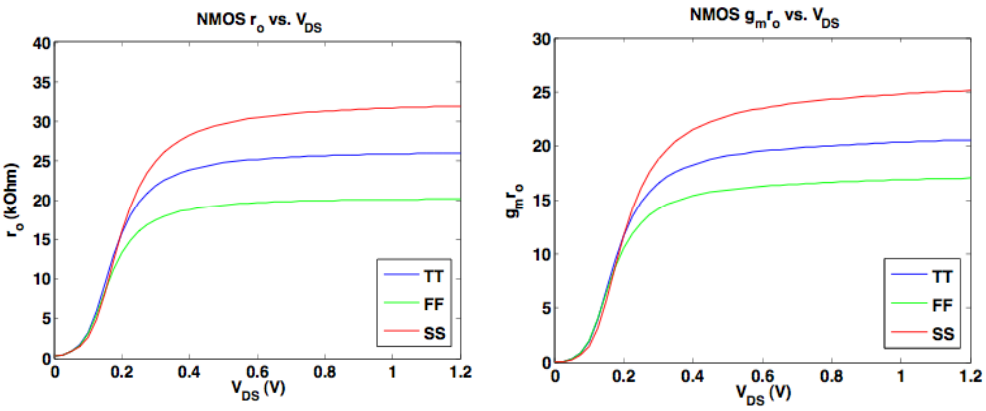
Solution:



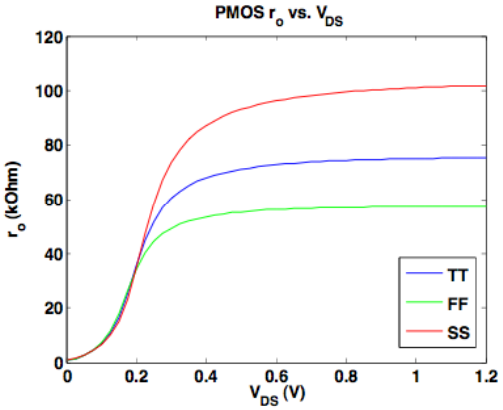


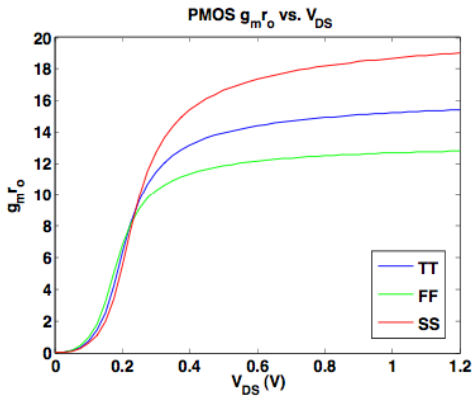
d. Plot the output resistance r_o and DC gain $g_m r_o$ versus V_{DS} for an NFET and PFET. You should bias the transistors with $V^* = 200\text{mV}$. What is the allowed output swing to maintain a DC gain of 80% of the peak value?

Solution:



To maintain a V* of 200mV the bias currents used were: TT,SS: I=77.3µA, FF: I=83.1µA





To maintain a V* of 200mV the bias currents used were: TT,SS,FF: I=18.5µA

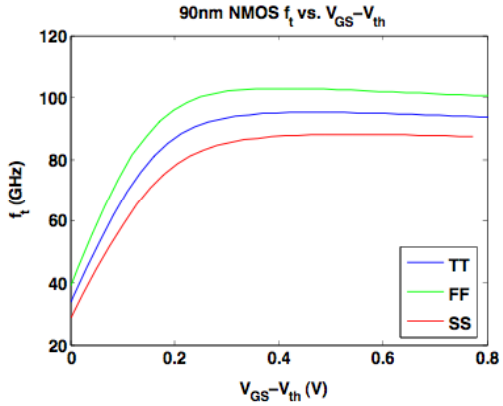
The NMOS device can handle ~0.9V of swing and the PMOS device can handle ~0.85V of swing while maintaining gain within 80% of its peak value.

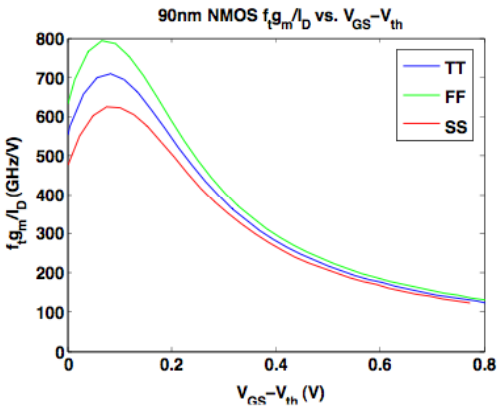
Note that for these devices SCBE isn't apparent over the range of voltage you'd normally operate the device, but if you increased $|V_{ds}|$ up to ~1.8-2V you will see that the model does include the effect.

e. Plot f_T and $f_T \cdot (g_m/I_D)$ as a function of $|V_{GS}-V_T|$ for L=90nm, 180nm, and 360nm. You should set $V_{DS} = V_{GS}$ and vary $|V_{GS}-V_T|$ from 0 to 500mV. What is the V^* that achieves the maximum $f_T \cdot (g_m/I_D)$ for each channel length?.

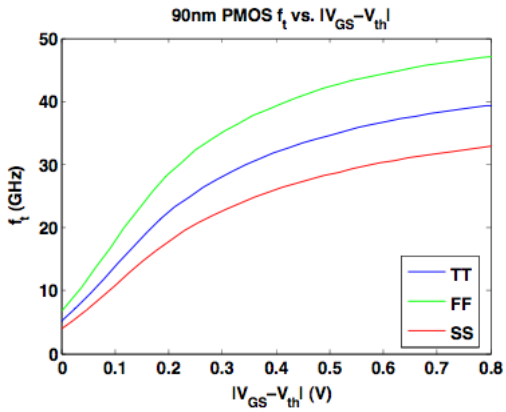
Solution:

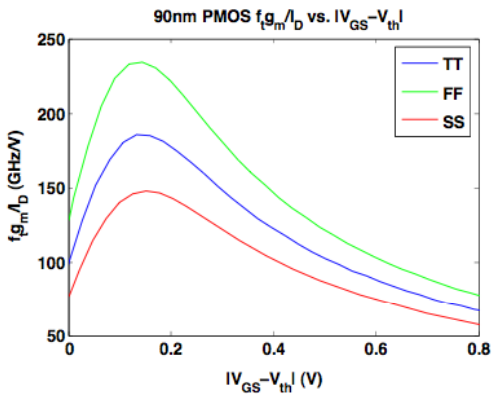
The simulations were performed with a .dc sweep of V_{gs} with V_{ds} = 1.2V. f_T was extracted using gm (lx7) divided by C_{gg} (lx82), which gives all gate capacitance. If you used lx18 it does not include overlap capacitance, and therefore is off by a factor of ~2. Also don't forget to divide by 2π!



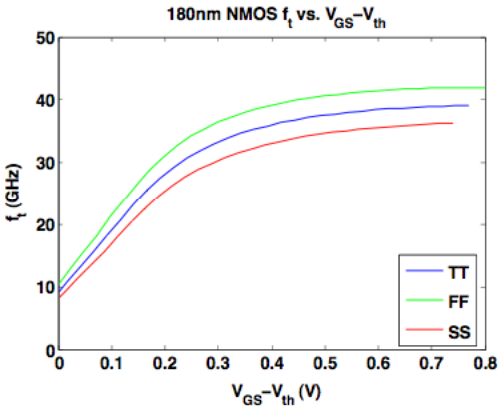


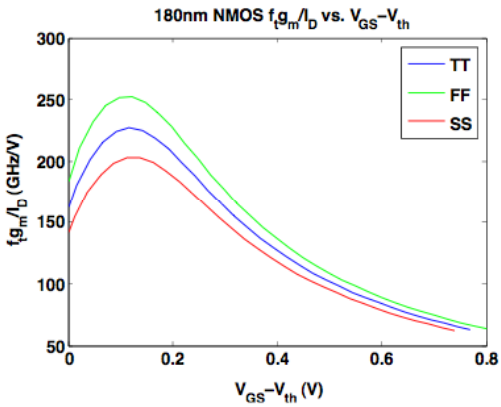
90nm NMOS peak $f_t g_m/I_D$: V* ~ 80mV



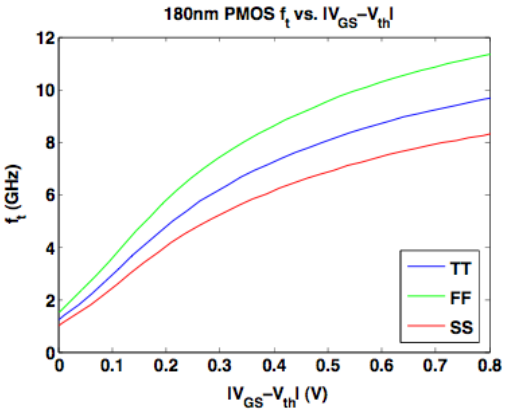


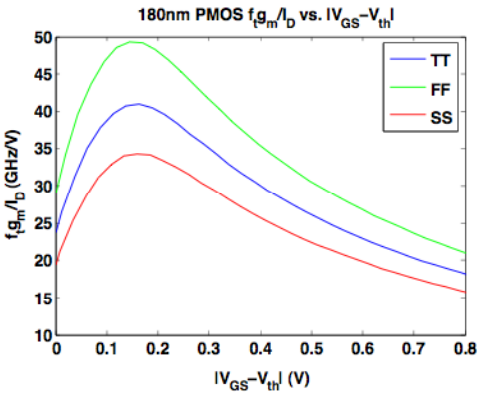
90nm PMOS peak $f_t g_m/I_D$: V* ~ 145mV



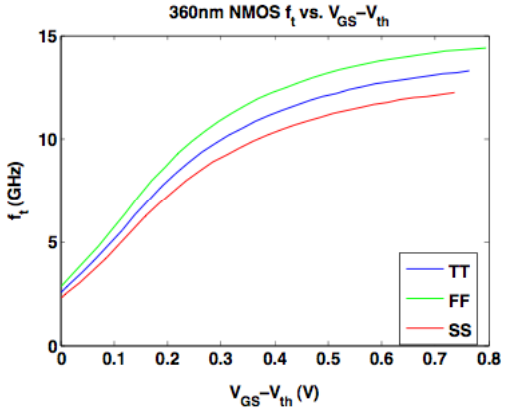


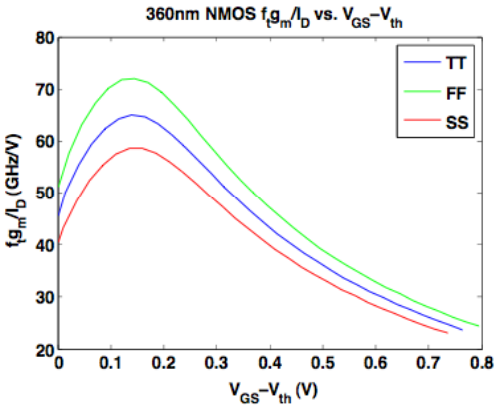
180nm NMOS peak $f_t g_m/I_D$: TT: V* ~ 115mV



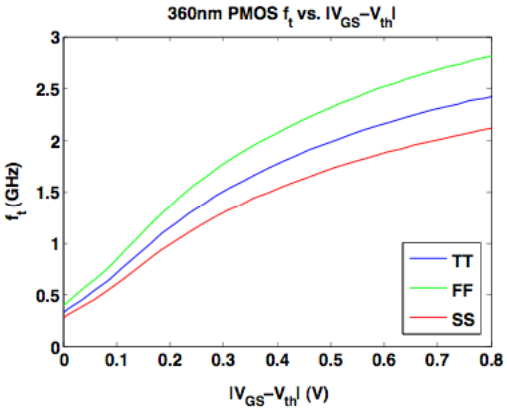


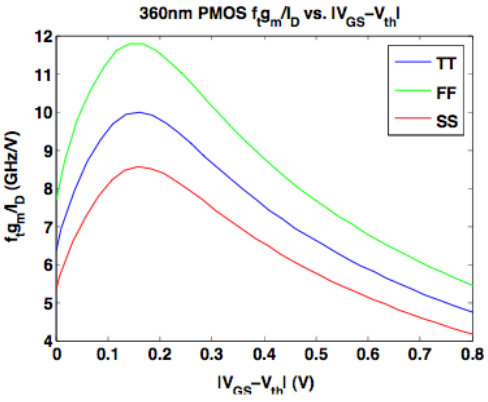
180nm PMOS peak $f_t g_m/I_D$: V* ~ 160mV





360nm NMOS peak f_tg_m/I_D: V* ~ 140mV





360nm PMOS peak f_tg_m/I_D: V* ~ 160mV