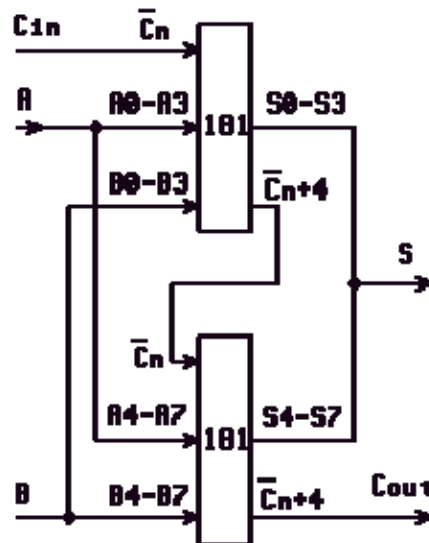


A microprocessor architecture

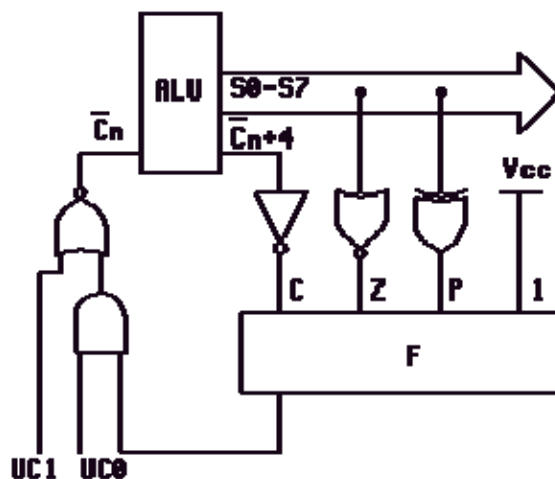
Basic 8 bit microprocessor

4.1.4 Arithmetic and Logic Unit (circuit U)

The arithmetic logic unit will consist of two circuits **74 LS 181** in cascade:



- The selected input C_n is obtained by means of the signal C derived from F and may be forced to either 0 or 1 with the aid of the signals UA_1 and CPU_0 :



UC_1	UC_0	C_n	note
0	0	1	Carry = 0
0	1	C_{n+4}	Carry = C
1	X	0	Carry = 1

- We call UM , $U.S.$ $_{3-0}$ control signals for the selection of the operation performed by the ALU. The following combinations will be:

Logical Operations			
UC	UM	U.S.	S
X	1	0	A^{-} (NOT)
X	1	1	$(A + B)^{-}$ (NOR)
X	1	3	0
X	1	4	$(AB)^{-}$ (NAND)
X	1	6	$A [+] B$ (XOR)
X	1	9	$(A [+] B)^{-}$ (NXOR)
X	1	B	AB (AND)
X	1	C	1
X	1	E	$A + B$ (OR)
X	1	F	A

Arithmetic			
UC	UM	U.S.	S
0	0	F	A-1
2	0	0	A +1
0	0	C	A + A
1	0	C	$A + A + C$
2	0	C	$A + A + 1$
0	0	9	A + B
1	0	9	$A + B + C$
2	0	9	$A + B + 1$
0	0	6	AB-1
1	0	6	$AB-1 + C$
2	0	6	AB

For logical operations will be taken $UC = 0$.