# Regular Correspondence

## Design Procedures for a Fully Differential Folded-Cascode CMOS Operational Amplifier

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*Abstract* — **A fully differential folded-cascode op amp is analyzed and the results are presented in the form of design equations and procedures. Trade-offs among such factors as bandwidth, gain, phase margin, bias currents, signal swing, slew rate, and power are made evident. Closed-form expressions are developed and a sequence of design steps is established. A graphical representation of the relationships among the gain, power, and phase margin for different capacitive loadings is presented to visually illustrate one form of design optimization. The results of SPICE simulations are shown to agree very well with the use of our design equations.**

### I. Introduction

This paper addresses the need for relatively inexperienced analog integrated circuit designers to be able to come up with reasonably efficient designs for complex analog building blocks such as the fully differential folded-cascode amplifier [1], [2]. An attempt is made to formalize the design of a fully differential folded-cascode amplifier for switched-capacitor applications by establishing design equations and procedures to assist in this process. In order to tailor the op amp to a particular application, it has to satisfy conditions on the gain, stability, bandwidth, slew rate, noise, etc. [3]. These conditions often conflict with one another, and are also very sensitive to process variations. The procedures outlined in this paper give an indication of how to efficiently satisfy these performance requirements, and at the same time ensure sufficient safety margins.

### II. Theoretical Analysis of the Fully Differential Folded-Cascode Amplifier

This section analyzes the frequency response of the fully differential folded-cascode amplifier proposed in [4]. The analysis will be useful in the formulation of the design equations outlined in Section III. The circuit schematic of the op amp is shown in Fig. 1. $M1$ and $M2$ are the input driver transistors, and $M6$ and $M7$ form the folded-cascode transistors. The common-mode feedback (CMFB) is achieved by controlling the bias voltages of $M4$ and $M5$. In the CMFB circuit comprising $M12$–$M19$, two differential pairs ($M14$, $M15$ and $M16$, $M17$) sum their differential currents into a current-mirror load $M18$, $M19$ with the output taken from $M18$. The common-mode voltage is held at a reference potential $V_{cm}$ which is usually analog ground in order to maximize output signal swing.

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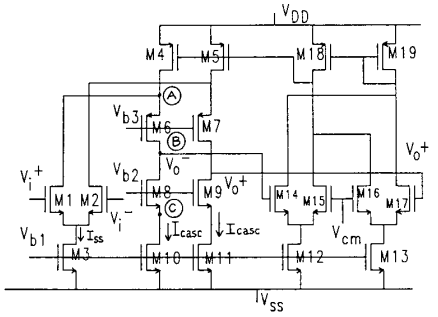


Fig. 1. Fully differential folded-cascode amplifier (after [4]).

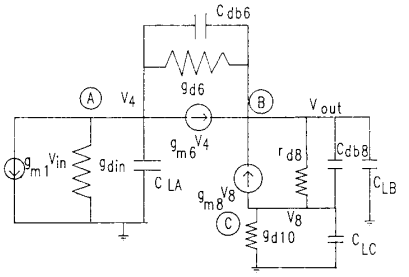


Fig. 2. High-frequency differential half equivalent circuit of the folded-cascode amplifier.

The frequency response of the op amp can be derived from its high-frequency differential half equivalent circuit shown in Fig. 2. The capacitances $C_{LA}$, $C_{LB}$, and $C_{LC}$ represent the total capacitances at nodes $A$, $B$, and $C$ respectively. These capacitances are related to the device capacitances by the following equations:

$$C_{LA} = C_{gd4} + C_{db4} + C_{db1} + C_{gs6} + C_{gb6} + C_{gd1} \quad (1)$$

$$C_{LB} = C_{gd8} + C_{gd6} + C_{gb14} + C_{gs14} + C_{gd14} + C_L \quad (2)$$

$$C_{LC} = C_{db10} + C_{gd10} + C_{gs8} + C_{gb8} \quad (3)$$

where $C_L$ is the external load capacitance at the output terminal, and the other capacitive terms have their usual meanings. For greater accuracy, the contribution from the source-to-substrate capacitances may be added to these terms.

Solving for the node equations and assuming that the $g_m$'s are much larger than the $g_d$'s, the transfer function of the circuit can be approximated as

$$A_d = -\frac{g_{m1}g_{m6}g_{m8}\left(1+\frac{sC_{db6}}{g_{m6}}\right)\left(1+\frac{s(C_{LC}+C_{db8})}{g_{m8}}\right)}{P_1(s)+P_2(s)} \quad (4)$$

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where

$$P_1(s) = g_{d8} g_{d10} g_{m6} \left(1 + \frac{sC_{db8}}{g_{d8}}\right)\left(1 + \frac{sC_{LC}}{g_{d10}}\right)\left(1 + \frac{s(C_{LA} + C_{db6})}{g_{m6}}\right) \tag{5}$$

$$P_2(s) = g_{din} g_{d6} g_{m8} \left(1 + \frac{sC_{LA}}{g_{in}}\right)\left(1 + \frac{sC_{LC}}{g_{m8}}\right)\left(1 + \frac{s(C_{LB} + C_{db6})}{g_{d6}}\right). \tag{6}$$

To determine the poles of the transfer function, it is first expressed in the general form shown below:

$$A_d(s) = \frac{A_0\left(1 - \frac{s}{z_1}\right)\left(1 - \frac{s}{z_2}\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)\left(1 - \frac{s}{p_3}\right)} \tag{7}$$

where $A_0$ is the small-signal dc gain of the amplifier given by

$$A_0 = -\frac{g_{m1}}{\frac{g_{d8} g_{d10}}{g_{m8}} + \frac{(g_{d1} + g_{d4}) g_{d6}}{g_{m6}}}. \tag{8}$$

The denominator can be written as a cubic equation of the form:

$$1 - s\left(\frac{1}{p_1} + \frac{1}{p_2} + \frac{1}{p_3}\right) + s^2\left(\frac{1}{p_1 p_2} + \frac{1}{p_2 p_3} + \frac{1}{p_1 p_3}\right) - s^3\left(\frac{1}{p_1 p_2 p_3}\right). \tag{9}$$

If the circuit is designed so as to have a dominant pole $p_1 \ll p_2, p_3$, the above equation can be written as

$$1 - \frac{s}{p_1} + s^2\left[\frac{1}{p_1}\left(\frac{1}{p_2} + \frac{1}{p_3}\right)\right] - \frac{s^3}{p_1 p_2 p_3} = 0. \tag{10}$$

After manipulating the denominator of (4) and equating the $s$ terms in (4) and (10), the following relations are obtained: the dominant pole is given by

$$p_1 = -\frac{1}{R_0 C_{L2}} \tag{11}$$

and the nondominant poles are given by

$$p_2 = -\frac{g_{m6}}{C_{L1}}, \quad p_3 = \frac{g_{m8}}{C_{L3}}. \tag{12}$$

Since there is a zero at approximately $-g_{m8}/C_{L3}$, the effect of $p_3$ is canceled out. $C_{L1}$ could be dominated by $C_{gs6}$, the gate–source capacitance of the cascode transistor, depending on the overlap and parasitic capacitances at the cascode node. Since the second pole of this op amp is designed to be at $p_2$, the phase margin of this amplifier is therefore a strong function of the parasitic capacitance at the cascode node. The phase margin of this amplifier is therefore degraded by the parasitic capacitance at this node.

## III. Design Equations for the Op Amp

The theoretical relations developed in the Section II were used to formulate a set of design equations for the op amp. These equations provide a means for directly estimating and tweaking

TABLE I
SUMMARY OF DESIGN EQUATIONS FOR THE FOLDED-CASCODE OP AMP

| Specification | Design Equation |
|---|---|
| Unity gain frequency | $g_{m1} = \omega_0 C_L$ |
| Phase margin | $g_{m6} = \omega_0 C_{L1} tan(PM)$ |
| Slew Rate | $I_{SS} = 2 \cdot SR \cdot C_L$ |
| Output swing | $\Delta V_o^+ = \frac{V_{DD} - V_{omax}}{2}$ <br> $\Delta V_o^- = \frac{V_{DD} - V_{omin}}{2}$ |
| Cascode bias current | $I_{casc} = \omega_0 C_{L1} tan(PM) \Delta V_o^+$ |
| Mid-band gain | $A_0 = \frac{2 g_{m1}}{\lambda^2 I_{casc}\left[\Delta V_0^+ + \Delta V_0^- + \frac{I_{SS}}{g_{m6}}\right]}$ |
| Power Consumption | $(2I_{casc} + I_{SS})(V_{DD} + V_{SS})$ |

TABLE II
NOTATION USED IN DESIGN EQUATIONS

| Symbol | Explanation |
|---|---|
| $g_{m1}$ | transconductance of input stage transistor |
| $g_{m6}$ | transconductance of cascode transistor |
| $\omega_0$ | Unity gain frequency |
| $C_L$ | Load capacitance |
| $I_{SS}$ | Input Stage Bias Current |
| SR | Slew Rate |
| PM | Phase margin |
| $\Delta V_0$ | Output Voltage Swing |
| $\lambda$ | Channel Length Modulation Factor |

TABLE III
$W/L$ RATIOS FOR FIG. 1

| Transistor | W/L ratio |
|---|---|
| M1 M2 | 33:1 |
| M3 | 4.6:1 |
| M4 M5 | 16.9:1 |
| M6 M7 | 9.4:1 |
| M8 M9 | 4.7:1 |
| M10 M11 | 12.6:1 |
| M12 M13 | 10:1 |
| M14-M17 | 1:1 |
| M18 M19 | 10:1 |

TABLE IV
COMPARISON BETWEEN POLE-ZERO LOCATIONS OBTAINED FROM THE FREQUENCY-DOMAIN MODEL AND COMPUTER SIMULATIONS

| Expression | Units | Frequency model | Pole-zeros program | SPICE |
|---|---|---|---|---|
| $p_1 = \frac{1}{R_o C_{L2}}$ | Hz | 250 | 355 | 316 |
| $p_2 = \frac{g_{m6}}{C_{L1}}$ | MHz | 13.62 | 13.43 | 14 |
| $p_3 = \frac{g_{m8}}{C_{L3}}$ | MHz | 38 | 36 | - |
| $z_1 = \frac{g_{m8}}{C_{L3}}$ | MHz | 38 | 36 | - |
| $z_2 = \frac{g_{m6}}{C_{db6}}$ | MHz | 94.5 | 95 | - |

TABLE V
COMPARISON OF DESIGNED AND SPICE-SIMULATED OP-AMP PERFORMANCE

| Parameter | Units | Design Target | Design Equations | SPICE Level 1 | SPICE Level 2 |
|---|---|---|---|---|---|
| $\omega_0$ | MHz | 10 | 10 | 9.8 | 9 |
| PM | degrees | > 60 | 70 | 71 | 72 |
| SR | $V/\mu s$ | > 3 | 5 | 4.6 | 4.4 |
| $A_0$ | dB | > 70 | 79 | 80 | 73 |
| $R_0$ | $M\Omega$ | > 10 | 29 | 29 | 14.5 |
| Dominant pole $p_1$ | Hz | 1000 | 1099 | 1000 | 2000 |
| Power Dissipation | mW | 5 | 5.32 | 5.81 | 5.47 |

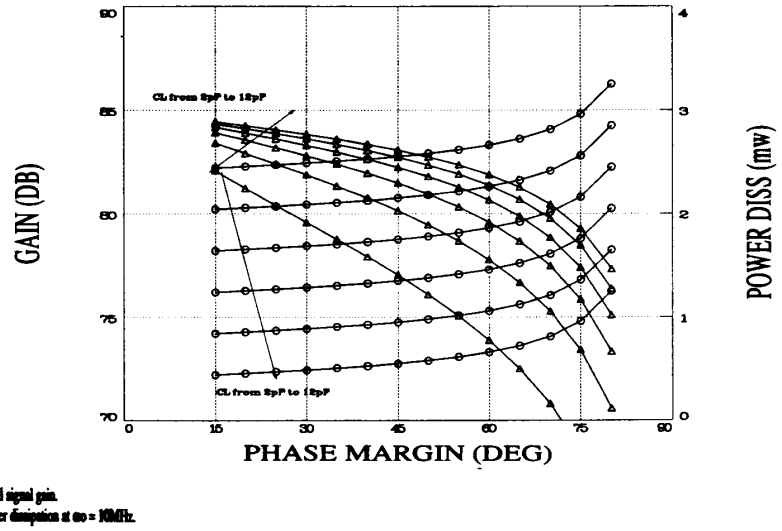


Fig. 3. An example set of design curves for the op amp.

the op-amp MOS circuit parameters from the original set of specifications for the op amp. Table I summarizes these design equations. The notation is clarified in Table II.

The ultimate goal of this design exercise is to directly obtain the $W/L$ ratios of the op amp from the performance requirements. This is achieved by relating the $W/L$ ratios to the $g_m$ parameters. Rearranging the following equation:

$$g_m = \sqrt{2K_n\left(\frac{W}{L}\right)\left(\frac{I_{ss}}{2}\right)} \tag{13}$$

gives

$$W/L = \frac{g_m^2}{2K_n\left(\frac{I_{ss}}{2}\right)}. \tag{14}$$

Table III lists the $W/L$ ratios used in the particular design example cited in this paper.

## IV. SIMULATIONS AND RESULTS

A fully differential folded-cascode op amp (designed to a set of typical specifications) was simulated with SPICE to obtain its small-signal parameters and device capacitances. $C_{L1}$, $C_{L2}$, and $C_{L3}$ were calculated using the formulas developed in Section II. The theoretical results showed good agreement with a Fortran pole-zero calculation program and with the SPICE frequency response plots (Table IV). The simulations verified the existence of a dominant pole governed by the load capacitance, and the effect of the pole-zero cancellation. The circuit was also simulated with large external capacitances added to $C_{L3}$. The frequency response remained unchanged, thereby verifying the presence of the high-frequency pole-zero pair.

The effectiveness of the design equations was studied by taking typical sets of specifications and using the design procedures outlined above to determine the $W/L$ ratios of the MOSFET's in the circuit. SPICE simulations were performed to verify the dc, ac, and transient response of each circuit. Table V summarizes the results of one such set. The SPICE-simulated performance of the op amp was in close agreement with the original specifications used in our design procedures.

Fig. 3 contains contour plots representing the variation in the small-signal gain and power dissipation for different load capacitors as a function of the phase margin of the amplifier. This plot

enabled us to evaluate the performance of the op amp for different sets of specifications without actually going into the circuit details of the op amp. It therefore provided us with valuable information regarding the range of possible values for each of the specified quantities, in order to meet the overall specifications for the op amp, and the interdependencies between those quantities, thereby saving us a huge amount of SPICE simulation time.

## V. Conclusion

The theoretical frequency response of the fully differential folded-cascode amplifier was analyzed, and this analysis was used to characterize the high-frequency behavior of the op amp. The expressions derived in this analysis have been verified with SPICE and a Fortran pole–zero program.

The development of a design equation based procedure provided a quick and effective mechanism for directly estimating the MOS circuit parameters of the op amp from the performance requirements. Op amps designed with these calculated circuit values were able to satisfy these requirements, as evidenced by our SPICE simulations. This considerably reduced the total number of SPICE runs for the design, thereby realizing our goal of minimizing the design and simulation efforts of the op amp. The design equations also highlighted the principal factors affecting the performance specifications, which made it very easy to redesign the circuit for different sets of specifications.

The design procedure used in this paper is based on a relatively simple first-order MOS model. Our motivation behind this approach has been to pave the way for relatively novice designers with little or no analog experience to easily come up with a first-pass design for something as complicated as a fully differential amplifier, and to give them the opportunity to design and simulate almost state-of-the-art analog building blocks. We feel that by extending these design procedures to other analog circuit functions, there is a potential for the evolution of a widespread, standardized analog design methodology. We also foresee this approach being applied in analog design automation systems. The relative simplicity of these design equations makes them efficient candidates for integration into knowledge-based analog CAD tools. These equations could also be used to generate a set of multidimensional curves on a workstation, with each dimension represented by a circuit parameter or performance specification. This would enable the designer to visually identify the effect of variations in a particular parameter on the rest of the circuit, thereby providing an insight into the trade-offs and other limitations in a particular design situation.

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# On the Relationship Between the CMRR or PSRR and the Second Harmonic Distortion of Differential Input Amplifiers

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***Abstract*—In this paper, the results of a harmonic distortion analysis for a differential pair are presented, including the effects of mismatches and of the finite nonlinear common-mode rejection ratio (CMRR) or power-supply rejection ratio (PSRR). Due to mismatches, a differential pair produces second harmonic distortion which is normally larger than the third one. The presence of a finite common-mode gain limits the amount of feedback which can be usefully applied to suppress the harmonic distortion. When the common-mode gain is nonlinear, additional distortion will be generated which is not suppressed by the feedback. When the amplifier has to drive a large load and when the supply line impedance is large, the finite PSRR causes similar effects.**

## I. Introduction

According to basic theories [1], a differential input pair only produces odd harmonics which can be suppressed indefinitely by applying more and more negative feedback. Due to mismatches between the input transistors, even harmonics will be produced as well. Although this effect is well known among circuit engineers, it is often treated as only a second-order effect. However, distortion measurements on a test amplifier, presented in Section II, show that the second harmonic distortion is even larger than the third one just because of the mismatches. Therefore, the effects of mismatches are of prime importance for distortion analysis.

The common-mode gain is another second-order effect which is often neglected in distortion analysis. When using a differential pair as a noninverting buffer, the common-mode input voltage is much larger than the differential input voltage and is not affected by the negative feedback. Moreover, the nonlinearity of the common-mode gain causes additional distortion which is not suppressed by the negative feedback and therefore becomes the major distortion contribution.

For large feedback factors, the differential input voltage of a noninverting amplifier is determined by the common-mode rejection ratio (CMRR) rather than by the differential gain. This is a third effect which is often neglected in distortion analyses. In this paper, it is shown that the finite CMRR limits the amount of feedback which can be usefully applied to suppress the distortion.

A similar effect is caused by the power-supply gain when an amplifier has to deliver a large output current and when the supply line impedance is considerable.

In the analysis below, the differential pair is treated as a nonlinear circuit with two independent inputs. Since it is only important to give a qualitative explanation of the effects mentioned above, only the second harmonic distortion is calculated. An analysis of the third harmonic distortion is quite involved and is omitted.

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