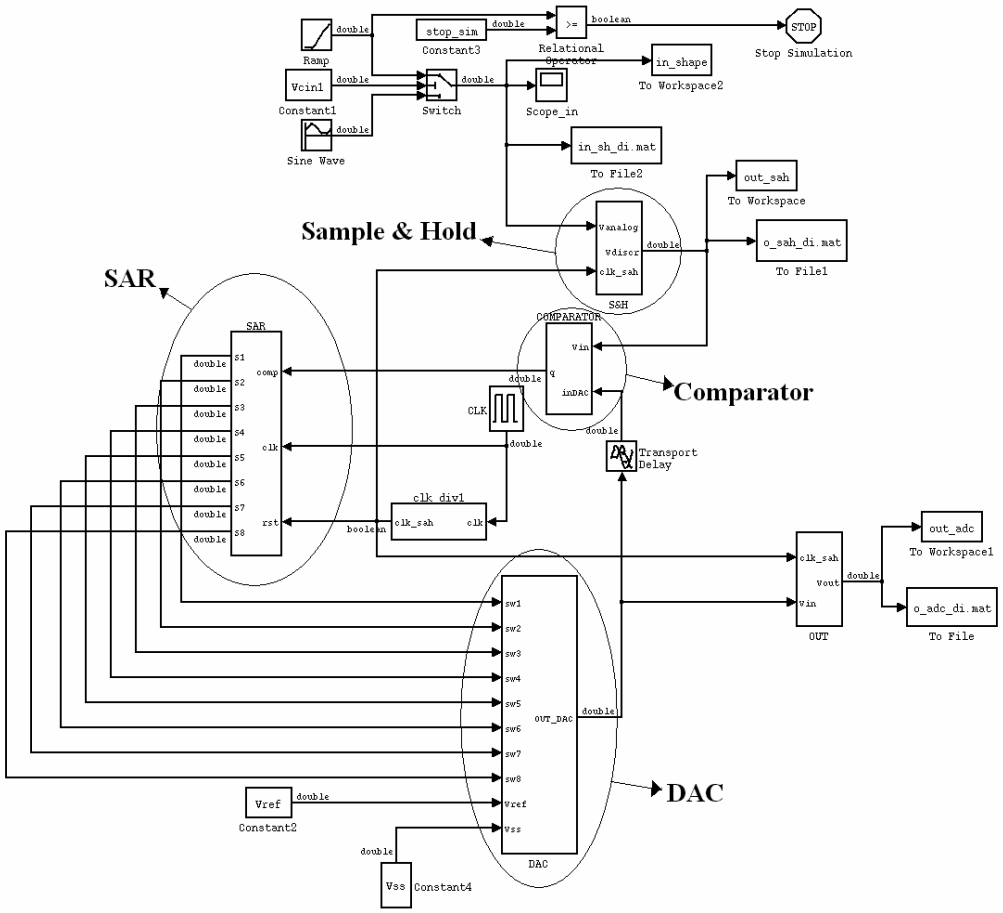

Figure 9: Simulink Model

The logic block (Figure 10) has been implemented using two shift register in order to perform the successive approximation routine [20]. Each shift register is composed by a chain of nine D Flip-Flops. The shift register on the top is used as a sequencer and is synchronous with the internal clock. The bottom register stores the conversion value.

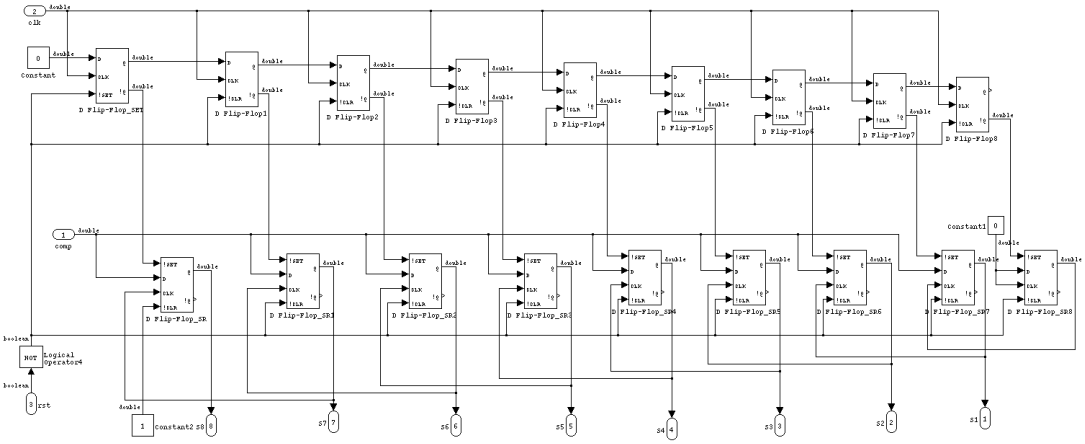

Figure 10: SAR Logic Simulink Model