DESIGN OF A PHASE FREQUENCY DETECTOR AND CHARGE PUMP FOR A PHASE-LOCKED LOOP IN 0.18μm CMOS

A Project

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Jeffrey Morgan

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Department of Electrical and Electronic Engineering

Abstract

of

DESIGN OF A PHASE FREQUENCY DETECTOR AND CHARGE PUMP

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The design and simulation of a phase frequency detector and a charge pump for a low-jitter, high-frequency phase-locked loop in 0.18μm CMOS are explored. The NAND-based sequential phase frequency detector is shown to accurately compare the phase differences between two clock signals without the presence of a "dead zone". The charge pump exhibits excellent linearity over a wide range of loop filter voltages as well as with varying differences in phase. A minimum phase offset of 2.45º is achieved by the use of current matching techniques and differential input transistors that are constantly kept in saturation. A new implementation of a common clamping technique has also been used in order to eliminate non-monotonicity in the charge pump output.

_____, Committee Chair
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Date

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Chapter 1

INTRODUCTION

1.1 Background

Stable high-frequency clocks are required in practically all RF and digital integrated circuits. Unfortunately the simple oscillators available for use on integrated circuits do not typically produce clocks with the low fluctuations in frequency (jitter) required for most applications [1]. The phase-locked loop (PLL) is a widely used solution to the problem of creating an oscillator with a precise frequency. A PLL is a circuit that uses feedback to align a high frequency on-chip clock to an accurate off-chip reference clock. A charge pump PLL, as described in this report, offers the benefit of nearly zero static phase error, meaning there is close to zero error in the phase and frequency of the on-chip clock when the loop is 'locked' [2].

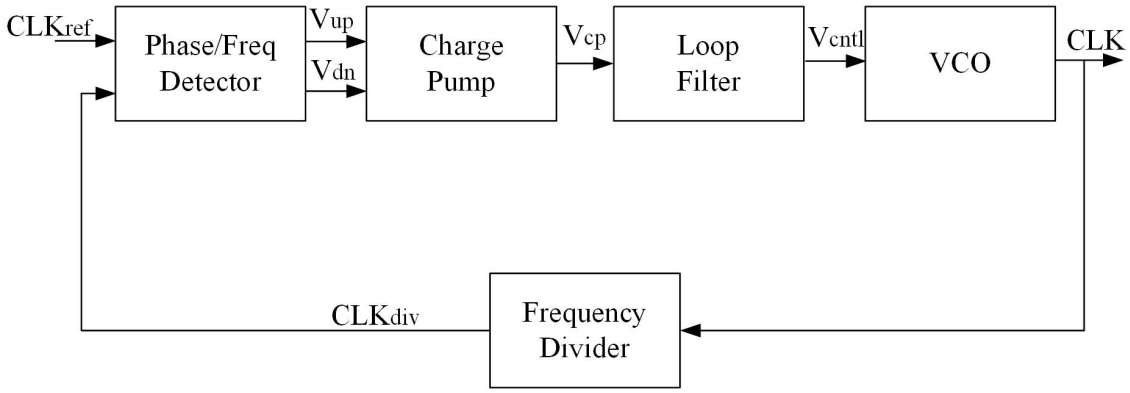


Figure 1.1 Block Diagram of a Charge Pump Phase-Locked Loop

Figure 1.1 shows the basic architecture of a charge pump PLL. The loop consists of a phase frequency detector, a charge pump, a low-pass filter, a voltage-controlled

oscillator (VCO), and a frequency divider. The phase frequency detector (PFD) compares the phase and frequency of the two clocks and produces either a pump-up or pump-down signal depending on whether the phase of the on-chip clock is lagging or leading the external reference clock. The charge pump increases the voltage on the loop filter capacitor when given a pump-up signal and decreases this voltage when given a pump-down signal. The loop filter is a low-pass filter used to average out the high-frequency components of the charge pump output and set the bandwidth of the PLL feedback loop. The VCO produces an output clock the frequency of which is proportional to its input voltage [3]. The frequency divider divides down the frequency of the VCO output clock to produce a clock signal with a frequency in the same range as that of the reference clock.

In Figure 1.1, CLK_{ref} represents the external reference clock, CLK represents the high-frequency output clock from the VCO, and CLK_{div} represents the frequency divided version of the VCO clock that can be compared with the lower frequency reference clock, CLK_{ref}. The negative feedback around the PLL loop adjusts the phase and frequency of the VCO clock until the PLL loop 'locks' to the reference clock by matching its phase and frequency.

1.2 Phase Frequency Detector

The PFD is a digital circuit that uses sequential logic to detect phase or frequency differences between its two input clocks [1]. When the clock fed back from the loop lags the reference clock, the pump-up output of the PFD goes high. This indicates that the

frequency of oscillation needs to be increased. Similarly, when the feedback clock leads the reference clock, the pump-down output goes high, indicating that the frequency of oscillation needs to be decreased [4].

1.3 Charge Pump

The charge pump is an analog circuit consisting primarily of two stacked differential pairs of transistors. A differential pair of PMOS transistors is used to steer the current from a PMOS current source so that charge is added to the loop filter capacitor when the pump-up signal is active, which increases the control voltage to the VCO thereby increasing its frequency. A differential pair of NMOS transistors is used to steer the current from an NMOS current source so that charge is removed from the loop filter capacitor when the pump-down signal is active, which decreases the control voltage to the VCO thereby decreasing its frequency [4].

1.4 Scope of Project & Report Organization

The goal of this project was to design a PFD and charge pump as part of a full PLL designed by a six-member project team. The focus of this report is on the work of one member of that team, and so the remainder of this report will specifically cover the design, simulation and layout of the PFD and charge pump circuits. Further information on the design of the VCO and the CML clock divider can be found in the reports written by the other members of the team [5][6].

The analysis and design of the PFD and charge pump circuits will be discussed in Chapter 2. Chapter 3 will cover the simulation results for each of these circuits. And Chapter 4 will discuss the layout for each circuit block.

Chapter 2

CIRCUIT DESIGN

2.1 Design of the Phase Frequency Detector

The sequential PFD chosen for this project consists of two pairs of cross-coupled R-S latches with a reset path [7], as shown in Figure 2.1. Each R-S latch is made up of a cross-coupled pair of nand gates. Because the latches are NAND-based, this PFD is negative-edge triggered.

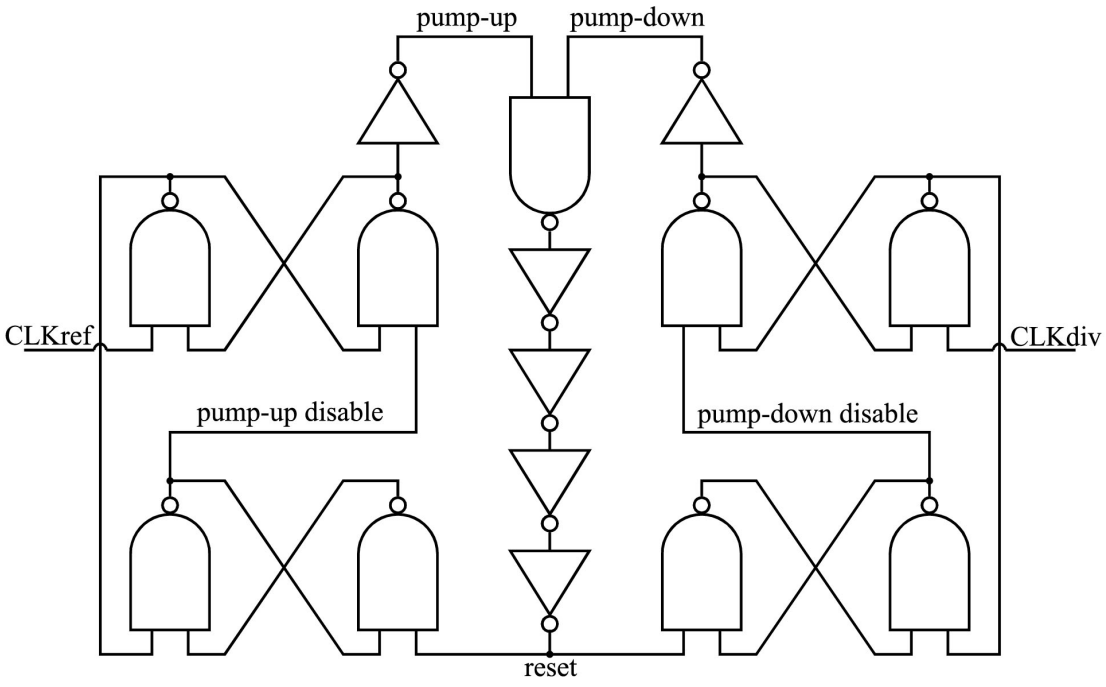


Figure 2.1 NAND-Based Sequential Phase Frequency Detector

The two top latches in Figure 2.1 provide the pump-up and pump-down signals while the two bottom latches disable the pump-up and pump-down signals when needed. The pump-up signal is triggered by the falling edge of CLK_{ref} and the pump-down signal

is triggered by the falling edge of CLK_{div}. The NAND gate in the reset path is used to trigger a reset signal whenever both pump-up and pump-down are active at the same time [4]. When both the pump-up and pump-down signals are high, the reset signal will go low. Triggering the reset signal forces both disable signals to go low, which in turn forces both the pump-up and pump-down signals to also go low. Pump-up disable is reset high on the rising edge of CLK_{ref} and pump-down disable is reset high on the rising edge of CLK_{div}. As an example of how this circuit operates, Figure 2.2 illustrates what happens in the case when CLK_{div} lags CLK_{ref} by 90º.

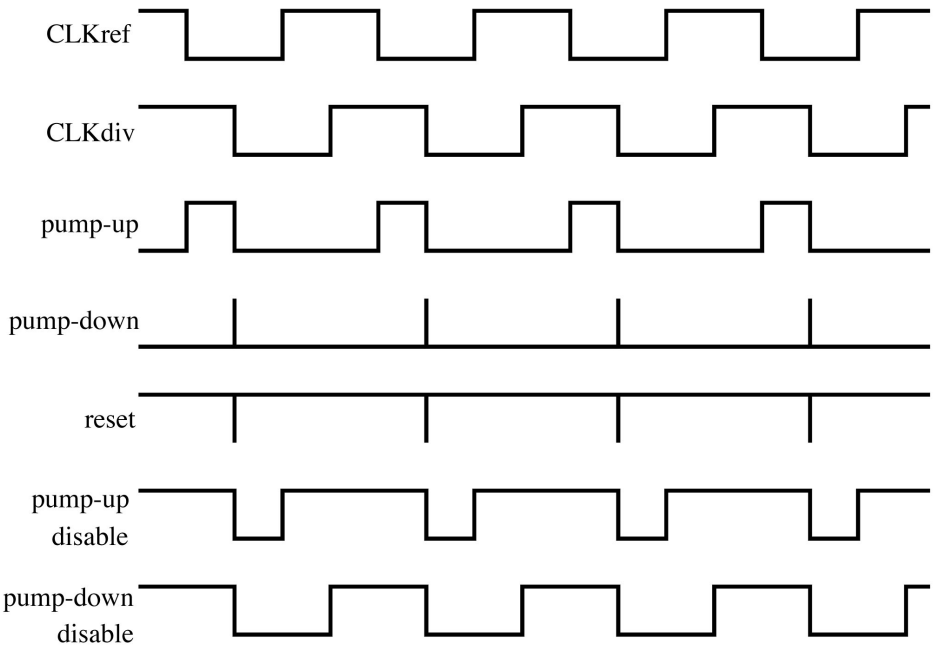


Figure 2.2 PFD Signals when CLK_{div} Lags CLK_{ref} by 90º

Even though the PLL loop requires only pump-up signals to compensate for the phase lag in this case, there will be a very narrow pulse of the pump-down signal once during each period. This occurs as a result of the gate delays in the reset path. These

narrow pulses will occur in both the pump-up and pump-down signals even when there is zero phase difference between CLK_{ref} and CLK_{div} [5]. This is actually desirable, since its effect is to eliminate something called a "dead zone" in the response of the PFD [4]. As we know, true square waves that switch in zero time do not exist in real circuits. A finite amount of time is always required for any logic gate to switch from one logic state to another. Consider the case when CLK_{ref} leads CLK_{div} by a very small phase difference. Without the presence of these narrow pump-up pulses, it is possible that the pump-up signal may not reach a full logic-high level and turn on the switches in the charge pump before being reset. This would result in a "dead zone", which is a range of tiny phase differences where the PLL loop is unable to provide corrective feedback. This contributes to undesirable jitter in the VCO and must be avoided [7].

A simple solution to eliminate this "dead zone" is to add gate delays in the reset path, to ensure that both the pump-up and pump-down signals always turn on for a minimum amount of time. The PFD used for this project includes four inverters in the reset path to add this delay. Since the PFD is used in conjunction with a charge pump, this increased delay has no effect on the loop filter voltage. As long as the minimum pump-up signal is equal to the minimum pump-down signal, no net charge is added to or removed from the loop filter capacitor.

Inverter	
W_P	4.14 µm
W_N	1.44 µm
L	0.18 µm

(a)

NAND Gate	
W_P	4.14 µm
W_N	2.88 µm
L	0.18 µm

(b)

Table 2.1 Phase Frequency Detector Device Sizes

The logic gates used for the PFD were optimized for speed and equal rise and fall times. Table 2.1 shows the device sizes used in this design. The pass gates use device sizes identical to the inverter. The final schematic for the PFD is shown in Figure 2.3.

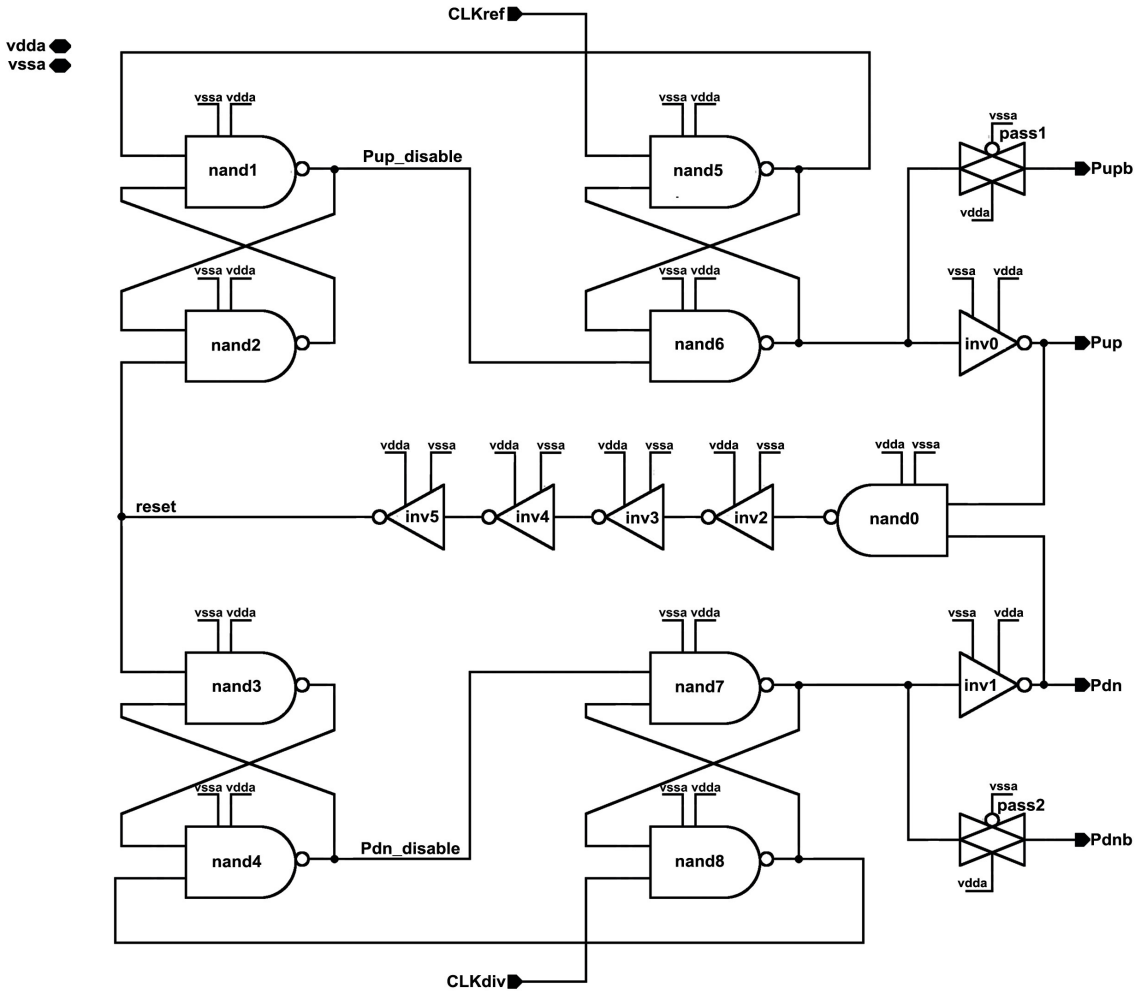


Figure 2.3 Phase Frequency Detector Circuit

Figure 2.3 shows the addition of two outputs, $P_{up}b$ and $P_{dn}b$. These signals are the compliments of P_{up} (pump-up) and P_{dn} (pump-down), respectively. The pass gates used for $P_{up}b$ and $P_{dn}b$ were included to equalize the gate delay to each of the four outputs.

These additional outputs were provided because the charge pump requires differential inputs. This will be discussed further in the next section.

2.2 Design of the Charge Pump

There are several important design considerations necessary to create a good charge pump with minimal phase offset [4]. As described in Chapter 1, the main function of the charge pump is achieved through the use of two differential pairs of transistors that steer current either toward or away from the loop filter capacitor. Several factors play a role in ensuring that the amounts of charge added to or removed from the loop filter capacitor are equal and consistent.

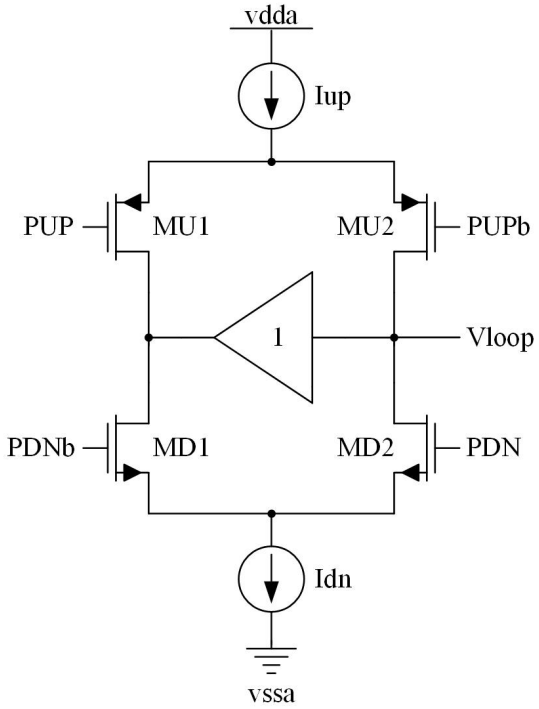
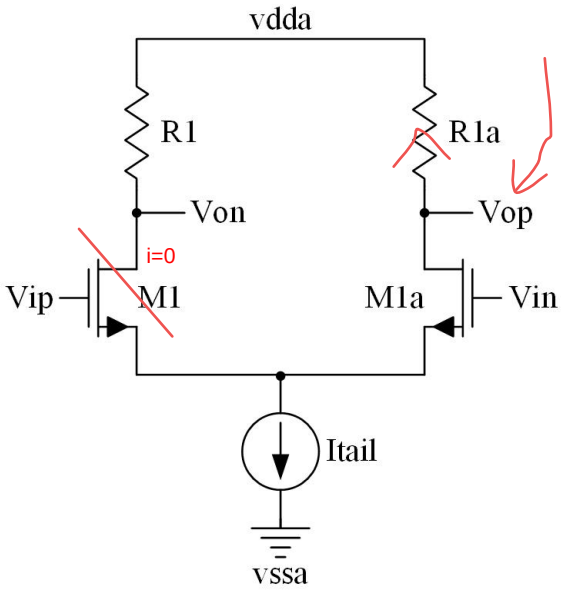


Figure 2.4 Architecture of a Basic Charge Pump

Figure 2.4 shows the basic charge pump architecture. The differential pairs consist of MU1, MU2, MD1 and MD2. If driven directly by the digital outputs of the PFD, these MOS transistors would operate as triode switches. For this design, it was decided that the MOSFETs in these differential pairs should instead be kept in saturation rather than used as switches. This allows these FETs to act as cascodes for the pump-up and pump-down current sources, which increases their output impedance and thereby keeps these currents more constant as the loop filter voltage varies. Saturation of the four devices in these differential pairs was maintained by limiting the voltage swing for the input signals that drive them to the minimum required to steer the tail currents from one side to the other. This was accomplished through the use of current-mode logic (CML) buffers as an interface between the full swing digital CMOS outputs of the PFD and the inputs of the charge pump.



$V_{on} = vdda$

$V_{op} = vdda - I_{tail} \cdot R1a$

Figure 2.5 Basic NMOS Current-Mode Logic Buffer

Each CML buffer converts its rail-to-rail digital CMOS input signal to a limited swing output signal without significantly altering the signal's phase or frequency. As shown in Figure 2.5, a basic CML buffer consists of a tail current source, an input differential pair, and two resistor loads [8]. When the tail current is steered completely to the right side of the buffer, the output voltages will be:

$$V_{on} = \text{vdda}$$

$$V_{op} = \text{vdda} - I_{tail} \cdot \text{R1a}$$

Since R1= R1a, V_{op} and V_{on} will have the opposite values when the tail current is steered entirely to the left side of the buffer. The resulting output signals appear similar to the input signals except that the output voltage swing has been limited. This is exactly what is needed for this application since the output voltage swing of each CML buffer can be optimized to keep the MOSFETs used in the differential pairs in the charge pump saturated.

Figure 2.6 shows two CML buffers, one using an NMOS differential pair and one using a PMOS differential pair. The output voltages of the NMOS buffer are referenced to the vdda supply, just as the input voltages for the PMOS differential pair used in the charge pump are referenced to the vdda supply. Therefore, an NMOS input CML buffer is well-suited to drive the PMOS differential pair in the charge pump. Similarly, the CML buffer that uses a PMOS differential pair is well-suited to drive the NMOS differential pair in the charge pump, since its common-mode voltage is referenced to the vssa supply. This configuration helps the circuit work reliably even with variations in supply voltage.

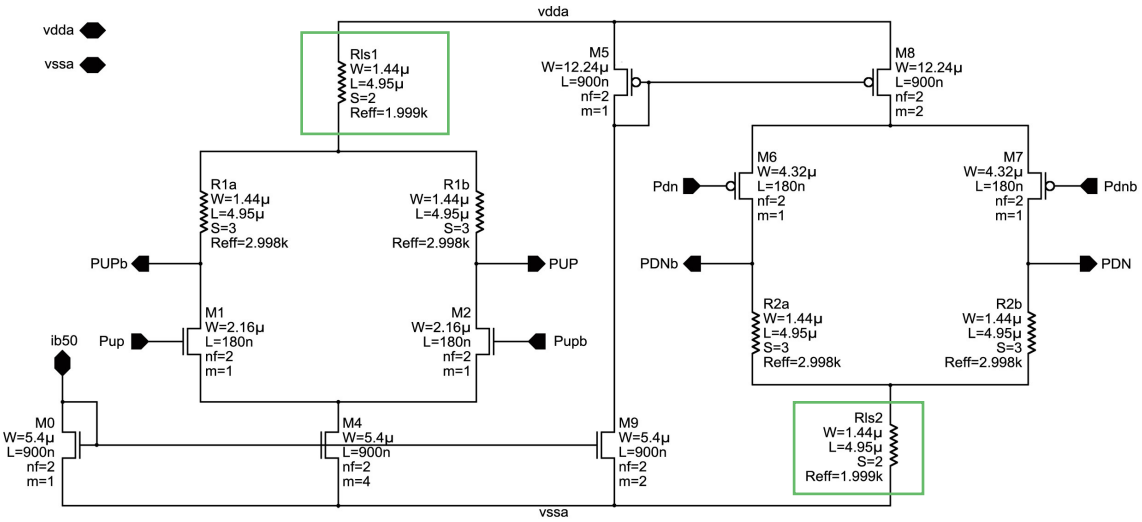


Figure 2.6 Complimentary Current-Mode Logic Buffer Circuits

The additional resistors, Rls1 and Rls2, act as level-shifters to adjust the output common-mode levels for these CML buffers to the values needed for the differential pairs in the charge pump. Ideally, the current through these level shift resistors is constant even as the CML buffers steer their tail currents from one side to the other [8]. The two CML buffers were optimized to exhibit similar R-C time constants at their outputs to equalize the delays through the signal paths for the pump-up and pump-down signals.

Another important consideration when designing a charge pump is the matching of the pump-up and pump-down currents. When the loop is 'locked' with zero phase difference between CLK_{ref} and CLK_{div}, there should be zero net charge added to the loop filter capacitor and therefore the loop filter voltage should not change [7]. When a mismatch exists between the pump-up and pump-down currents, a nonzero amount of charge will be either added to or removed from the loop filter capacitor during each cycle

when the loop is 'locked'. This results in a phase difference being required between CLK_{ref} and CLK_{div} to produce an unchanging loop filter voltage, which is referred to as a phase offset. For this PLL application a small amount of phase offset is acceptable, since the goal is not to synchronize the phase of the output clock precisely with the reference clock, but instead to produce a stable high-frequency clock. Another disadvantage of having a mismatch between the pump-up and pump-down currents is that the loop filter voltage will change at a different rate when pumping up than it will when pumping down. As a result the PLL loop bandwidth when pumping up will be slightly different than the PLL loop bandwidth when pumping down. However this is also acceptable, as long as the mismatch between the pump-up and pump-down currents is kept small. Of more concern than either of these two effects is the jitter caused by a mismatch between these currents, which is the main reason why this mismatch must be minimized for this application.

The full charge pump used for this project is shown in Figure 2.7. This charge pump circuit utilizes a wide-swing cascode bias circuit to improve the matching between the pump-up and pump-down currents as the loop filter voltage varies. The cascode devices greatly increase the output impedance of the current mirrors. This high output impedance reduces variations in the current over the output voltage range.

As shown by Marcel Pelgrom [10], there are two key process variations which contribute to current mismatch in MOS devices. First, small variations in device geometry due to edge effects will cause larger variations in drain current with small device sizes than with large device sizes. Second, CMOS processes also exhibit variations in the MOS threshold voltage (V_T). The effect of variations in V_T can be

reduced by increasing the overdrive voltage ($V_{ON} = V_{GS} - V_T$) of the transistor. Pelgrom's research also showed that for current mirrors the mismatch in the output current will vary inversely with the channel length (L) of the devices used [10]. So by increasing L, variations in the mirror output current due to both edge effects and variations in V_T are reduced. In Figure 2.7 NMOS transistors M1, M2, M3 and M4 along with PMOS transistors M6 and M7 make up the main current mirrors. All of these devices were designed with five times the minimum channel length to improve current matching. Mismatch in the cascode devices M1C, M2C, M3C and M6C only contribute a little to the current mismatch, so they were designed with shorter channel lengths to reduce capacitance.

The PLL loop dynamics are determined by the charge pump current, the VCO gain and the loop filter characteristics. The charge pump current, provided as the drain currents of M4 and M7, was chosen to be 50μA to produce a loop bandwidth for the overall PLL of 2MHz.

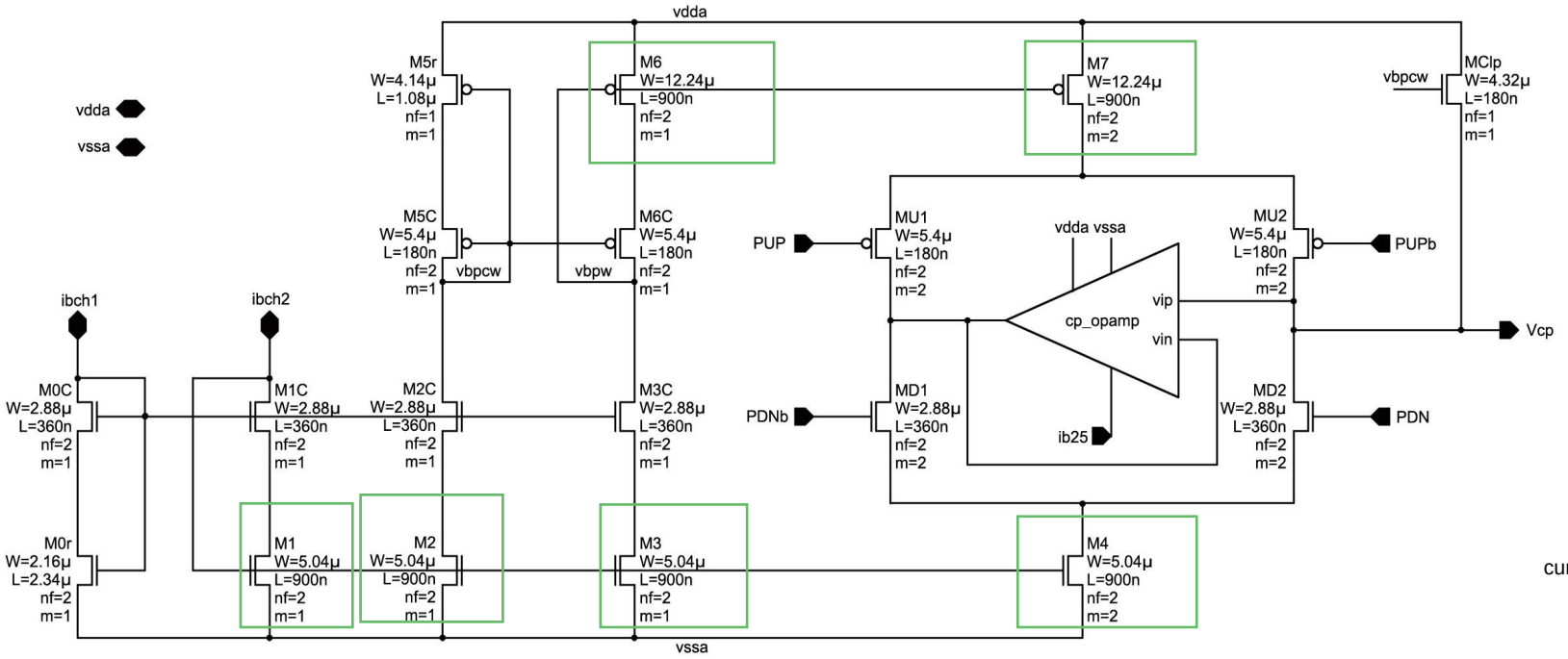


Figure 2.7 Charge Pump Circuit

current mirrors

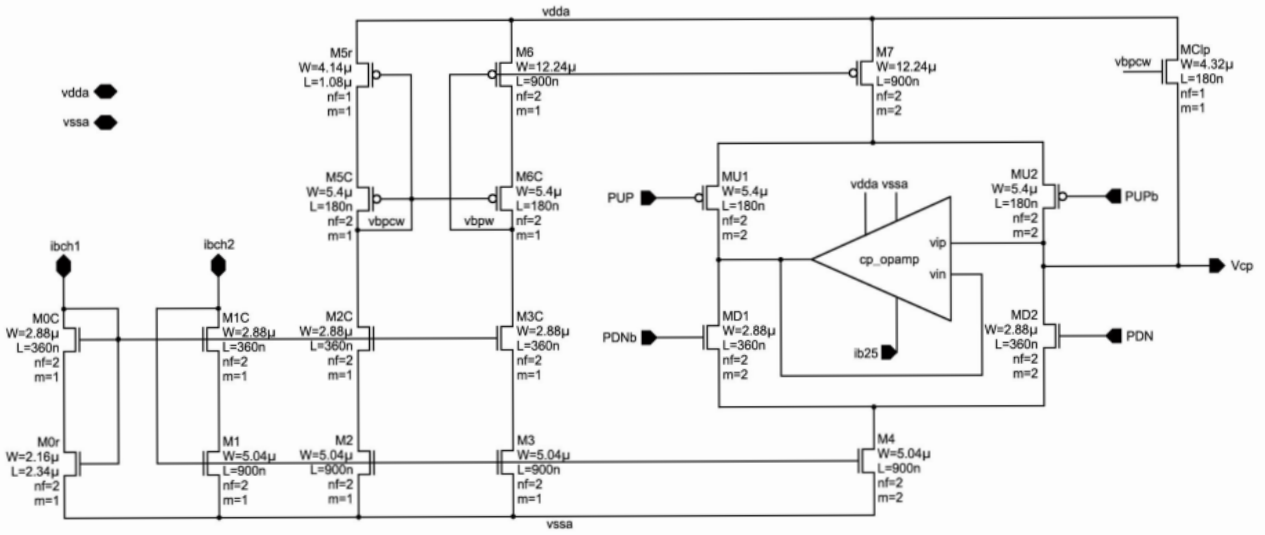


Figure 2.7 Charge Pump Circuit

2.3 Design of the Unity Gain Buffer

The operational amplifier shown in Figure 2.7 is used as a unity gain buffer to equalize the voltages at the outputs of the differential pairs in the charge pump, which ensures these transistors operate in saturation. This op amp also sources or sinks the pump-up or pump-down currents as the charge pump switches. An op amp used in this manner does not require a large amount of gain. Also, a small input-referred offset voltage of a few millivolts will not compromise the intended function of the op amp. And the unity gain bandwidth of the op amp only needs to be high enough that the op amp can easily change its output as fast as changes occur in the loop filter voltage, which is relatively slow. Therefore the main design concerns for this op amp were a wide output voltage swing, a sufficient input common-mode voltage range, and a good phase margin [9].

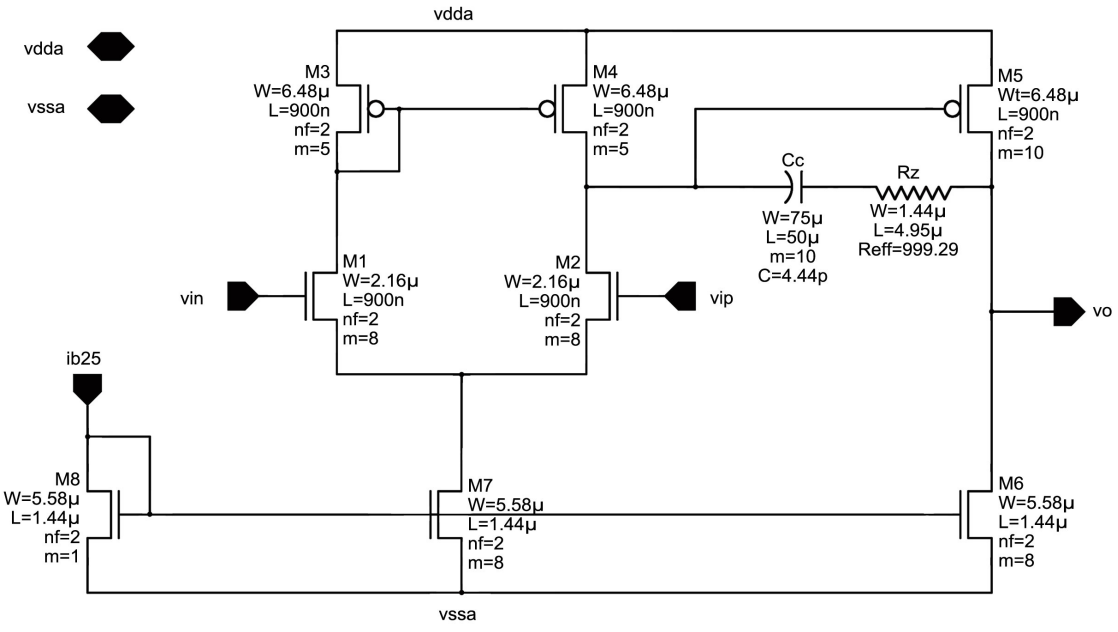


Figure 2.8 Two-Stage Operational Amplifier Circuit

The two-stage operational amplifier used as the unity gain buffer for this design is shown in Figure 2.8. Compensation is provided by adding a capacitor and resistor in series between the output and the input of the second stage of the op amp [9]. The addition of the capacitor, C_c, splits the poles at the outputs of the first and second stages. The pole at the output of the first stage is moved to a lower frequency while the pole at the output of the second stage is moved to a higher frequency [9]. The resistor, R_z, cancels the right-half plane zero that degrades the phase margin of the op amp [3]. Fine-tuning of these two components was done to optimize the phase margin.

Since the input of the op amp is connected to the loop filter, the op amp must be able to operate for all possible loop filter voltages at its input and output. For this application, the loop filter voltage required by the VCO was expected to remain within 0.9V to 1.6V. This two-stage op amp was able to meet this required input common-mode voltage range and output voltage swing. In the unlikely event that the loop filter voltage might drop below 320mV (e.g. during startup), it is possible that the op amp would not be able to recover. To prevent this potential issue, an NMOS clamp was added at the output of the charge pump. This clamp is shown as MClp in Figure 2.7. The operation of this clamp will be discussed in Chapter 3.

Chapter 3

SIMULATION RESULTS

Each circuit used for this project was simulated across five variations of process, supply voltage, and temperature known as PVT "corners" in order to ensure that the circuits would function over a wide range of process variations and operating conditions. Table 3.1 shows the values for the process variation, temperature and supply voltage used for each simulation corner. SS represents the process corner where both NMOS and PMOS devices are slow, SF represents slow NMOS and fast PMOS devices, TT represents typical NMOS and typical PMOS devices, FS represents fast NMOS and slow PMOS devices, and FF represents both fast NMOS and PMOS devices. High temperature and low supply voltage were combined with the SS corner in order to examine all of the worst case conditions at one end of the spectrum together, while low temperature and high supply voltage were combined with the FF corner to examine all of the best case conditions at the other end of the spectrum together. Nearly all PVT corner variations will occur between these two extreme cases.

Process	Temperature	Supply
SS	85º C	1.6 V
SF	30º C	1.8 V
TT	30º C	1.8 V
FS	30º C	1.8 V
FF	0º C	2.0 V

Table 3.1 PVT Corners Simulated

3.1 Simulation of the Phase Frequency Detector

Figure 3.1 shows the behavior of the phase frequency detector in the SS corner when CLK_{div} lags CLK_{ref} by 90º. Notice that the pump-down signal easily reaches a full logic high level before being reset even when the phase difference causes a long pump-up signal. This is thanks to the additional inverter delays added in the reset path.

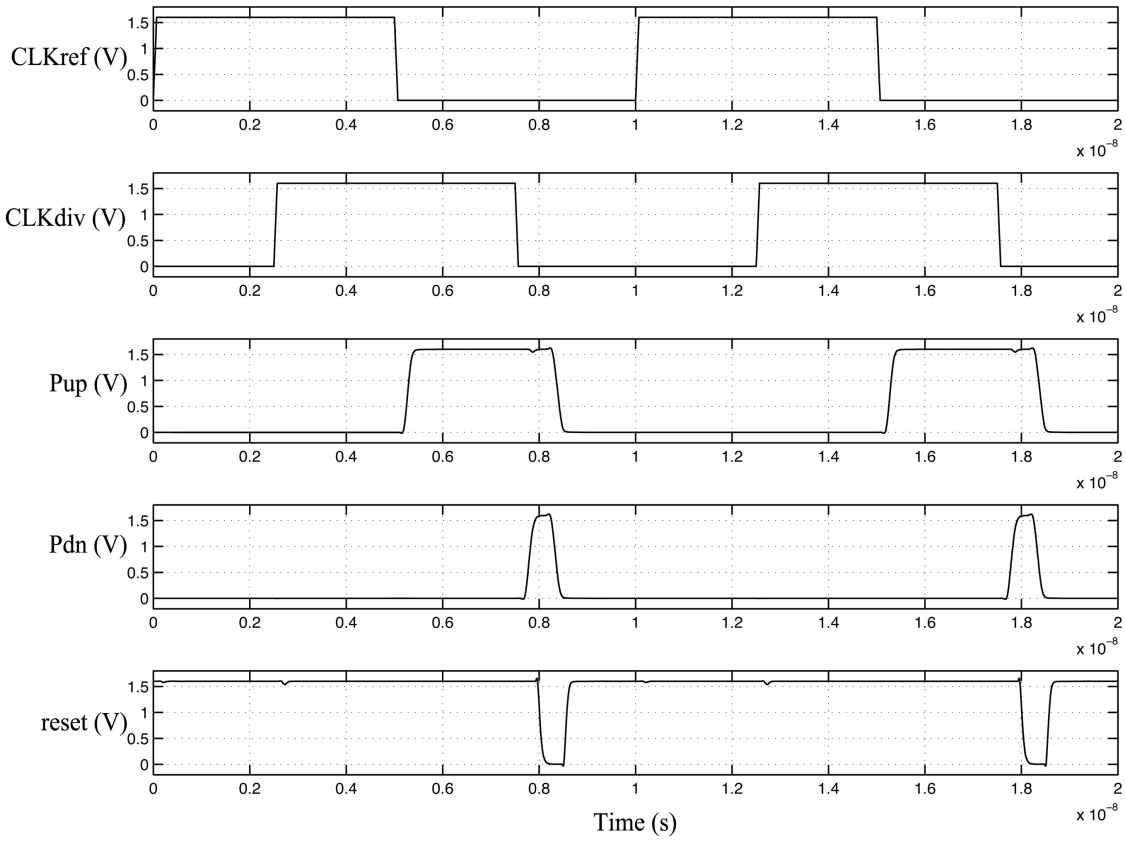


Figure 3.1 PFD Simulation when CLK_{div} Lags CLK_{ref} by 90º (SS Corner)

Table 3.2 shows the reset delay for each PVT corner. The reset delay is the amount of time that it takes for the reset signal to go low after both of the pump-up and pump-down signals have switched to a logic-high state. This delay time was measured from the point when Pdn has reached 50% of the supply voltage to the point when reset has fallen to 50% of the supply voltage. Table 3.3 shows the input to output delay for each PVT corner. The input to output delay represents the time it takes for a change in the input to cause a change in the output. This delay time was measured from the point where CLK_{ref} falls to 50% of the supply voltage to the point where Pup reaches 50% of the supply voltage.

PVT Corner	Delay
SS	222.6 ps
SF	173.3 ps
TT	173.3 ps
FS	173.3 ps
FF	145.7 ps

Table 3.2 PFD Reset Delay

PVT Corner	Delay
SS	244.4 ps
SF	192.9 ps
TT	192.9 ps
FS	192.9 ps
FF	164.2 ps

Table 3.3 PFD Input to Output Delay

3.2 Simulation of the Charge Pump and Sub-Circuits

The output voltage swing for each of the two CML buffers driving the charge pump was optimized so that the FETs in the charge pump could be kept in saturation. Figure 3.2 shows the output swings for the two CML buffers in the SS corner. Tables 3.4 and 3.5 show the simulated output voltage swing for these two CML buffers.

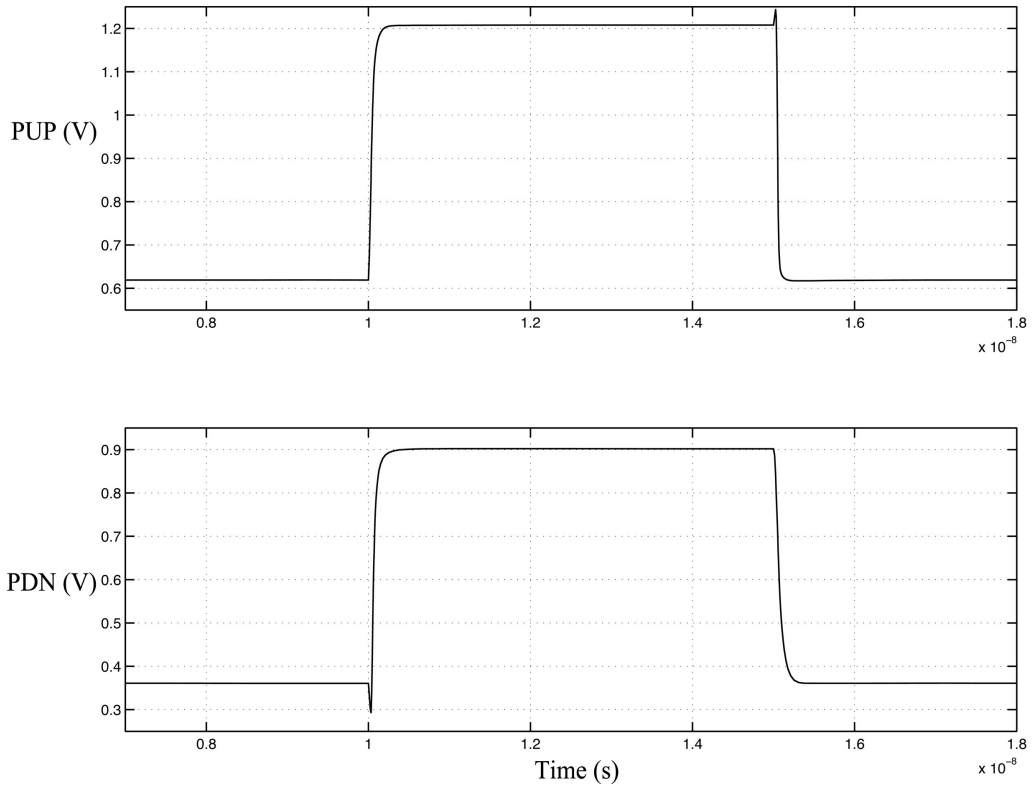


Figure 3.2 Output Voltage Swings for the CML Buffers (SS Corner)

PVT Corner	Max	Min	Swing
SS	1.208 V	618.8 mV	589.2 mV
SF	1.398 V	793.2 mV	604.8 mV
TT	1.398 V	793.9 mV	604.1 mV
FS	1.398 V	793.8 mV	604.2 mV
FF	1.589 V	972.1 mV	616.9 mV

Table 3.4 Pump-Up CML Buffer Output Swing

PVT Corner	Max	Min	Swing
SS	902.2 mV	360.8 mV	541.4 mV
SF	985.4 mV	394 mV	591.4 mV
TT	985.9 mV	394.2 mV	591.7 mV
FS	985.3 mV	394 mV	591.3 mV
FF	1.026 V	410.3 mV	615.7 mV

Table 3.5 Pump-Down CML Buffer Output Swing

A DC operating point simulation was run for the unity gain buffer in each simulation corner. For these tests every MOSFET in the op amp remained in saturation with a minimum input voltage of 630 mV. This meets the 900 mV minimum input voltage specification for this op amp. Figure 3.3 shows the AC response of the op amp at the SS corner, with the results for the remaining corners summarized in Table 3.6. The unity gain bandwidth of the op amp exceeds ten times the PLL loop bandwidth of 2 MHz in all corners. The target phase margin for the op amp was 72º. The simulation results show that variations were within 2.5º of the desired phase margin across all simulation corners.

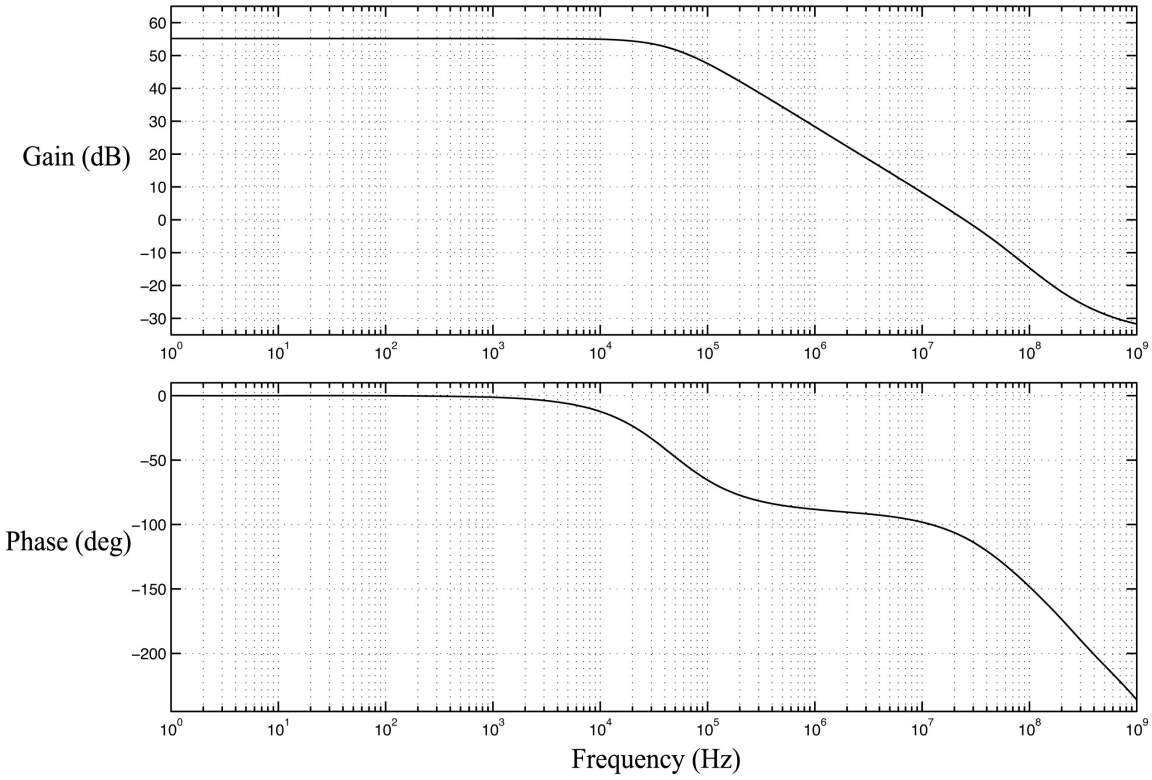


Figure 3.3 AC Response of the Unity Gain Buffer (SS Corner)

PVT Corner	Gain	Phase Margin	UGBW
SS	55.16 dB	69.918º	24.9264 MHz
SF	61.44 dB	72.401º	29.5706 MHz
TT	61.44 dB	72.401º	29.5706 MHz
FS	61.44 dB	72.401º	29.5706 MHz
FF	64.725 dB	74.322º	32.5832 MHz

Table 3.6 Simulation Results for the Unity Gain Buffer

Figure 3.4 shows the drain currents of M4 and M7. The drain current of M7 is the pump-up current and the drain current of M4 is the pump-down current for the charge pump. Table 3.7 shows how closely these currents are matched in each PVT corner.

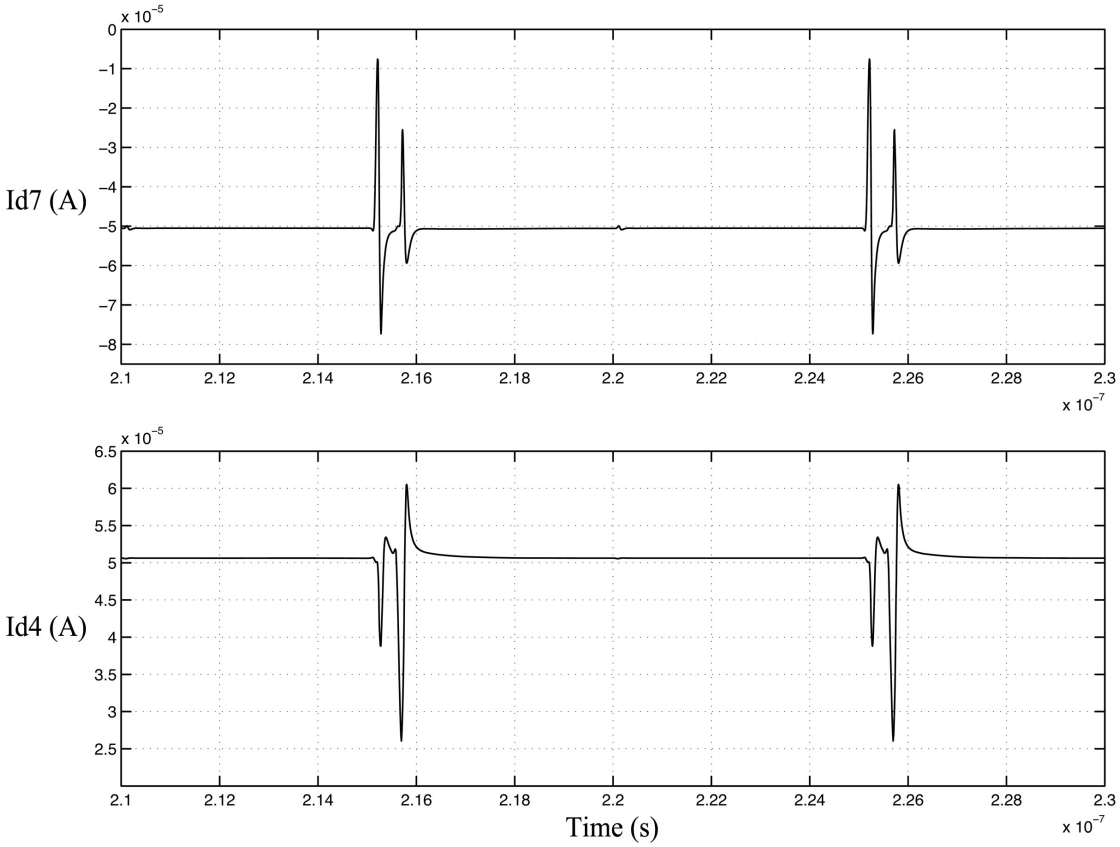


Figure 3.4 Pump-Up and Pump-Down Currents (SS Corner)

Corner	Pup Current	Pdn Current
SS	50.536 µA	50.559 µA
SF	50.9 µA	52.62 µA
TT	50.904 µA	52.62 µA
FS	50.9 µA	52.62 µA
FF	51.232 µA	53.757 µA

Table 3.7 Pump-Up and Pump-Down Currents

Figure 3.5 shows the amount of net charge that is added to the loop filter capacitor per pump depending on the phase difference between CLK_{ref} and CLK_{div}. Notice that the slope of the line is approximately the same when charge is being added to the filter capacitor as the slope when charge is being removed from the filter capacitor. This is because the pump-up and pump-down currents are very well matched in the SS corner. Similar plots for the other corners where the current is less well matched would exhibit a slight change in slope where the line crosses the point of zero net charge.

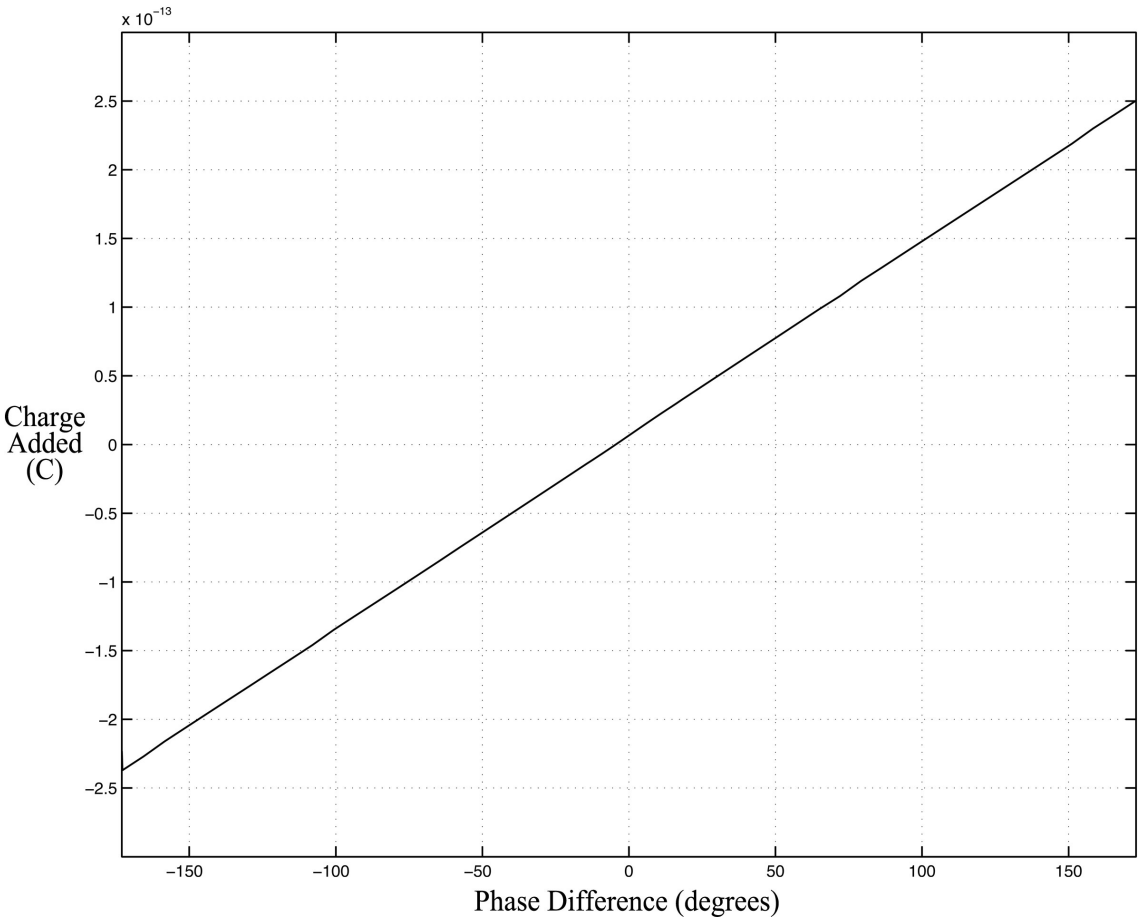


Figure 3.5 Charge Added vs. Phase Difference (SS Corner)

The phase offset shown in Figure 3.5 is the phase difference where zero net charge is added to the loop filter capacitor. The phase offset for this circuit could be caused by several possible factors. One is that the minimum pulse-width of the pump-up signal is slightly greater than the minimum pulse-width of the pump-down signal, resulting in a small amount of net charge being added to the loop filter when there is no phase difference between CLK_{ref} and CLK_{div}. However, it is unlikely that this is the main contributor to the phase offset for this circuit, since the minimum pulse-widths of the two signals were carefully designed to match. More likely the small phase offset observed in these simulations was caused by sub-threshold leakage current from the NMOS clamp, MClp. Table 3.8 shows the phase offset measured for each simulated PVT corner.

PVT Corner	Phase Offset
SS	4.44º
SF	3.15º
TT	3.15º
FS	3.15º
FF	2.45º

Table 3.8 Charge Pump Phase Offset

Figure 3.6 shows the amount of charge that is added to the loop filter capacitor per pump-up pulse relative to the loop filter voltage in the SS simulation corner when CLK_{div} lags CLK_{ref} by 10º. Similarly, Figure 3.7 shows the amount of charge that is removed from the loop filter capacitor per pump-down pulse relative to the loop filter voltage in the SS simulation corner when CLK_{div} lags CLK_{ref} by 10º. It can be seen from

these figures that the amount of charge added or subtracted by the charge pump is remarkably constant over a wide range of loop filter voltages, which includes the expected range during normal operation. However the charge pump is unable to add charge to the loop filter capacitor for voltages near the vdda supply rail and unable to remove charge from the loop filter capacitor for voltages near the vssa supply rail in the SS PVT corner.

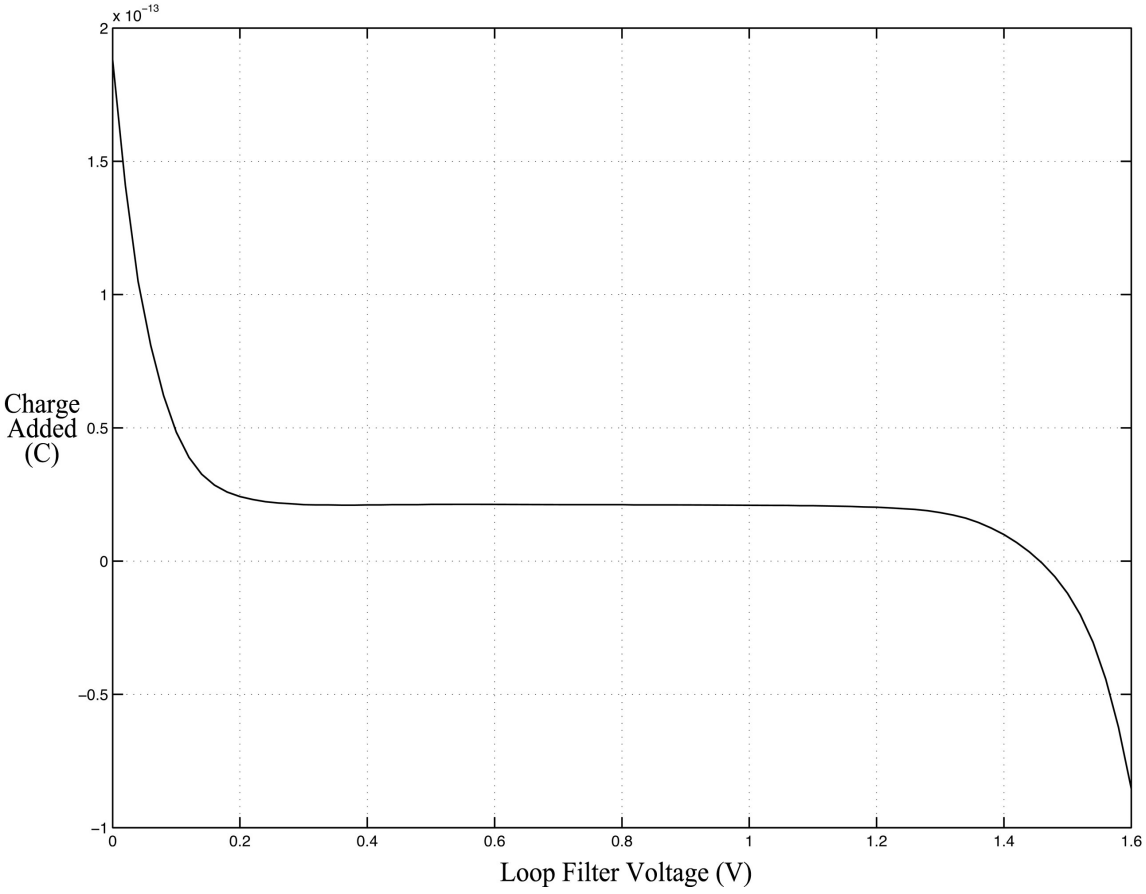


Figure 3.6 Charge Added vs. Loop Filter Voltage while Pumping Up (SS Corner)

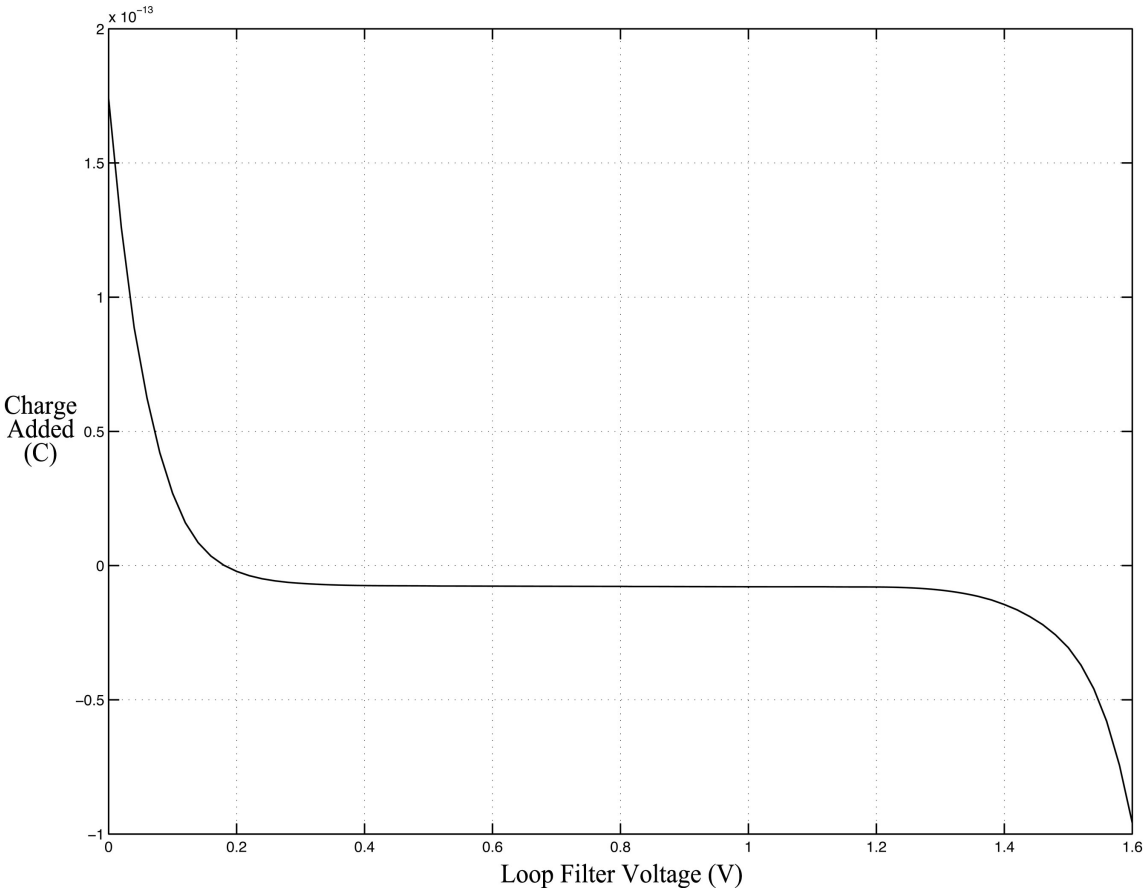


Figure 3.7 Charge Added vs. Loop Filter Voltage while Pumping Down (SS Corner)

Previous simulations run before the addition of the NMOS clamp showed that for low loop filter voltages the charge pump would actually remove charge from the loop filter capacitor while trying to pump-up in some simulation corners. In Figure 3.6 this would have looked like a dip in the curve below zero for loop filter voltages in the range of 80 – 320 mV in the FF corner and 80 – 190 mV in the TT, SF and FS corners. This non-monotonic behavior would have prevented the PLL loop from recovering should the loop filter voltage ever drop into this range, such as when the chip is first powered on. The NMOS clamp, MClp was added to prevent this from happening, by preventing the

loop filter voltage from ever dropping this low. MClp was biased such that low loop filter voltages cause this clamp transistor to turn on and add charge to the loop filter capacitor in order to increase the loop filter voltage. Figure 3.8 shows the drain current of MClp over a range of loop filter voltages. Note that this clamp transistor will only turn on if the loop filter voltage goes too low, and so it does not interfere with the normal operation of the PLL.

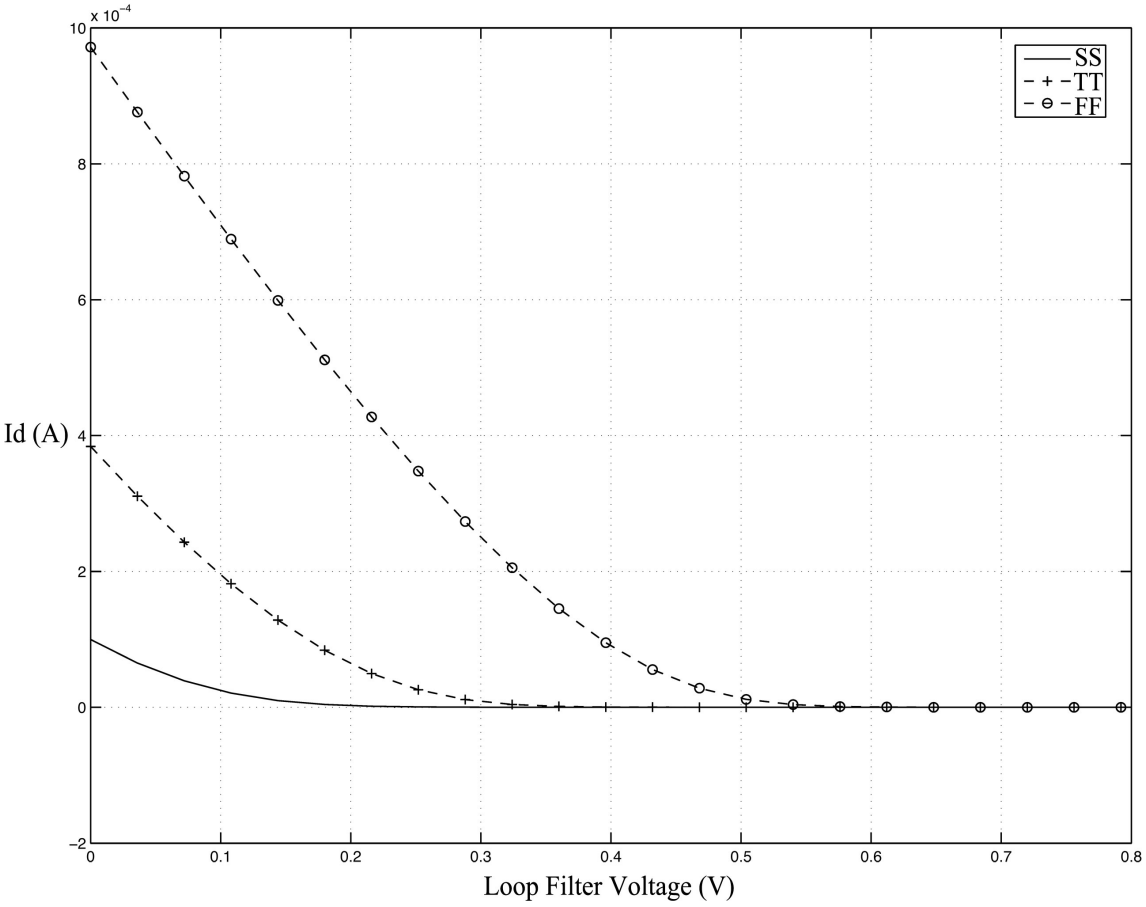


Figure 3.8 NMOS Clamp Drain Current Across Corners

Transient simulations were performed in order to observe the behavior of the loop filter voltage near the supply rails while the charge pump is either continuously pumping up or continuously pumping down. Figure 3.9 shows the loop filter voltage approaching a maximum value as CLK_{div} steadily lags CLK_{ref} by 60º in the SS PVT corner. Similarly, Figure 3.10 shows the loop filter voltage approaching a minimum value as CLK_{div} steadily leads CLK_{ref} by 60º in the SS PVT corner. Table 3.9 summarizes these maximum and minimum voltages across all PFT corners.

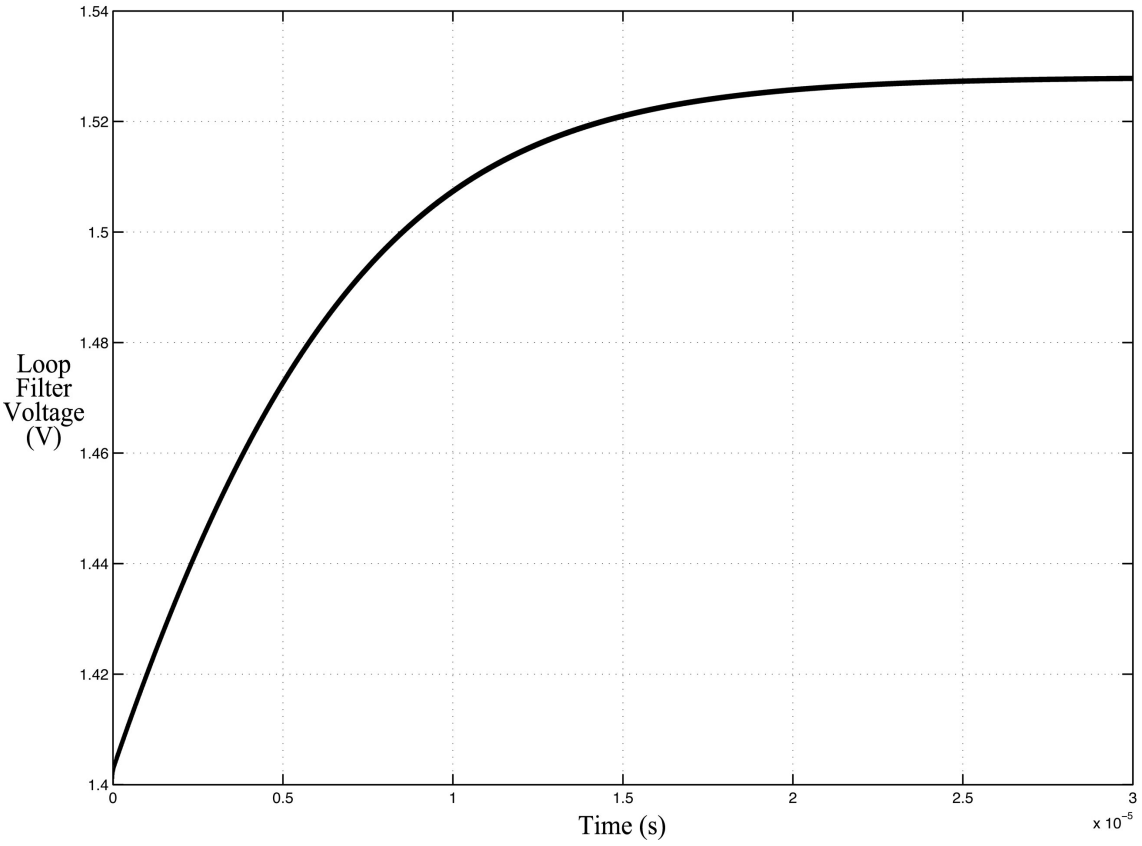


Figure 3.9 Loop Filter Voltage Upper Limit (SS Corner)

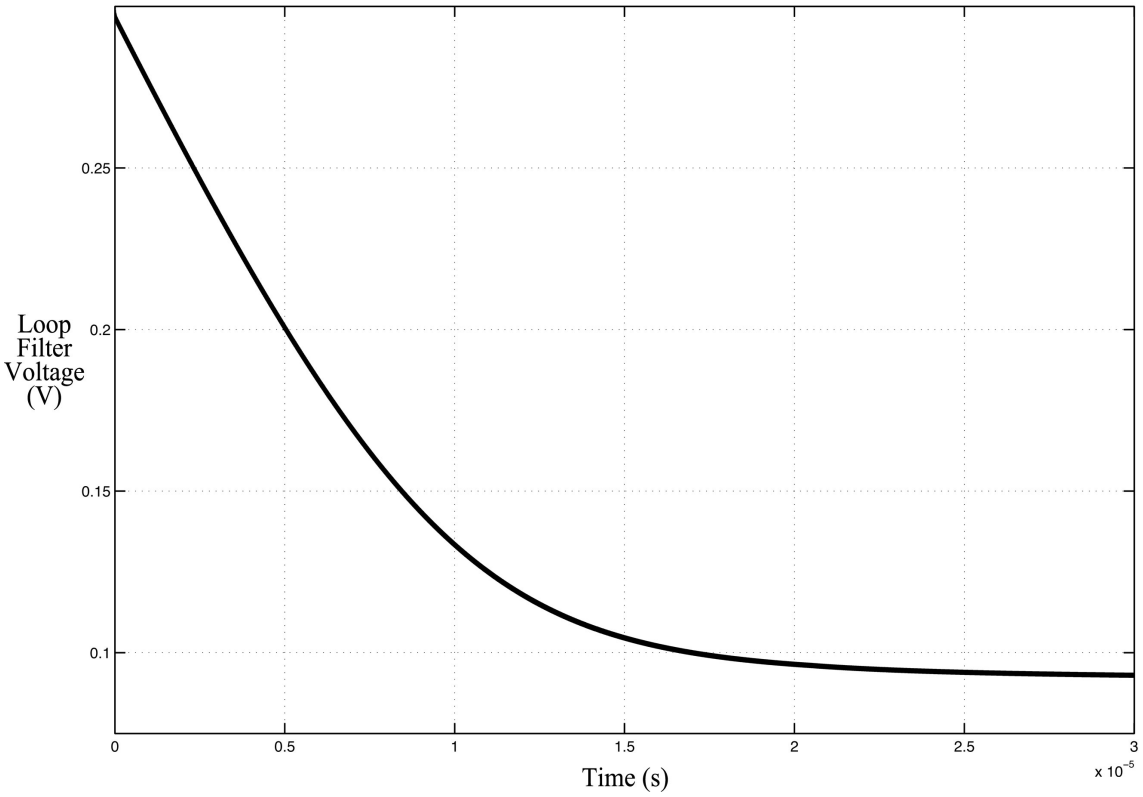


Figure 3.10 Loop Filter Voltage Lower Limit (SS Corner)

PVT Corner	Max	Min
SS	1.527 V	93 mV
SF	1.743 V	199 mV
TT	1.744 V	199 mV
FS	1.742 V	199 mV
FF	1.95 V	359 mV

Table 3.9 Loop Filter Voltage Limits

Chapter 4

CONCLUSIONS

The phase frequency detector and charge pump for a phase-locked loop in 0.18µm CMOS were successfully designed and simulated. The design of the NAND-based phase frequency detector demonstrated the operation of a digital circuit that is able to accurately detect phase and frequency differences between two clock signals. The potential problem of a "dead zone" in the PFD response was avoided through the addition of extra inverter delays in the reset path. During the charge pump design current-mode logic buffers were used to limit the output signal swing from the PFD in order to keep the input transistors of the charge pump in saturation. Wide-swing cascode current mirrors were used for the charge pump current sources because of their high output resistance, which reduces variations in the charge pump output currents as the loop filter voltage changes. A two-stage operational amplifier was used as a unity gain buffer to keep the voltages on both sides of the charge pump approximately the same, as well as to source or sink the pump-up and pump-down currents as needed as the charge pump switches. An NMOS clamp was used to eliminate the non-monotonic behavior observed when the loop filter voltage went outside of its normal range of operation. The PFD and charge pump were simulated together and shown to exhibit minimal phase offset across PVT corners. They also delivered a consistent amount of charge to the loop filter over the entire range of loop filter voltages expected during normal operation.

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