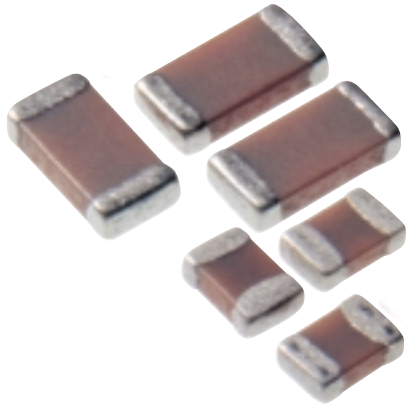
Application note

DC, AC and Pulse Load of Multilayer Ceramic Capacitors



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DC, AC and Pulse Load of Multilayer Ceramic Capacitors

CONTENTS

Introduction

General introduction

Multilayer Ceramic Capacitors (MLCCs) are increasingly being used in applications in which the electrical load becomes critical. This publication is particularly concerned with the susceptibility of MLCCs to:
- DC electrical fields
- AC electrical fields at various frequencies, and
- pulse loads

The resistance to these types of load is important for application areas such as automotive and lighting and in switched-mode power supplies. The use at elevated temperatures in some applications adds further demands.

This application note presents typical data that may help the application engineer in selecting the optimal product. The aim is to present general rules concerning the immunity to given electrical loads. The MLCC insulation resistance was used as a criterion to check the immunity against a given electrical load.

The data, however, is not relevant for all applications and we recommend that customers use the application questionnaire in the Annex, for special questions.

Before going into details of the various tests, we present some general information important for a proper understanding of the various failure mechanisms.

First we shall describe MLCC construction and present structural parameters that determine resistance to electrical breakdown.

Three types of breakdown mechanism are then discussed: *dielectric breakdown, electro-thermal breakdown* and *electro-mechanical breakdown*.

Construction

An MLCC comprises several layers of non-fired stacked ceramic foils on which electrode material is printed. These foils are pressed and sintered to obtain a compact multilayer structure.

The capacitance of an MLCC depends on the capacitive area of each electrode (A_e), on the number of inner electrodes (N_e), the thickness of the ceramic dielectric (d) and on the relative dielectric constant of the ceramic material (ε_r):

$$C = \frac{\varepsilon_0 \varepsilon_r (N_e - 1) A_e}{d} \qquad (1)$$

MLCCs in a series with a given rated voltage have a related minimum dielectric thickness. The dielectric thickness is greatest for high-voltage products and may also be larger for low-capacitive MLCCs in general.

Figure 1 shows a typical construction. An electrical load will give rise to an electric field across the dielectric as well as across the various creepage paths (margins). The three types of margin are: the end margin, the side margin and the cover layer thickness (see Fig.1). The magnitude of these margins is great compared with the dielectric thickness. Hence only the dielectric layers form a potential breakdown pathway.

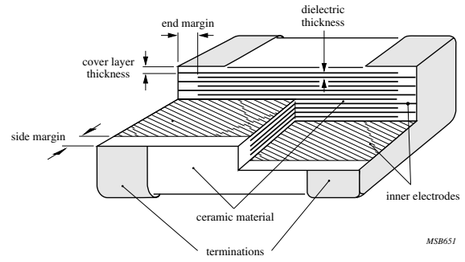


Fig.1 Construction of a ceramic multilayer capacitor

Dielectric breakdown

The MLCC may show *dielectric breakdown* at very strong field strengths. The component may fail because of the limited intrinsic dielectric strength of the ceramic material.

This failure mechanism is related not only to the quality of the ceramic dielectric material but also to the dielectric thickness d (the field strength is inversely proportional to d) and the area of the dielectric.

With the actual MLCC constructions in a given voltage series (as referred to above), there is no simple relation between the dielectric breakdown and capacitance. At lower capacitances, the larger dielectric thickness and the higher total effective capacitive surface may have opposing effects on the dielectric breakdown voltage.

Electro-thermal breakdown

High local temperatures caused by power dissipation may result in electro-thermal breakdown. The ambient temperature is an important factor here. Additionally, electro-thermal breakdown is influenced by the heat generated inside the MLCC and by the heat flow to its surroundings. The heat generated inside the MLCC depends on the dissipation factor (which is a function of temperature, frequency, voltage and construction), on the voltage amplitude, the voltage-time relation (e.g. the frequency of an AC load) and the capacitance.

The heat flow to the surroundings of an MLCC may take place by conduction, radiation and convection. It depends on the MLCC geometry, the thermal conductivities of the various materials (ceramic, terminations, solder, print board material), air flow, radiation, temperature gradients and heat-transfer coefficients.

A special type of electro-thermal breakdown may occur when the voltage difference between the terminations is high enough to cause *air discharges (corona)*. These discharges on the *outer* surface of the MLCC may lead to high local currents that destroy regions in the MLCC itself ('burning spots'). Factors influencing this are:
- the form of the electrodes. Sharp points result in high electrical field gradients which may be damaging. Sharp points may be the result of bad soldering.
- air humidity and surface condition (presence of conductive surface contamination, e.g. from human skin).
- distance between the two terminations. This distance increases in the order 0402 < 0603 < 0805 < 1206 = 1210 < 1808 = 1812 .

Electro-mechanical breakdown

When piezoelectric materials are exposed to an electric field they are deformed. This has become known as the inverse piezoelectric effect. For polycrystalline ferroelectric materials, as used in Phycomp type II MLCCs (dielectric X7R and Y5V), below the Curie point the crystallites take on tetragonal symmetry. The + and - charge sites do not coincide, resulting in electric dipoles. The material is said to be composed of *Weiss domains*. Within a Weiss domain, all the dipoles are aligned, giving a net dipole moment to the domain. The directions of polarization between neighbouring domains within a crystallite can differ by 90° or 180°. Exposing the material to a strong electric field below the Curie point will result in growth of domains most nearly aligned with the field at the expense of other domains. The material will also lengthen in the direction of the field. If this change in dimension takes place slowly, the resulting stresses in the material may be relaxed. However, at fast field changes, i.e. at high dV/dt or in other words at high currents, the stresses may exceed a critical threshold value and result in electro-mechanical breakdown.

Electro-mechanical breakdown due to the ferro-electric properties of the ceramic material does not occur in MLCCs with type I ceramic material (NP0).

Power dissipation

The general equation for power dissipation upon stressing the MLCC with AC fields is

$$P = \omega C V^2_{RMS} \tan\delta \qquad (2)$$

At thermal equilibrium, the power generated inside the MLCC equals the heat transferred to the environment. This means that

$$P = R_{th}.\ \Delta T \qquad (3)$$

in which R_{th} is the thermal resistance for heat transfer to the environment by conduction, radiation and convection in K/W and ΔT is the temperature rise of the MLCC in K. From equations (2) and (3) it follows that the temperature rise of an MLCC caused by an AC load of voltage V at a given frequency will, in theory, be proportional to V^2_{RMS}. This has been found for type I MLCCs, not for type II MLCCs, in which tanδ is a function not only of frequency but also of applied voltage and temperature.

DC load

An MLCC loaded at increasing voltages will finally break down because of the limited dielectric strength. This failure mechanism has been treated in the preceding chapter.

Figures 2 to 5 present experimental data on the DC instant breakdown voltage. In these figures, exposure time is about 5 s. Breakdown after prolonged exposure will be somewhat lower. Corona effects may occur at higher voltage levels, especially when testing smaller sized products such as 0603 and 0805.

Typical breakdown voltages of products with a rated voltage ≥ 50 V are above 1.5 kV for NP0 and above 500 V for X7R products. NP0 type products with a construction comparable to X7R type products turn out to have superior DC immunity. As expected, DC immunity is better for products with large dielectric thickness. This is the case for high-voltage products (rated voltage 200 V, 500 V, 1 kV and 3 kV), and because of their construction, it is also the case for low capacitive products in general.

Comparable and sometimes improved DC breakdown voltages are reached for larger product sizes (1812 compared with 1206), if the capacitance, dielectric thickness and type of ceramic material are the same. Additionally, to avoid corona effects it is advisable to use MLCCs with larger termination separation lengths (1812 = 1808 > 1206), especially when using low-capacitance MLCCs.

Note that the maximum DC load is not equivalent to voltage rating, which is usually 10 to 20 times lower. In the first case, DC breakdown levels refer to the behaviour at ambient temperatures, while the voltage rating of an MLCC is determined by its behaviour at elevated temperatures (maximum specified temperature of 125 °C for both NP0 and X7R type MLCCs) and over extended periods (1000 hr at 1.5 times the rated voltage) in order to meet the international CECC requirements.

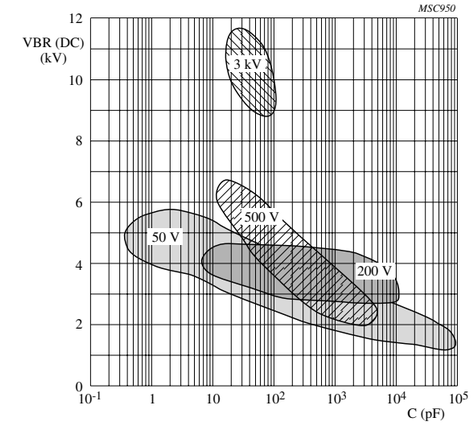


Fig.2 DC instant breakdown voltage as a function of capacitance, rated voltage and size for NP0 MLCCs. Curves through the 50% cumulative defect points are given

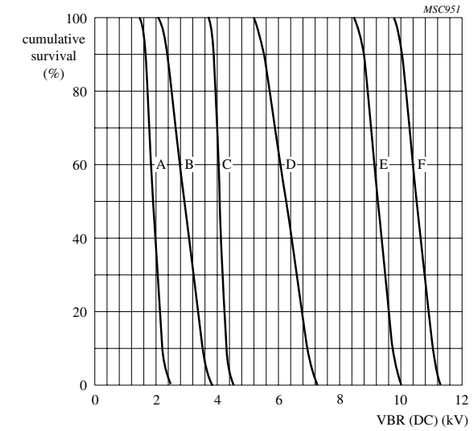


Fig.3 Typical DC instant breakdown voltage curves for NP0 MLCCs. A: 10 pF/0805/200 V, B: 1 nF/1206/50 V, C: 10 nF/1812/50 V, D: 15 pF/1206/500 V, E: 82 pF/1812/3 kV, F: 10 pF/1808/3 kV

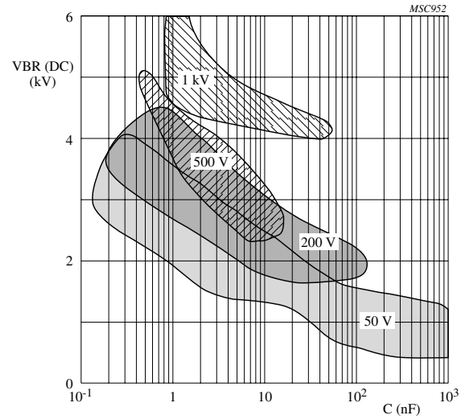


Fig.4 DC instant breakdown voltage as a function of capacitance, rated voltage and size for X7R MLCCs. Curves through the cumulative defect points are given

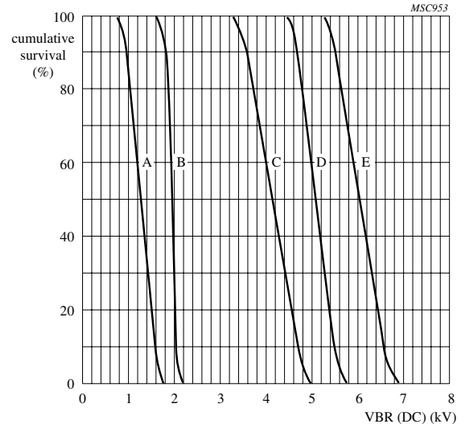


Fig.5 Typical DC instant breakdown voltage curves for X7R MLCCs. A: 47 nF/1206/50 V, B: 10 nF/1206/50 V, C: 330 pF/1206/50 V, D: 470 pF/1206/500 V, E: 1 nF/1808/1 kV

AC load

The AC immunity levels presented below are not specified but represent typical values.

AC breakdown is observed as a strong drop in the insulation resistance. The voltage level is used as an indicator only, because V and I are related.

Figures 6 and 7 show AC breakdown curves at 50 Hz as a function of the MLCC capacitance. There is a very close correspondence between the data presented here and the DC immunity data presented in the previous chapter.

Also here, increased immunity is found for lower capacitance MLCCs at higher rated voltages. NP0 type MLCCs of comparable construction are superior to X7R type MLCCs.

Figures 8 and 9 show AC breakdown levels as a function of frequency. The AC instant breakdown curve as a function of frequency can be divided into two regions:

- At low frequencies (below roughly 1 to 50 kHz), the breakdown level is nearly independent of frequency. Breakdown occurs because of the *limited dielectric strength* of the ceramic material and possibly because of electro-mechanical effects.
  The AC RMS instant breakdown level is about 35% of the DC instant breakdown level.
- At frequencies roughly above 1 to 50 kHz, breakdown occurs at decreasing voltage levels because of *energy dissipation*.

Figure 10 shows temperature rise as a function of voltage at higher frequencies for 1 nF 0805 50 V NP0 and X7R MLCCs. The temperature rise of NP0 MLCCs is less than that of X7R MLCCs under the same conditions. This is due to the lower loss factor of NP0 capacitors. Note that for NP0 types, temperature rise is more or less proportional to frequency and the square of the voltage as given in equations (2) and (3). The temperature rise of X7R types deviates from this behaviour. The data suggests that tanδ decreases with temperature and applied field which has indeed been found for X7R types.

Note: for both AC and DC loads, the use of higher rated voltage MLCCs (200 and 500 V) is generally recommended instead of the standard 50 V products.

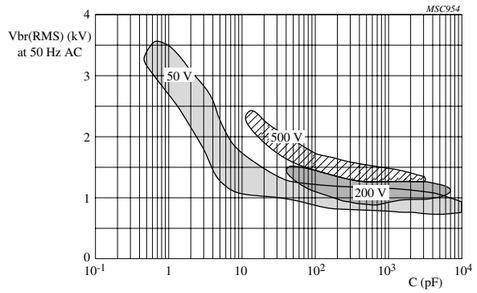


Fig.6 AC instant breakdown voltage as a function of capacitance, rated voltage and size for NP0 MLCCs. AC frequency: 50 Hz. Curves through the 50% cumulative defect points are given

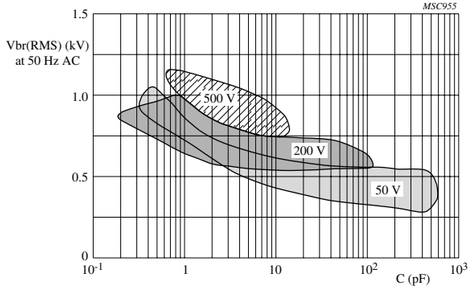
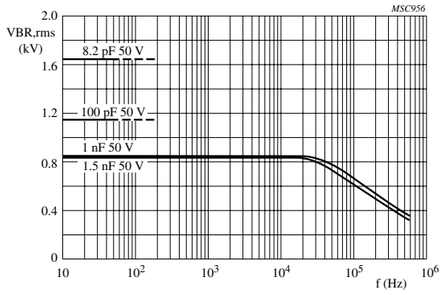
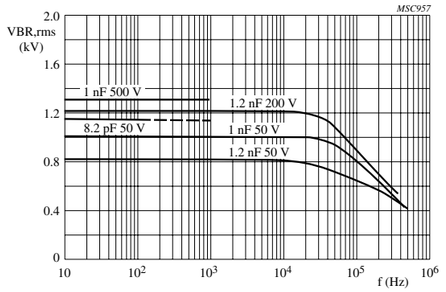


Fig. 7 AC instant breakdown voltage as a function of capacitance, rated voltage and size for X7R MLCCs. AC frequency: 50 Hz. Curves through the 50% cumulative defect points are given

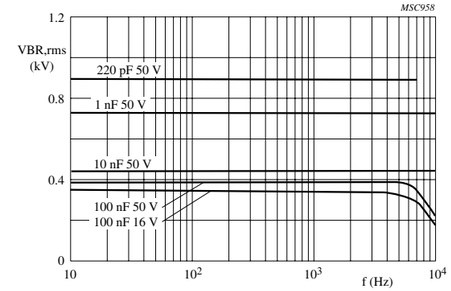


(a)

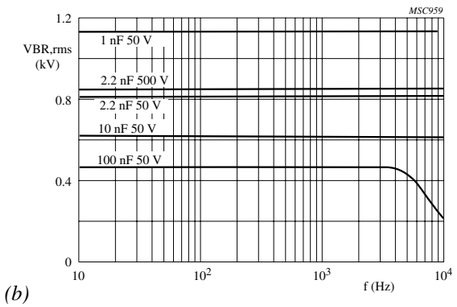


(b)

Fig. 8 AC instant breakdown voltage as a function of AC frequency for NP0 MLCCs. Curves through the 50% cumulative defect points are given. (a) 0805, (b) 1206



(a)



(b)

Fig. 9 AC instant breakdown voltage as a function of AC frequency for X7R MLCCs. Curves through the 50% cumulative defect points are given. (a) 0805, (b) 1206

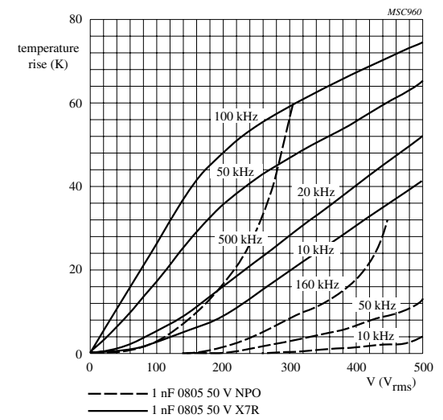


Fig.10 Example of MLCC temperature rise as a function of AC voltage for 1 nF 0805 50 V NP0 and X7R MLCCs

Pulse load

This section discusses the immunity of MLCCs to various types of transient. Three different groups of transient can be considered:

rise-time	energy level	relevant test
fast (1 ns)	low (µJ-mJ)	ESD
slow (1 µs)	medium (1-10 s of mJ)	automotive pulses
slow (0.1-10 µs)	high (1-100 s of J)	surge tests

The various pulses cover the whole spectrum from fast and low-energy pulses to slow and high-energy pulses.

ESD pulses

Electrostatic Discharge (ESD) of persons or electrically-loaded objects is a well known threat to the optimal behaviour of electronic equipment.

Nowadays, all equipment brought onto the market, put into operation or already in production in countries within the European Union must comply with EMC (ElectroMagnetic Compatibility) requirements on both emission and immunity. One of the immunity requirements concerns ESD. Although there is no such requirement for components, their behaviour will influence the behaviour of the equipment in which they operate.

The immunity of MLCCs to ESD pulses is not well characterized. Tests were therefore performed to analyze the effect of these *fast* and *low-energy* pulses. Pulse tests were performed according to two standards: MIL-STD 883C *(Human Body Model)* and UZW-BO/FQ-B302 *(Machine Model)* developed by Philips. These standards were originally developed for the ESD testing of semiconductors and we have adapted the test methods to make them suitable for MLCCs. The tests were performed on an adapted Verifier test apparatus. MLCCs soldered onto IC substrates were subjected to six positive pulses per test run. These pulses were applied by direct contact rather than by air discharge. A discharging step, not specified in the original standards, was added between each pulse. (Negative pulses were not applied owing to the apolarity of the MLCCs).

When subjected to ESD pulses, low-capacitance MLCCs sometimes exhibited corona effects without internal damage. In these cases, the products were immersed in oil (Dow Corning fluid 550) to obtain the immunity data.

Human Body Model pulses according to MIL-STD 883C.
These pulses simulate the discharge of an electrically-loaded human body by using a discharge circuit with a capacitor of 100 pF, a resistance of 1.5 kΩ and an inductance of 7.5 µH (not specified in the standard but derived from pulse characteristics).

Figure 11 shows a typical pulse form. The pulse rise time t_{ri} is less than 10 ns, the delay time t_d is 150 ns, the peak current at 2 kV is 1.25 A (short circuit) and at 4 kV it is 2.5 A (short circuit). I_r caused by ringing must be less than 5% of the peak current. The voltage level is 0 to 10 kV.

In Fig.12 the ESD immunity has been given for NP0 and X7R type MLCCs tested according to the MIL-STD 883C standard.

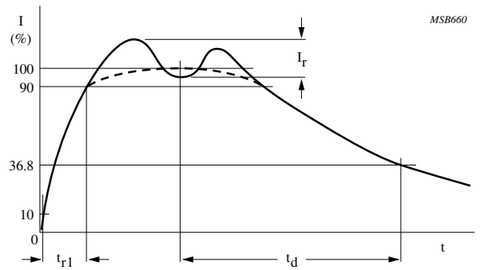


Fig.11 Typical ESD pulse based on the Human Body Model according to MIL-STD 883 C

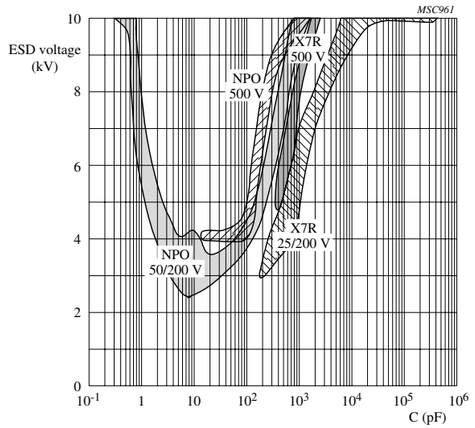


Fig.12 Experimental data on ESD immunity of NP0 and X7R MLCCs of size 0805 and 1206 based on Human Body Model pulses according to MIL-STD 883C

Machine Model pulses according to the Philips standard UZW-BO/FQ-B302.
These pulses simulate the discharge of an electrically-loaded machine by using a discharge circuit with a capacitor of 200 pF, a resistance of only 25 Ω and an inductance of 2.5 µH (not specified in the standard, but derived from pulse characteristics).

A typical pulse form is presented in Fig.13. It is the calibration-current waveform for a charged voltage of 400 V. The first peak current I_{p1} is 3 A. The damping I_{p1}/I_{p2} is 1.4. The resonant frequency is 7.1 MHz. The voltage level is 0 to 2 kV.

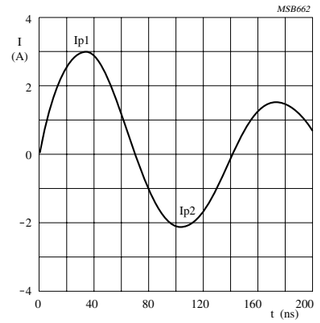


Fig.13 Typical ESD pulse based on the Machine Model according to standard UZW-BO/FQ-B302 developed by Philips

Figure 14 gives data on ESD immunity for NP0 and X7R type MLCCs tested according to the Machine Model standard. Several types of 25, 50, 200 and 500 V products in NP0 and X7R ceramic were measured. All products were resistant to at least 2.5 kV HBM and 1 kV MM pulses. 0805 and 1206 products showed the same behaviour.

The advantage of the high-voltage products (rated voltage 500 V) is clear when comparing the 50 V data with the 500 V data since higher immunity levels are obtained for the high-voltage products.

The experimental data presented in Figs 12 and 14 show that energy dissipation is highest (and the ESD breakdown voltage level is lowest) when the tested MLCC has a capacitance close to the capacitance of the discharge circuit. This is in line with our model calculations. Moreover, the figures show that the X7R data seems to be shifted somewhat to higher capacitance values compared with the NP0 data. This may be due to the voltage-dependent capacitance of X7R products, which causes a lowering of capacitance at higher DC voltage levels. Additionally, the ESD immunity of X7R products is found to be lower than that of NP0 products with the same capacitance and rated voltage.

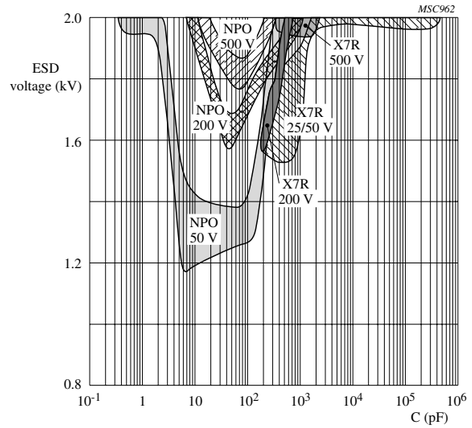


Fig.14 Experimental data on ESD immunity of NP0 and X7R MLCCs based on Machine Model pulses according to Philips standard UZW-BO/FQ-B302. Size 0805 and 1206

Automotive pulses
Other pulses relevant for MLCC applications are the so-called *automotive pulses*. Compared with ESD pulses, treated in the previous section, these pulses are characterized by slower rise times but higher energies.

Automotive pulses are generally characterized in the international standards DIN 40839, ISO/TR 7637/1 and SAE J1113. The immunity tests in these standards are aimed at determining the ability of various electrical devices to withstand transients that normally occur in motor vehicles. Transients can be added to the standard electrical voltage of 12 V or 24 V, caused, for example, by the release of stored energy during start and turn off of vehicles. These are general tests, not for MLCCs only.

No defects were found after testing NP0 and X7R products with a minimum rated voltage of 50 V and a size of 1206 and larger. This concerns test pulses no. 1, 2, 3a and 3b, mentioned in the various standards.

With the exception of the DC offset (U_p in Fig.15), these pulses were produced with a Schaffner NSG 500/B14 pulse generator.

The maximum absolute value of the peak voltage mentioned in the standard documents was 200 V for single pulses and pulse trains. In our tests we were able to over stress samples to a 350 to 500 V level and an average dV/dt of 500 V/µs, without failure.

The automotive pulses according to DIN 40839 part I, ISO/TR 7637/1 and SAE J1113 are characterized as follows:

Single pulses, pulse 1 and 2. A typical pulse form is given in Fig.15(a). The vehicle power supply voltage U_p is 12 or 24 V. The rise time t_r is in general 1 µs. The pulse voltage U_s is -100 V (pulse 1, U_p = 12 V) or -200 V (pulse 1, U_p = 24 V) or +100 V (pulse 2, U_p = 12 V, 24 V). The pulse duration t_d is 50 µs. The cycle time t_1 is 0.5 - 5 s. The number of pulses is 5000 or higher.

Pulse train, pulse 3a and 3b. A typical pulse form is given in Fig.15(b). The vehicle power supply voltage U_p is 12 or 24 V. The rise time t_r is 5 ns. The pulse voltage U_s is +100 V (pulse 3b, U_p = 12 V), +200 V (pulse 3b, U_p = 24 V), -150 V (pulse 3a, U_p = 12 V) or -200 V (pulse 3a, U_p = 24 V). The pulse duration t_d is 0.1 µs. The cycle time t_1 is 100 µs. The pulse train duration t_4 is 10 ms (100 pulses). The delay time t_5 is 90 ms. The duration of the test is 1 hour or longer (36000 pulse trains).

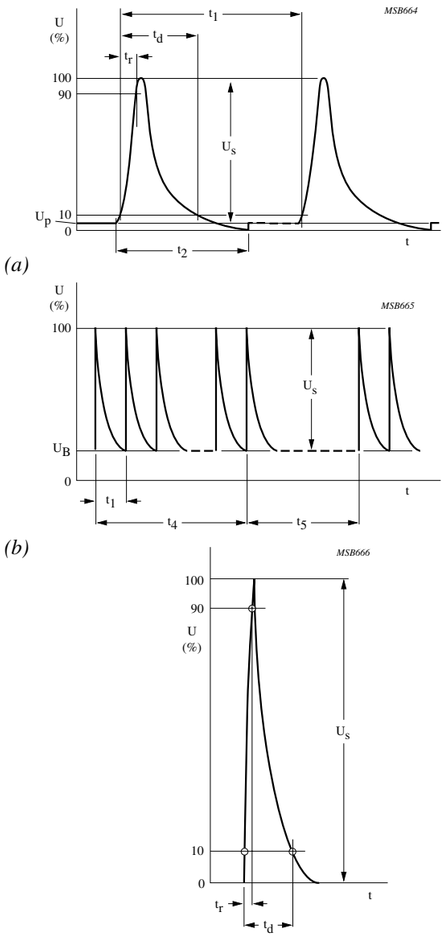


Fig.15 Automotive pulses. (a) single pulses, pulses 1 and 2; (b) pulse train, pulses 3a and 3b

Surge pulses

Surge pulses are high-energy pulses caused by the switching of inductive or capacitive loads and (of less importance to multilayer capacitors) lightning. A standardized pulse is the so-called 1.2/50 µs surge pulse. The pulse rise time is roughly 1 µs, comparable to the single automotive pulses treated above. The pulse duration is 50 µs. The voltage level, *up to 4 kV*, is much higher than the voltage level used in automotive pulses. The 1.2/50 µs surge pulses are standardized according to IEC 1000-4-5.

So called 1.2/50 µs pulses are given with the typical pulse form shown in Fig.16. The front time t_1 equals $1.67 \times t_3 = 1.2$ µs, the time to half value t_2 is 50 µs, the voltage U ranges from 0 to 4 kV and the pulse repetition frequency is 160 ms.

NP0 products of rated voltage 50, 200 and 500 V and size 1206, and X7R products of rated voltage 16, 25, 50, 200 and 500 V and size 0805, 1206 and 1812 were treated with a 1.2/50 µs surge pulse. The pulses were generated by an EM TEST USC 500 immunity-test generator.

Figures 17 and 18 give the surge immunity level of the products referred to as a function of capacitance and dielectric thickness respectively. Long-term treatment is expected to result in somewhat lower immunity levels. The usual picture arises from the initial breakdown experiments, also seen after DC and AC load i.e. higher immunity levels are obtained

- for lower capacitance products,
- for higher rated voltage MLCCs (greater dielectric thickness),
- for NP0 products compared with X7R products with identical dielectric thickness.

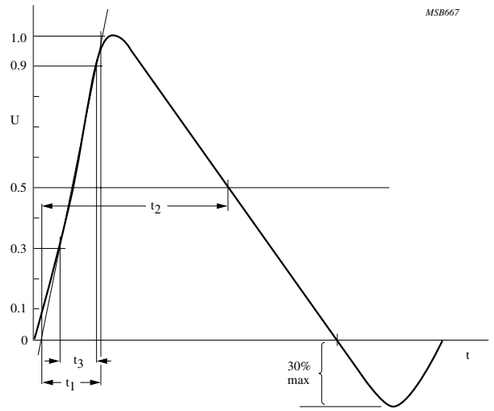


Fig.16 1.2/50 µs surge pulses

We have found a clear relationship between the breakdown peak voltage and the dielectric thickness of the measured products.

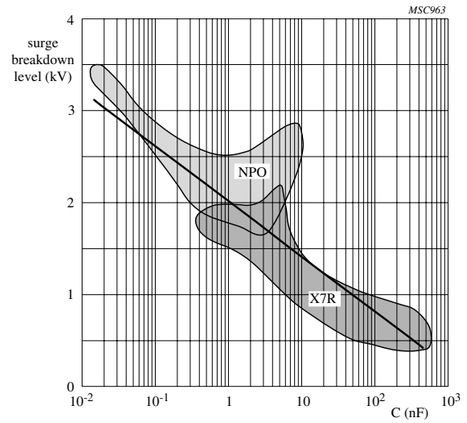


Fig.17 Instant breakdown peak voltage as a function of capacitance for NP0 and X7R products treated with 1.2/50 µs surge pulses. NP0 products: rated voltage 50, 200 and 500 V, size 1206; X7R products: rated voltage 16, 25, 200 and 500 V, sizes 0805, 1206 and 1812. The straight line shows the result of a linear fit of the combined NP0 and X7R data

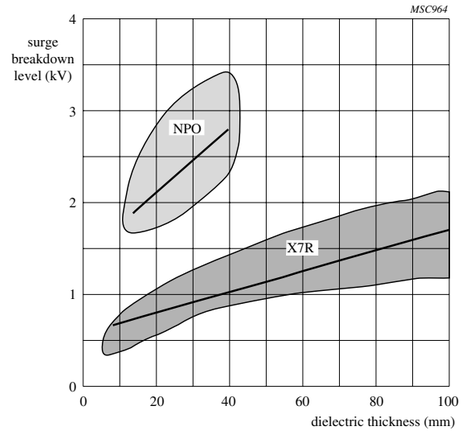


Fig.18 Instant breakdown peak voltage as a function of capacitance for NP0 and X7R products subjected to 1.2/50 µs surge pulses. The straight line shows the result of a linear fit of the combined NP0 and X7R data

ANNEX Application Questionnaire for DC, AC & Pulse Testing of MLCCs

Please complete in as much detail as you can.

1. General

Capacitance: . . . . . .pF
Tolerance: . . . . . .%
Rated voltage V

Termination: AgPd/NiSn
Dielectric material: NP0/X7R
Size: 0402/0603/0805/1206/1210/1808/1812/2220

2. Application

	Starting up/ intermittent	Continuous operation
Maximum peak voltage:	. . . . . .V_p	. . . . . .V_p
Maximum peak-to-peak voltage:	. . . . . .V_{p-p}	. . . . . .V_{p-p}
Maximum RMS voltage:	. . . . . .V_{RMS}	. . . . . .V_{RMS} RMS
Maximum peak current:	. . . . . .I_p	. . . . . .I_p
Maximum peak-to-peak current:	. . . . . .I_{p-p}	. . . . . .I_{p-p}
Frequency (main period)	. . . . . .Hz	. . . . . .Hz

Voltage waveform

t→

Current waveform

t→

3. Pulse application

Automotive pulses according to DIN 40839
pulse number: 1/2/3a/3b . .voltage level: V
ESD pulses according to MIL-STD 883C Human Body Model
number of pulses: . . . . . .voltage level: V
ESD pulses according to Machine Model
number of pulses: . . . . . .voltage level: V
Surge pulses according to IEC 1000-4-5, type 1.2/50 µs
number of pulses: . . . . . .voltage level: V
General
number of pulses: . . . . . .maximum dV/dt: . . . . . .V/µs
maximum current: . . . . . .A maximum dI/dt: . . . . . .A/µs

4. Climatic requirements

Ambient temperature: . . . . . .minimum . . . . . .°C Average . . . . . .°C maximum . . . . . .°C

5. Remarks

. . . . . .
. . . . . .

6. Name: . . . . . .

Company: . . . . . .
Address: . . . . . .
. . . . . .
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Printed in The Netherlands

Document order number: 9398 084 31011

Date of release: September 2001

www.phycomp-components.com