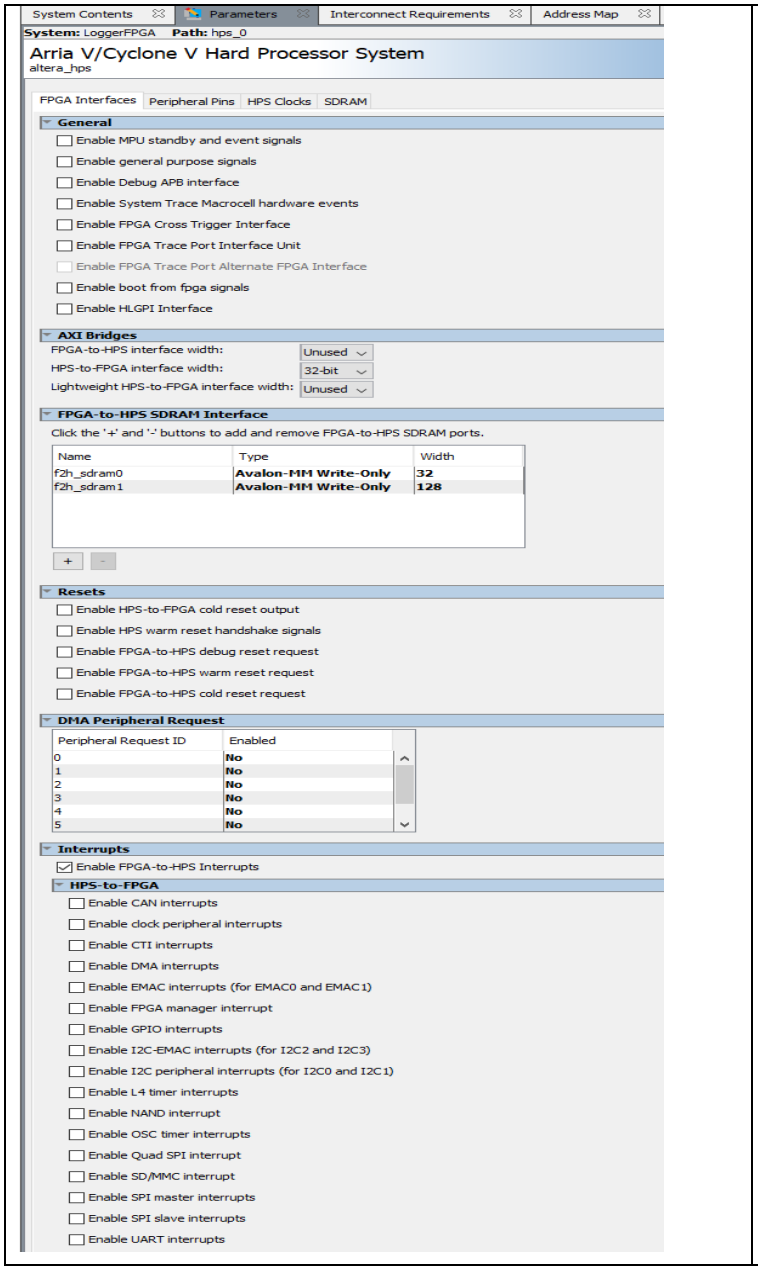
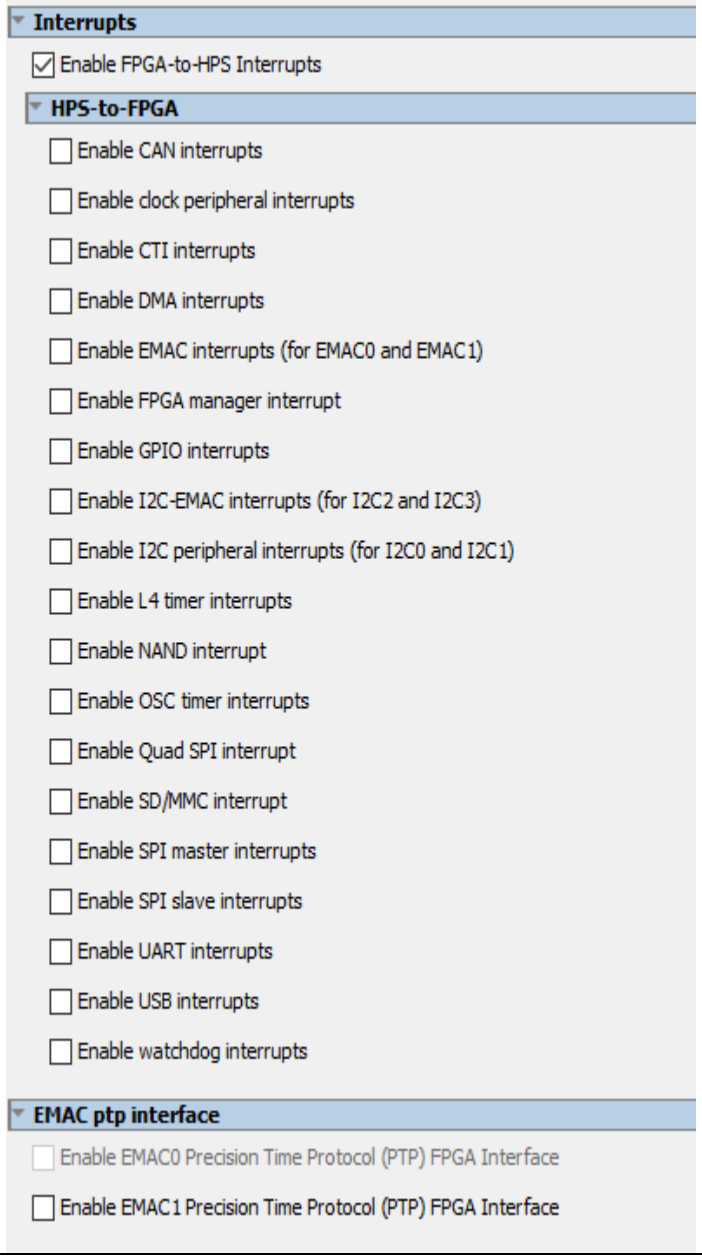
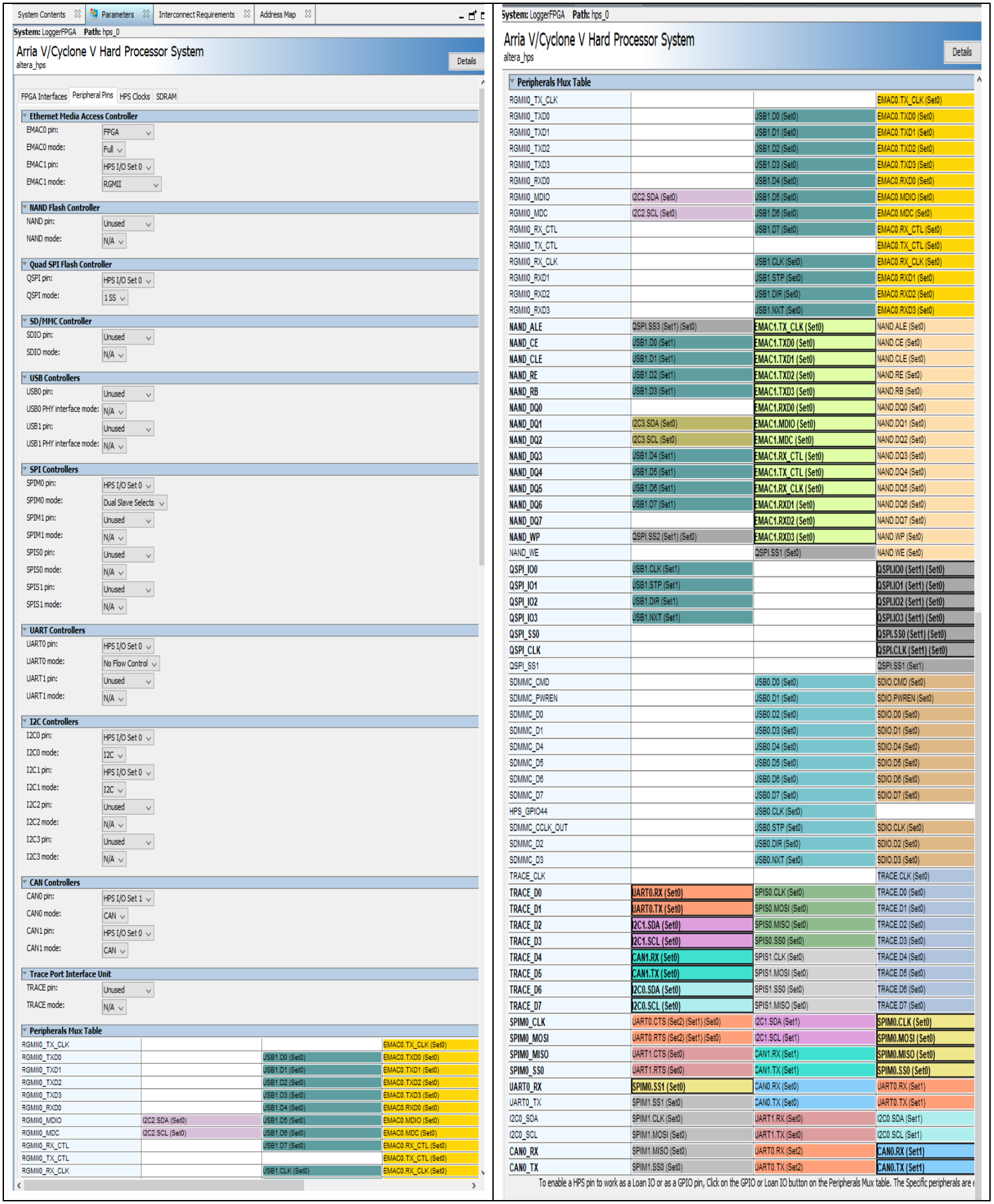
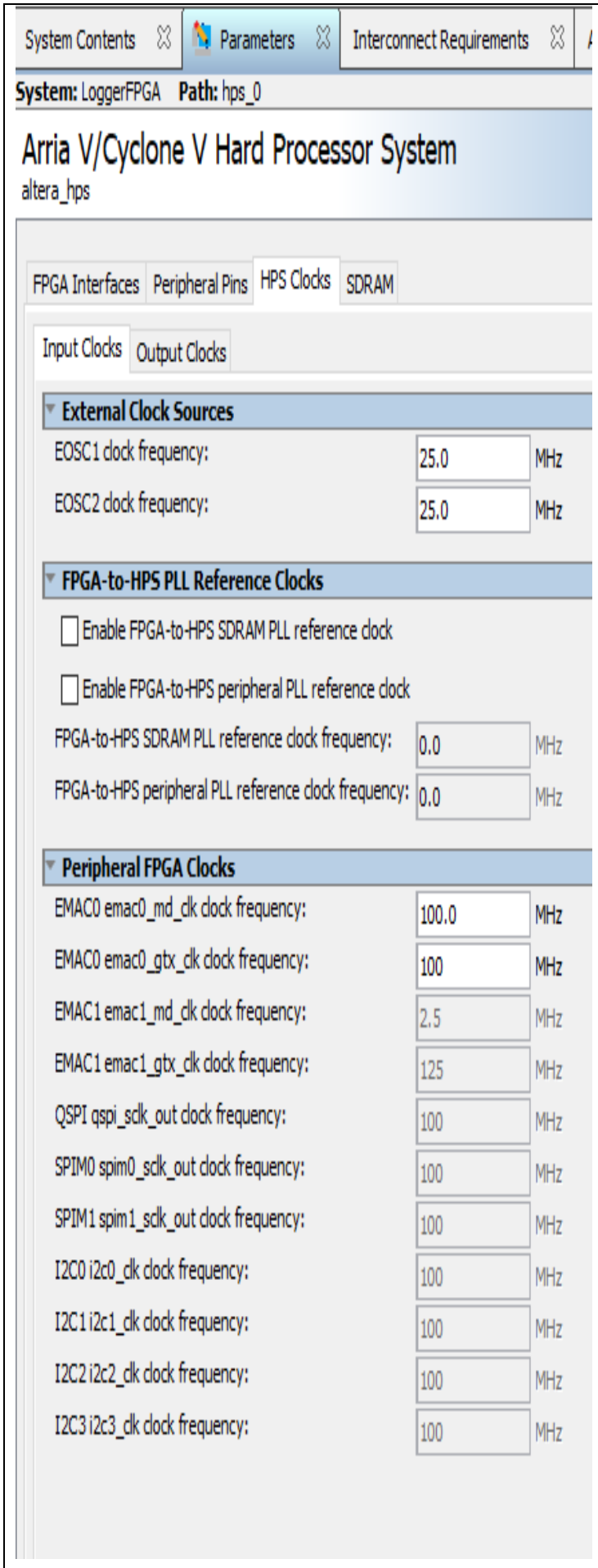
Cyclone V Hard Processor System

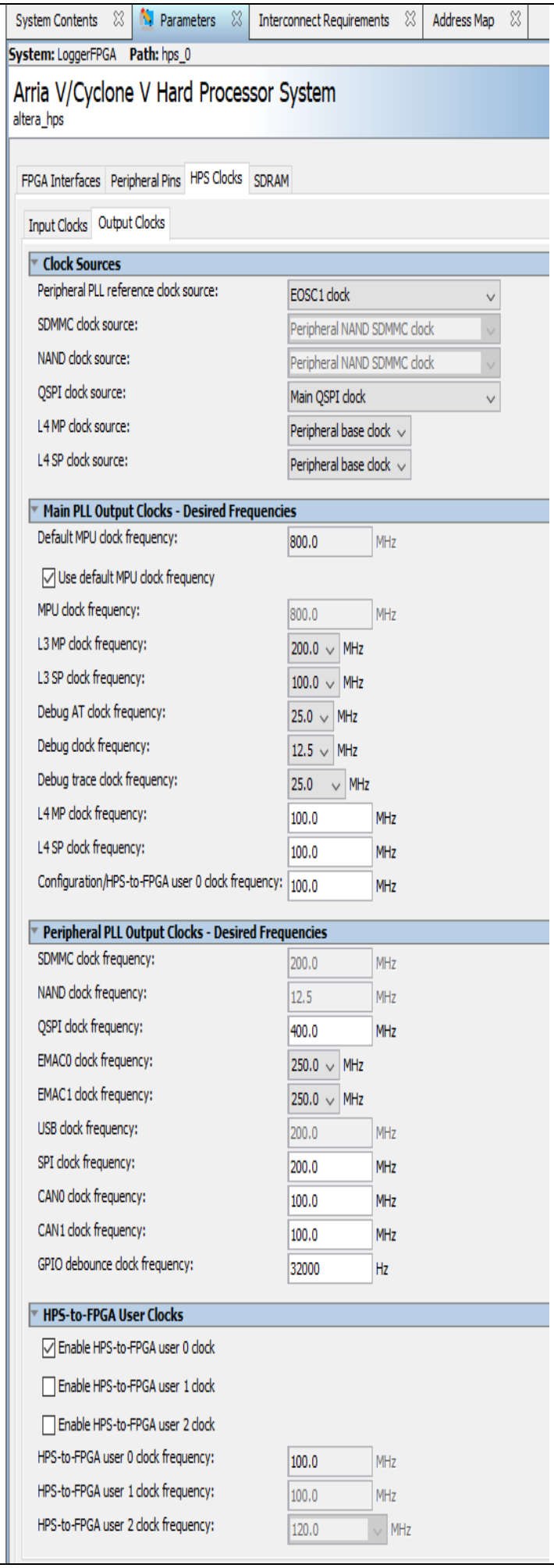
Parameters

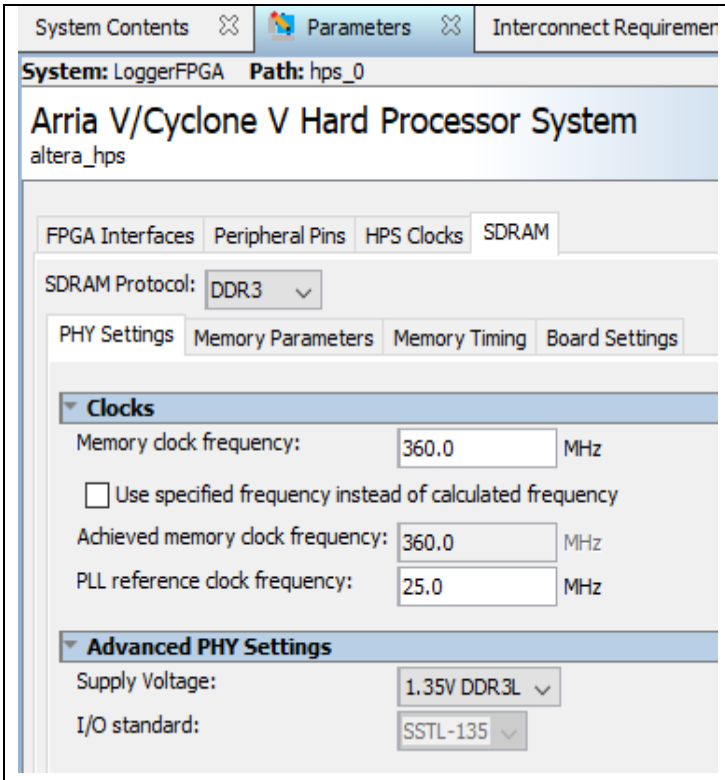


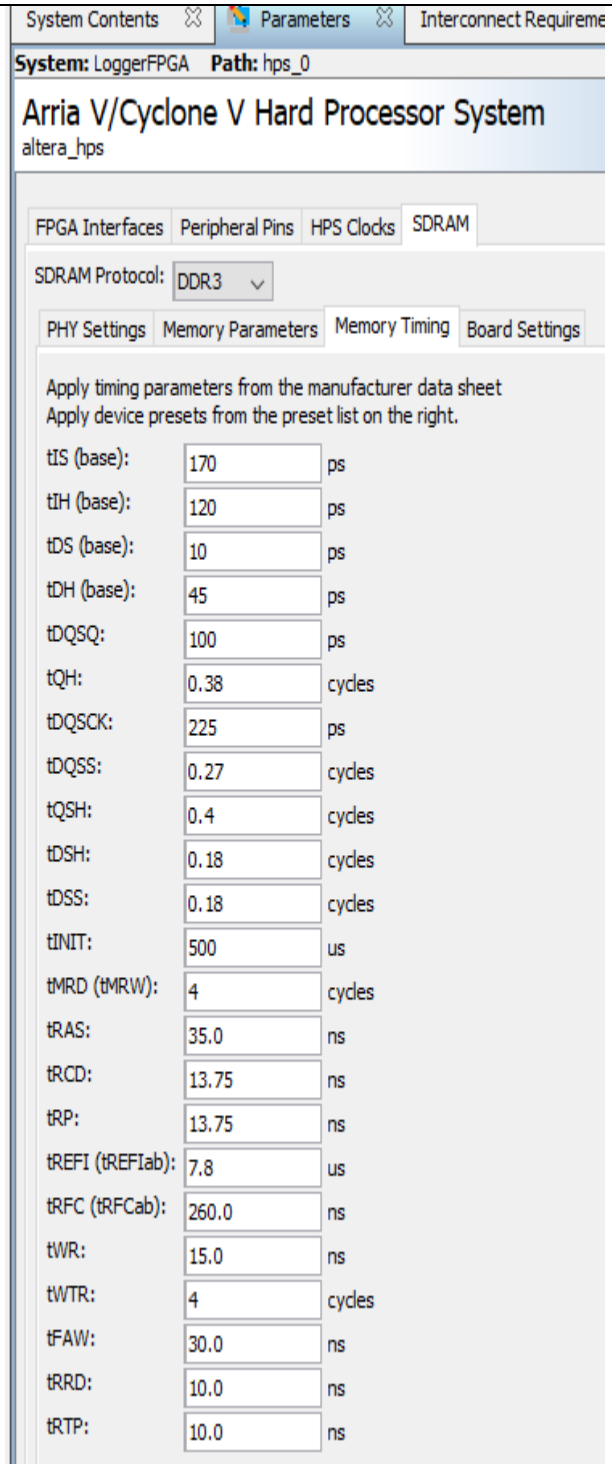


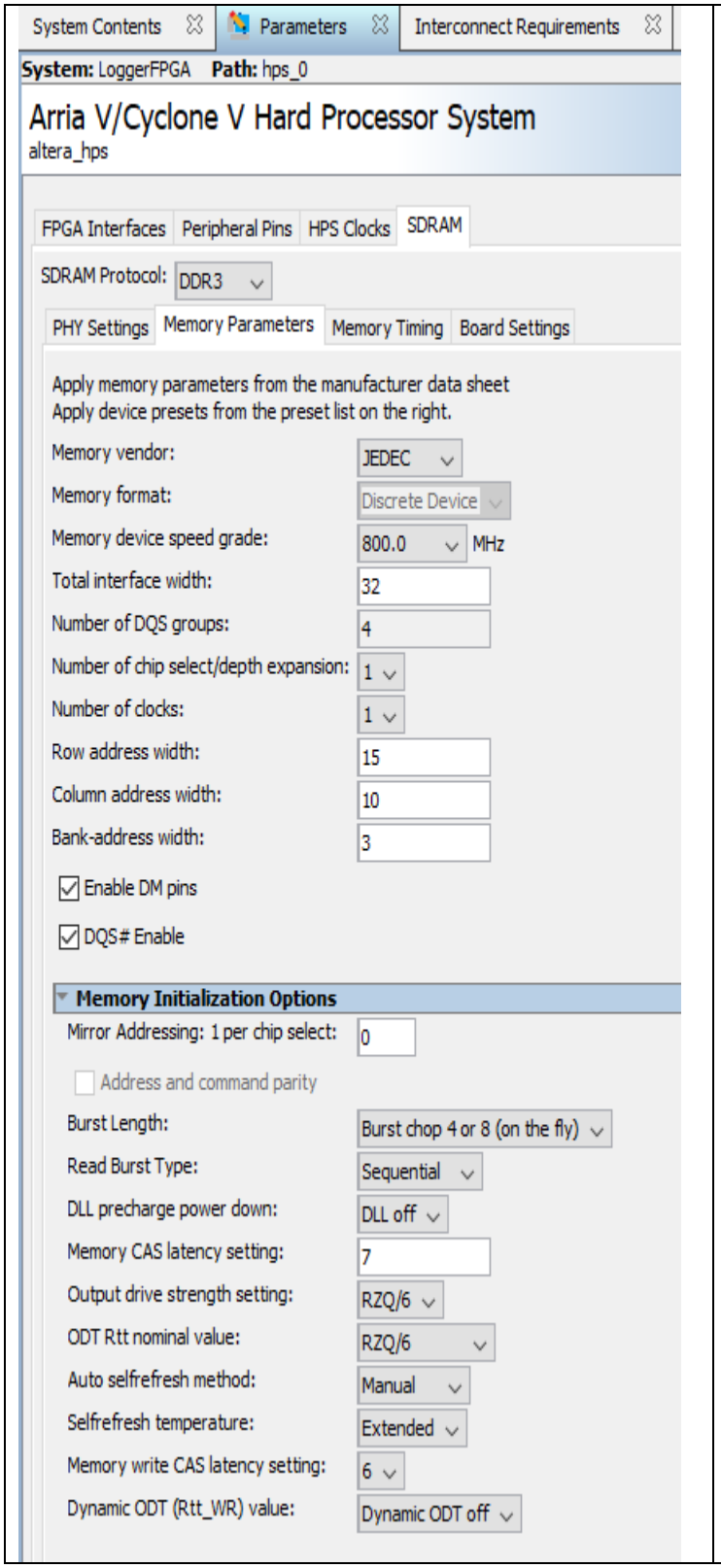

System Contents
Parameters
Interconnect Requirements
Address Map
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
Details
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
Ethernet Media Access Controller
EMAC0 pin: FPGA
EMAC0 mode: Full
EMAC1 pin: HPS I/O Set 0
EMAC1 mode: RGMII
NAND Flash Controller
NAND pin: Unused
NAND mode: N/A
Quad SPI Flash Controller
QSPI pin: HPS I/O Set 0
QSPI mode: 1 SS
SD/MMC Controller
SDIO pin: Unused
SDIO mode: N/A
USB Controllers
USB0 pin: Unused
USB0 PHY interface mode: N/A
USB1 pin: Unused
USB1 PHY interface mode: N/A
SPI Controllers
SPIM0 pin: HPS I/O Set 0
SPIM0 mode: Dual Slave Selects
SPIM1 pin: Unused
SPIM1 mode: N/A
SPIS0 pin: Unused
SPIS0 mode: N/A
SPIS1 pin: Unused
SPIS1 mode: N/A
UART Controllers
UART0 pin: HPS I/O Set 0
UART0 mode: No Flow Control
UART1 pin: Unused
UART1 mode: N/A
I2C Controllers
I2C0 pin: HPS I/O Set 0
I2C0 mode: I2C
I2C1 pin: HPS I/O Set 0
I2C1 mode: I2C
I2C2 pin: Unused
I2C2 mode: N/A
I2C3 pin: Unused
I2C3 mode: N/A
CAN Controllers
CAN0 pin: HPS I/O Set 1
CAN0 mode: CAN
CAN1 pin: HPS I/O Set 0
CAN1 mode: CAN
Trace Port Interface Unit
TRACE pin: Unused
TRACE mode: N/A
Peripherals Mux Table
RGMII0_TX_CLK EMAC0.TX_CLK (Set0)
RGMII0_TXD0 USB1.D0 (Set0) EMAC0.TXD0 (Set0)
RGMII0_TXD1 USB1.D1 (Set0) EMAC0.TXD1 (Set0)
RGMII0_TXD2 USB1.D2 (Set0) EMAC0.TXD2 (Set0)
RGMII0_TXD3 USB1.D3 (Set0) EMAC0.TXD3 (Set0)
RGMII0_RXD0 USB1.D4 (Set0) EMAC0.RXD0 (Set0)
RGMII0_MDIO I2C2.SDA (Set0) USB1.D5 (Set0) EMAC0.MDIO (Set0)
RGMII0_MDC I2C2.SCL (Set0) USB1.D6 (Set0) EMAC0.MDC (Set0)
RGMII0_RX_CTL USB1.D7 (Set0) EMAC0.RX_CTL (Set0)
RGMII0_TX_CTL EMAC0.TX_CTL (Set0)
RGMII0_RX_CLK USB1.CLK (Set0) EMAC0.RX_CLK (Set0)
RGMII0_RXD1 USB1.STP (Set0) EMAC0.RXD1 (Set0)
RGMII0_RXD2 USB1.DIR (Set0) EMAC0.RXD2 (Set0)
RGMII0_RXD3 USB1.NXT (Set0) EMAC0.RXD3 (Set0)
NAND_ALE QSPI.SS3 (Set1) (Set0) EMAC1.TX_CLK (Set0) NAND.ALE (Set0)
NAND_CE USB1.D0 (Set1) EMAC1.TXD0 (Set0) NAND.CE (Set0)
NAND_CLE USB1.D1 (Set1) EMAC1.TXD1 (Set0) NAND.CLE (Set0)
NAND_RE USB1.D2 (Set1) EMAC1.TXD2 (Set0) NAND.RE (Set0)
NAND_RB USB1.D3 (Set1) EMAC1.TXD3 (Set0) NAND.RB (Set0)
NAND_DQ0 EMAC1.RXD0 (Set0) NAND.DQ0 (Set0)
NAND_DQ1 I2C3.SDA (Set0) EMAC1.MDIO (Set0) NAND.DQ1 (Set0)
NAND_DQ2 I2C3.SCL (Set0) EMAC1.MDC (Set0) NAND.DQ2 (Set0)
NAND_DQ3 USB1.D4 (Set1) EMAC1.RX_CTL (Set0) NAND.DQ3 (Set0)
NAND_DQ4 USB1.D5 (Set1) EMAC1.TX_CTL (Set0) NAND.DQ4 (Set0)
NAND_DQ5 USB1.D6 (Set1) EMAC1.RX_CLK (Set0) NAND.DQ5 (Set0)
NAND_DQ6 USB1.D7 (Set1) EMAC1.RXD1 (Set0) NAND.DQ6 (Set0)
NAND_DQ7 EMAC1.RXD2 (Set0) NAND.DQ7 (Set0)
NAND_WP QSPI.SS2 (Set1) (Set0) EMAC1.RXD3 (Set0) NAND.WP (Set0)
NAND_WE QSPI.SS1 (Set0) NAND.WE (Set0)
QSPI_IO0 USB1.CLK (Set1) QSPI.IO0 (Set1) (Set0)
QSPI_IO1 USB1.STP (Set1) QSPI.IO1 (Set1) (Set0)
QSPI_IO2 USB1.DIR (Set1) QSPI.IO2 (Set1) (Set0)
QSPI_IO3 USB1.NXT (Set1) QSPI.IO3 (Set1) (Set0)
QSPI_SS0 QSPI.SS0 (Set1) (Set0)
QSPI_CLK QSPI.CLK (Set1) (Set0)
QSPI_SS1 QSPI.SS1 (Set1)
SDMMC_CMD USB0.D0 (Set0) SDIO.CMD (Set0)
SDMMC_PWREN USB0.D1 (Set0) SDIO.PWREN (Set0)
SDMMC_D0 USB0.D2 (Set0) SDIO.D0 (Set0)
SDMMC_D1 USB0.D3 (Set0) SDIO.D1 (Set0)
SDMMC_D4 USB0.D4 (Set0) SDIO.D4 (Set0)
SDMMC_D5 USB0.D5 (Set0) SDIO.D5 (Set0)
SDMMC_D6 USB0.D6 (Set0) SDIO.D6 (Set0)
SDMMC_D7 USB0.D7 (Set0) SDIO.D7 (Set0)
HPS_GPIO44 USB0.CLK (Set0)
SDMMC_CCLK_OUT USB0.STP (Set0) SDIO.CLK (Set0)
SDMMC_D2 USB0.DIR (Set0) SDIO.D2 (Set0)
SDMMC_D3 USB0.NXT (Set0) SDIO.D3 (Set0)
TRACE_CLK TRACE.CLK (Set0)
TRACE_D0 UART0.RX (Set0) SPIS0.CLK (Set0) TRACE.D0 (Set0)
TRACE_D1 UART0.TX (Set0) SPIS0.MOSI (Set0) TRACE.D1 (Set0)
TRACE_D2 I2C1.SDA (Set0) SPIS0.MISO (Set0) TRACE.D2 (Set0)
TRACE_D3 I2C1.SCL (Set0) SPIS0.SS0 (Set0) TRACE.D3 (Set0)
TRACE_D4 CAN1.RX (Set0) SPIS1.CLK (Set0) TRACE.D4 (Set0)
TRACE_D5 CAN1.TX (Set0) SPIS1.MOSI (Set0) TRACE.D5 (Set0)
TRACE_D6 I2C0.SDA (Set0) SPIS1.SS0 (Set0) TRACE.D6 (Set0)
TRACE_D7 I2C0.SCL (Set0) SPIS1.MISO (Set0) TRACE.D7 (Set0)
SPIM0_CLK UART0.CTS (Set2) (Set1) (Set0) I2C1.SDA (Set1) SPIM0.CLK (Set0)
SPIM0_MOSI UART0.RTS (Set2) (Set1) (Set0) I2C1.SCL (Set1) SPIM0.MOSI (Set0)
SPIM0_MISO UART1.CTS (Set0) CAN1.RX (Set1) SPIM0.MISO (Set0)
SPIM0_SS0 UART1.RTS (Set0) CAN1.TX (Set1) SPIM0.SS0 (Set0)
UART0_RX SPIM0.SS1 (Set0) CAN0.RX (Set0) UART0.RX (Set1)
UART0_TX SPIM1.SS1 (Set0) CAN0.TX (Set0) UART0.TX (Set1)
I2C0_SDA SPIM1.CLK (Set0) UART1.RX (Set0) I2C0.SDA (Set1)
I2C0_SCL SPIM1.MOSI (Set0) UART1.TX (Set0) I2C0.SCL (Set1)
CAN0_RX SPIM1.MISO (Set0) UART0.RX (Set2) CAN0.RX (Set1)
CAN0_TX SPIM1.SS0 (Set0) UART0.TX (Set2) CAN0.TX (Set1)
To enable a HPS pin to work as a Loan IO or as a GPIO pin, Click on the GPIO or Loan IO button on the Peripherals Mux table. The Specific peripherals are

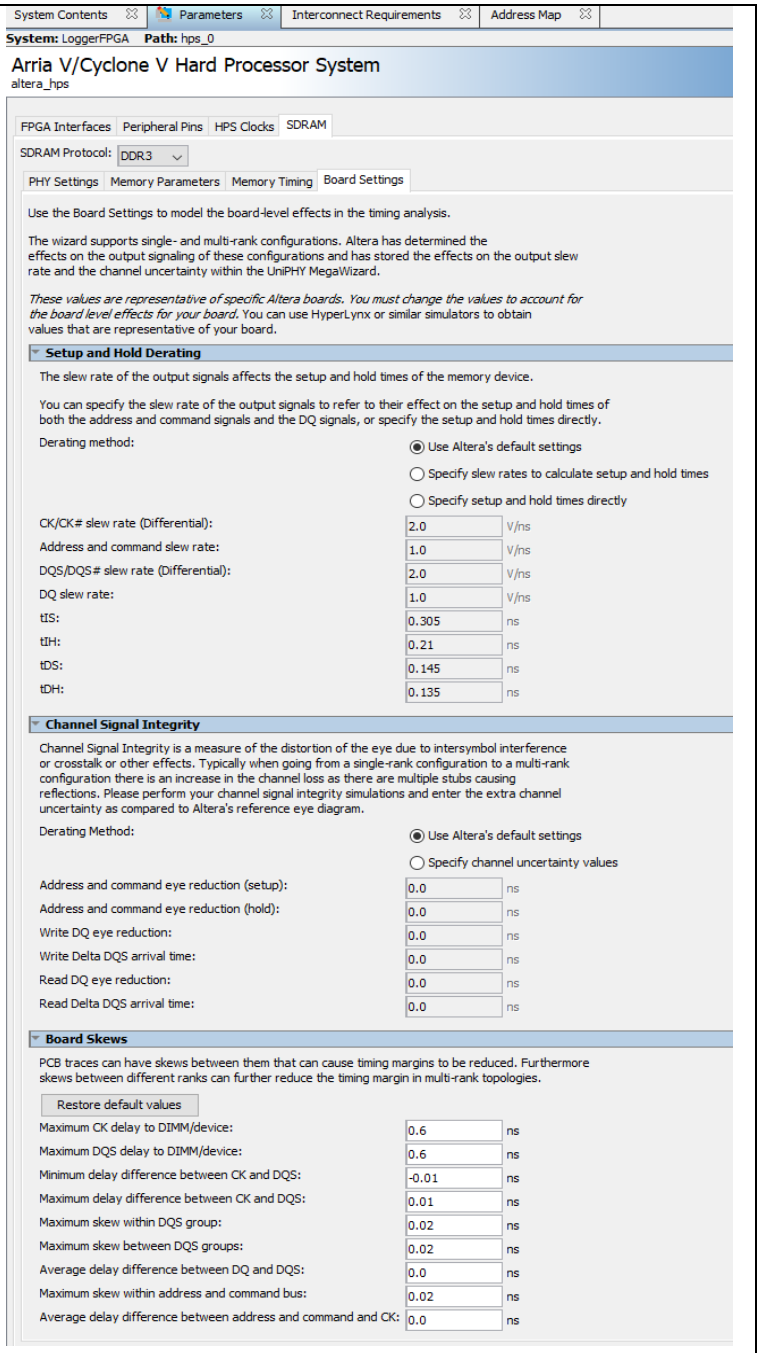

System Contents
Parameters
Interconnect Requirements
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
Input Clocks
Output Clocks
External Clock Sources
EOSC1 clock frequency: 25.0 MHz
EOSC2 clock frequency: 25.0 MHz
FPGA-to-HPS PLL Reference Clocks
Enable FPGA-to-HPS SDRAM PLL reference clock
Enable FPGA-to-HPS peripheral PLL reference clock
FPGA-to-HPS SDRAM PLL reference clock frequency: 0.0 MHz
FPGA-to-HPS peripheral PLL reference clock frequency: 0.0 MHz
Peripheral FPGA Clocks
EMAC0 emac0_md_clk clock frequency: 100.0 MHz
EMAC0 emac0_gtx_clk clock frequency: 100 MHz
EMAC1 emac1_md_clk clock frequency: 2.5 MHz
EMAC1 emac1_gtx_clk clock frequency: 125 MHz
QSPI qspi_sclk_out clock frequency: 100 MHz
SPIM0 spim0_sclk_out clock frequency: 100 MHz
SPIM1 spim1_sclk_out clock frequency: 100 MHz
I2C0 i2c0_clk clock frequency: 100 MHz
I2C1 i2c1_clk clock frequency: 100 MHz
I2C2 i2c2_clk clock frequency: 100 MHz
I2C3 i2c3_clk clock frequency: 100 MHz


System Contents
Parameters
Interconnect Requirements
Address Map
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
Input Clocks
Output Clocks
Clock Sources
Peripheral PLL reference clock source: EOSC1 clock
SDMMC clock source: Peripheral NAND SDMMC clock
NAND clock source: Peripheral NAND SDMMC clock
QSPI clock source: Main QSPI clock
L4 MP clock source: Peripheral base clock
L4 SP clock source: Peripheral base clock
Main PLL Output Clocks - Desired Frequencies
Default MPU clock frequency: 800.0 MHz
Use default MPU clock frequency
MPU clock frequency: 800.0 MHz
L3 MP clock frequency: 200.0 MHz
L3 SP clock frequency: 100.0 MHz
Debug AT clock frequency: 25.0 MHz
Debug clock frequency: 12.5 MHz
Debug trace clock frequency: 25.0 MHz
L4 MP clock frequency: 100.0 MHz
L4 SP clock frequency: 100.0 MHz
Configuration/HPS-to-FPGA user 0 clock frequency: 100.0 MHz
Peripheral PLL Output Clocks - Desired Frequencies
SDMMC clock frequency: 200.0 MHz
NAND clock frequency: 12.5 MHz
QSPI clock frequency: 400.0 MHz
EMAC0 clock frequency: 250.0 MHz
EMAC1 clock frequency: 250.0 MHz
USB clock frequency: 200.0 MHz
SPI clock frequency: 200.0 MHz
CAN0 clock frequency: 100.0 MHz
CAN1 clock frequency: 100.0 MHz
GPIO debounce clock frequency: 32000 Hz
HPS-to-FPGA User Clocks
Enable HPS-to-FPGA user 0 clock
Enable HPS-to-FPGA user 1 clock
Enable HPS-to-FPGA user 2 clock
HPS-to-FPGA user 0 clock frequency: 100.0 MHz
HPS-to-FPGA user 1 clock frequency: 100.0 MHz
HPS-to-FPGA user 2 clock frequency: 120.0 MHz


System Contents
Parameters
Interconnect Requiremer
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol:
DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Clocks
Memory clock frequency:
360.0
MHz
Use specified frequency instead of calculated frequency
Achieved memory clock frequency:
360.0
MHz
PLL reference clock frequency:
25.0
MHz
Advanced PHY Settings
Supply Voltage:
1.35V DDR3L
I/O standard:
SSTL-135


System Contents
Parameters
Interconnect Requireme
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol:
DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Apply timing parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
tIS (base): 170 ps
tIH (base): 120 ps
tDS (base): 10 ps
tDH (base): 45 ps
tDQSQ: 100 ps
tQH: 0.38 cycles
tDQSCK: 225 ps
tDQSS: 0.27 cycles
tQSH: 0.4 cycles
tDSH: 0.18 cycles
tDSS: 0.18 cycles
tINIT: 500 us
tMRD (tMRW): 4 cycles
tRAS: 35.0 ns
tRCD: 13.75 ns
tRP: 13.75 ns
tREFI (tREFIab): 7.8 us
tRFC (tRFCab): 260.0 ns
tWR: 15.0 ns
tWTR: 4 cycles
tFAW: 30.0 ns
tRRD: 10.0 ns
tRTP: 10.0 ns


System Contents
Parameters
Interconnect Requirements
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol: DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Apply memory parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
Memory vendor: JEDEC
Memory format: Discrete Device
Memory device speed grade: 800.0 MHz
Total interface width: 32
Number of DQS groups: 4
Number of chip select/depth expansion: 1
Number of clocks: 1
Row address width: 15
Column address width: 10
Bank-address width: 3
Enable DM pins
DQS# Enable
Memory Initialization Options
Mirror Addressing: 1 per chip select: 0
Address and command parity
Burst Length: Burst chop 4 or 8 (on the fly)
Read Burst Type: Sequential
DLL precharge power down: DLL off
Memory CAS latency setting: 7
Output drive strength setting: RZQ/6
ODT Rtt nominal value: RZQ/6
Auto selfrefresh method: Manual
Selfrefresh temperature: Extended
Memory write CAS latency setting: 6
Dynamic ODT (Rtt_WR) value: Dynamic ODT off


System Contents
Parameters
Interconnect Requirements
Address Map
System: LoggerFPGA Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol: DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Use the Board Settings to model the board-level effects in the timing analysis.
The wizard supports single- and multi-rank configurations. Altera has determined the effects on the output signaling of these configurations and has stored the effects on the output slew rate and the channel uncertainty within the UniPHY MegaWizard.
These values are representative of specific Altera boards. You must change the values to account for the board level effects for your board. You can use HyperLynx or similar simulators to obtain values that are representative of your board.
Setup and Hold Derating
The slew rate of the output signals affects the setup and hold times of the memory device.
You can specify the slew rate of the output signals to refer to their effect on the setup and hold times of both the address and command signals and the DQ signals, or specify the setup and hold times directly.
Derating method:
Use Altera's default settings
Specify slew rates to calculate setup and hold times
Specify setup and hold times directly
CK/CK# slew rate (Differential): 2.0 V/ns
Address and command slew rate: 1.0 V/ns
DQS/DQS# slew rate (Differential): 2.0 V/ns
DQ slew rate: 1.0 V/ns
tIS: 0.305 ns
tIH: 0.21 ns
tDS: 0.145 ns
tDH: 0.135 ns
Channel Signal Integrity
Channel Signal Integrity is a measure of the distortion of the eye due to intersymbol interference or crosstalk or other effects. Typically when going from a single-rank configuration to a multi-rank configuration there is an increase in the channel loss as there are multiple stubs causing reflections. Please perform your channel signal integrity simulations and enter the extra channel uncertainty as compared to Altera's reference eye diagram.
Derating Method:
Use Altera's default settings
Specify channel uncertainty values
Address and command eye reduction (setup): 0.0 ns
Address and command eye reduction (hold): 0.0 ns
Write DQ eye reduction: 0.0 ns
Write Delta DQS arrival time: 0.0 ns
Read DQ eye reduction: 0.0 ns
Read Delta DQS arrival time: 0.0 ns
Board Skews
PCB traces can have skews between them that can cause timing margins to be reduced. Furthermore skews between different ranks can further reduce the timing margin in multi-rank topologies.
Restore default values
Maximum CK delay to DIMM/device: 0.6 ns
Maximum DQS delay to DIMM/device: 0.6 ns
Minimum delay difference between CK and DQS: -0.01 ns
Maximum delay difference between CK and DQS: 0.01 ns
Maximum skew within DQS group: 0.02 ns
Maximum skew between DQS groups: 0.02 ns
Average delay difference between DQ and DQS: 0.0 ns
Maximum skew within address and command bus: 0.02 ns
Average delay difference between address and command and CK: 0.0 ns

Interconnect Requirements

System Contents | Parameters | Interconnect Requirements | Address Map

Configure interconnect requirements for the system or an interface.

System-wide Requirements

Limit interconnect pipeline stages to: 1

Clock crossing adapter type: Handshake

All Requirements

Identifier	Setting	Value
$system	Clock crossing adapter type	Handshake
$system	Limit interconnect pipeline stages to	1
$system	Enable ECC protection	FALSE
$system	Automate default slave insertion	FALSE
mm_interconnect_0|FPGA_Block_0_avalon_sla...	Internal interconnect pipeline count	0
mm_interconnect_0|FPGA_Block_0_avalon_sla...	Internal interconnect pipeline count	0
mm_interconnect_0|cmd_mux_006.src/FPGA_...	Internal interconnect pipeline count	0

Address Map

System Contents | Parameters | Interconnect Requirements | Address Map

System: LoggerFPGA **Path:** hps_0

	FPGA_Block_0.master	FPGA_Block_0.hslog_master	eMMC_0.master	hps_0.h2f_axi_master
CAN_Controller_0.avalon_slave_0				0x0002_0000 - 0x0002_03ff
CAN_Controller_1.avalon_slave_0				0x0002_0400 - 0x0002_07ff
FPGA_Block_0.avalon_slave_0				0x0008_0000 - 0x000b_ffff
MRAM_0.avalon_slave_0				0x0020_0000 - 0x003f_ffff
TickBlock_0.avalon_slave_0				0x0000_0000 - 0x0000_003f
UART_0.avalon_slave_0				0x0003_0000 - 0x0003_003f
UART_1.avalon_slave_0				0x0003_0100 - 0x0003_013f
UART_2.avalon_slave_0				0x0003_0200 - 0x0003_023f
eMMC_0.avalon_slave_0				0x0004_0000 - 0x0004_003f
hps_0.f2h_sdram0_data	0x0000_0000 - 0xffff_ffff			
hps_0.f2h_sdram1_data		0x0000_0000 - 0xffff_ffff		