Laird™
CONNECTIVITY

Datasheet

Sterling™-LWB5

Version 3.5

Revision History

Version	Date	Notes	Contributors	Approver
3.0	10 Dec 2020	Updated to new Laird Connectivity format Updated all regulatory information	Maggie Teng Ryan Urness	Jonathan Kaye
3.1	14 Jan 2021	Moved regulatory information to separate document	Sue White	Jonathan Kaye
3.2	29 Mar 2021	Updated Figure 31	Peter Scharpf	Alex Mohr
3.3	24 May 2022	Updated BT spec to 5.2	Dave Drogowski	Andy Ross
3.4	27 May 2022	Updated Infineon references	Dave Drogowski	Elaine Baxter
3.5	Feb 28 2023	Updated Declaration ID to D057228 in Bluetooth SIG Qualification.	Dave Drogowski	Jonathan Kaye

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CONTENTS

1 Description 4
2 Module Variants....5
3 Functional features....7
4 Ordering Information....8
5 Module accessories....8
6 Block DiagramS....9
7 SIP Module Footprint and Pin Definitions....11
8 SIP Module Pin Descriptions....12
9 U.FL and Chip Antenna Module Footprint and Pin Definitions....15
10 U.FL AND Chip antenna module Pin Descriptions....16
11 Module Power States....18
12 Module PIN I/O States....18
13 Electrical Specifications....20
13.1 Absolute Maximum Ratings....20
13.2 Recommended Operating Conditions....20
13.3 General Characteristics....20
13.4 WLAN Power Consumption....20
13.5 Bluetooth Power Consumption....21
13.6 Power Supply Requirements....22
13.7 Power Supply Sequencing....23
14 Crystal Oscillator Requirements....26
14.1 WLAN RF Characteristics....27
14.2 Bluetooth RF Characteristics....34
15 WLAN Host Interface....34
15.1 SDIO Interface....34
16 Bluetooth UART Host Interface....36
16.1 Overview....36
16.2 Soldering Recommendations....37
16.3 Recommended Reflow Profile for Lead Free Solder....38
17 Cleaning....38
18 Optical Inspection....38
19 Rework....38
20 Shipping, Handling, and Storage....39
21 Regulatory....40
22 Bluetooth SIG Qualification....40
23 Chip Antenna Performance....42
24 Base SIP Module Mechanical Data....48
25 Base SIP Module PCB Footprint....49
26 Base SIP Module tAPE AND REEL Packaging....50
27 U.fl and Chip Antenna Mechanical Data....51
28 u.fl and Chip Antenna PCB Footprint....52
29 u.fl and Chip antenna Tape and Reel Packaging....53
30 Device Markings....54
31 Additional Information....54

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1 DESCRIPTION

The Sterling-LWB5 is a high performance 2.4 GHz and 5 GHz WLAN and Bluetooth LE combo module based on latest-generation silicon (Infineon's CYW43353). With an industrial temperature rating, broad country certifications, and the availability of two different package styles, the Sterling-LWB5 provides significant flexibility to meet various end user application needs.

The on-module chip antenna package style for the Sterling-LWB5 eliminates complexity for design integration, simplifies manufacturing assembly with larger pin outs, and features an advanced chip antenna that offers greater resistance to de-tuning than typical trace or chip antennas.

The module includes the MAC, Baseband and Radio to support WLAN applications and an independent, high-speed UART is provided for the Bluetooth host interface. In addition, the latest Linux and Android drivers are supported directly by Laird Connectivity and Infineon.

Need to get to market quickly? Not an expert in 802.11. Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? Laird Connectivity's Design Services will be happy to develop custom hardware or software, or assist with integrating the design. Contact us at sales@lairdconnect.com or call us at 262-375-4400.

Features

- IEEE 802.11 a/b/g/n/ac (single stream n)
- Typical WLAN Transmit Power:
  - +16 dBm, 11 Mbps, CCK (b)
  - +13 dBm, 54 Mbps, OFDM (g)
  - +11 dBm, HT20 MCS7 (n)
- Typical WLAN Sensitivity:
  - -87 dBm, 8% PER,11 Mbps (b)
  - -73 dBm, 10% PER, 54 Mbps (g)
  - -71 dBm, 10% PER, MCS7 (n)
- Bluetooth 2.1+EDR, Bluetooth 3.0, Bluetooth 5.2 (Bluetooth Low Energy)
- WLAN and Bluetooth coexistence
- Available in two footprint styles:
  - Easy to Integrate: 15.5 mm x 21 mm
  - Miniature footprint: 10 mm x 10 mm
- Available with integrated chip antenna or U.FL connector for external antenna
- Operating voltage: VBAT = 3.20V to 3.60V
- VDDIO = 1.71V to 1.89V
- Operating temperature: -40 to +85° C
- Compact design based on Infineon's CYW43353 SoC
- Worldwide acceptance: FCC (USA), ISED (Canada), EU, MIC (Japan) and AS/NZS
- BT SIG QDID: 97564
- REACH and RoHS compliant

Applications

- Security & Building Automation
- Internet of Things / M2M Connectivity
- Smart Gateways

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2 Module Variants

The Laird Connectivity Sterling-LWB5 Module is available in three different versions. Depending on the user's antenna and footprint needs, there is a variant to suite most application requirements. We recommend that for simplicity of both the host PCB design, as well as the manufacturing process, that either the Chip Antenna or RF Connector version of the modules be used in your design.

2.1 450-0162 - Base SIP Module

This module variant is supplied in a compact, 84 pin, LGA footprint. Unlike the other module variants, it requires the addition of either an off-module antenna or RF connector, as well as the associated matching components. In order to benefit from the EMC certifications on the module, strictly following the layout in the module application guide is required. This requires adherence to the PCB stack-up and layout around the antenna. The footprint of this module may require additional care during reflow and PCB assembly.

Figure 1: Sterling-LWB5 Base SIP Module (450-0162)

2.2 450-0168 – U.FL Module

This module variant integrates the 450-0162 Base SIP Module, a U.FL RF connector, and all associated RF matching components on a PCB. This integrated approach not only provides a U.FL connector for connections to external antennas, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.

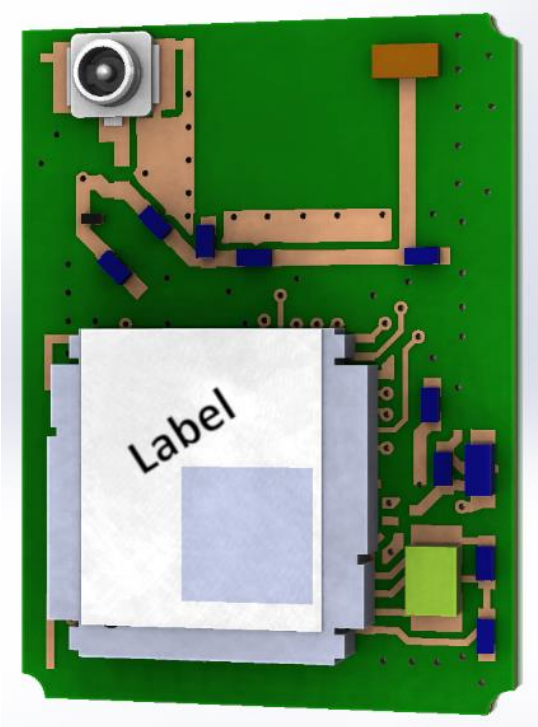

Figure 2: Sterling-LWB5 U.FL Module (450-0168)

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2.3 450-0169 - Chip Antenna Module

This module variant integrates the 450-0162 Base SIP Module, a chip antenna, and all associated RF matching components on a PCB. This integrated approach not only provides an external antenna solution, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.

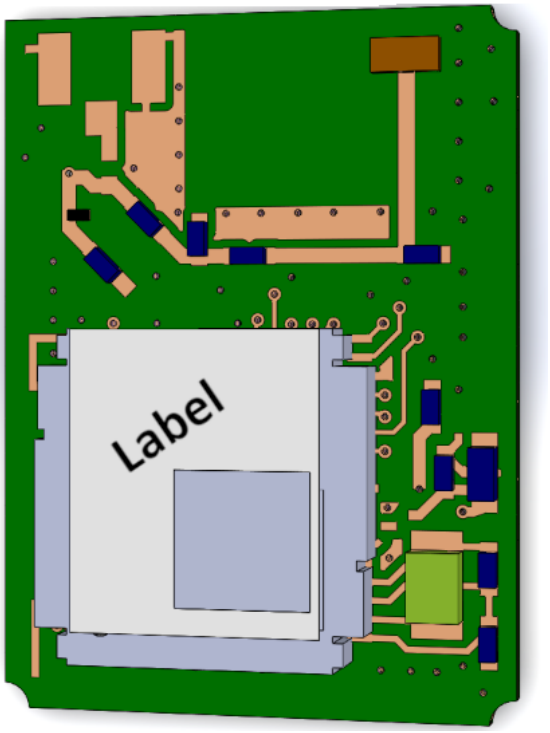

Figure 3: Sterling-LWB5 Chip Antenna Module (450-0169)

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3 FUNCTIONAL FEATURES

3.1 WLAN Features

- IEEE 802.11 a/b/g/n/ac 1x1 2.4 GHz Radio
  - Internal Power Amplifier (PA)
  - Internal Low Noise Amplifier(LNA)
  - Internal T/R Switch
  - Simultaneous BT/WLAN reception with a single antenna.
- Media Access Controller (MAC)
- Physical Layer (PHY)
- Baseband Processor
- **Standards**
  - IEEE 802.11a, 802.11b, 802.11g, 802.11n (single stream), 802.11ac

3.2 Bluetooth Features

- Class 2 power amplifier with Class 2 capability
- HCI Interface using High Speed UART
- PCM for Audio Data
- **Standards**
  - Bluetooth 2.1+EDR, Bluetooth 3.0, Bluetooth 5.2 (Bluetooth Low Energy)

3.3 Wireless Security System Features

- Supported modes:
  - Open (no security)
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)

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4 Ordering Information

Table 1: Sterling-LWB5 Part Numbers

Order Number	Description
450-0168C	Sterling-LWB5 U.FL Module (Cut Tape)
450-0168R	Sterling-LWB5 U.FL Module (Tape and Reel, SPQ = 1000)
450-0169C	Sterling-LWB5 Chip Antenna Module (Cut Tape)
450-0169R	Sterling-LWB5 Chip Antenna Module (Tape and Reel, SPQ = 1000)
450-0162C	Sterling-LWB5 Base SIP Module (Cut Tape)
450-0162R	Sterling-LWB5 Base SIP Module (Tape and Reel, SPQ = 1000)
450-0171	Sterling-LWB5 SD Development Board, U.FL
450-0172	Sterling-LWB5 SD Development Board, Chip Antenna

5 Module Accessories

	Order Number	Description
	001-0009	2.4 GHz and 5.5 GHz Dipole Antenna with Reverse Polarity SMA Connector
	080-0001	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm
	001-0016	2.4 GHz and 5.5GHz FlexPIFA Antenna
	Johanson 2450AD14A5500T	2.4/5.5 GHz Chip Antenna

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6 BLOCK DIAGRAMS

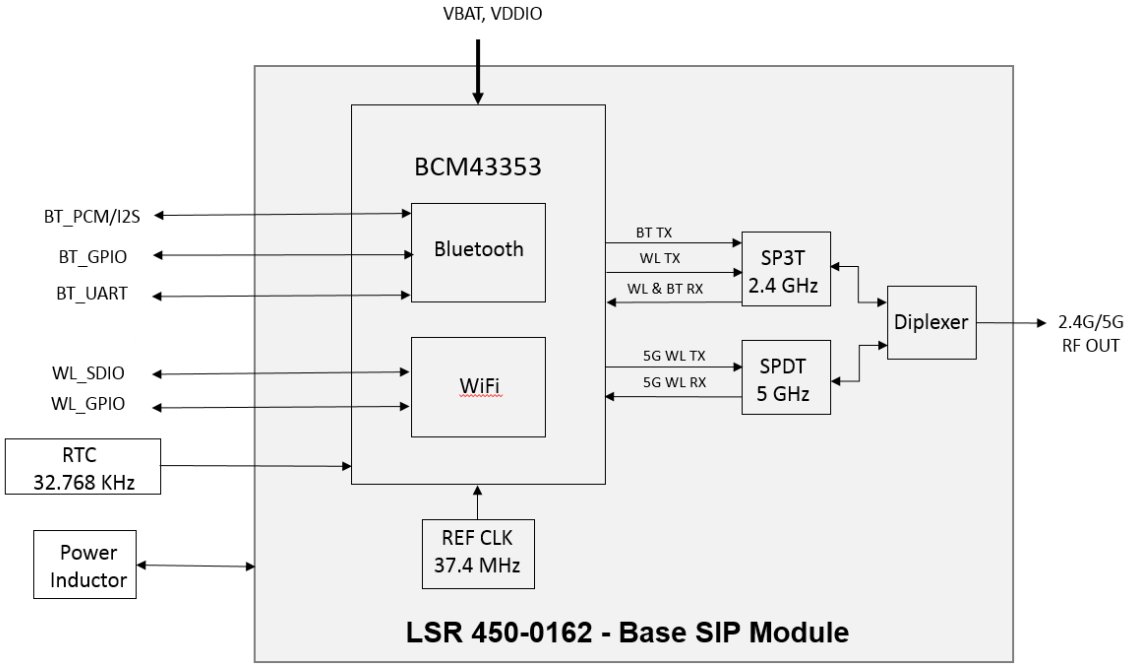

Figure 4: Sterling-LWB5 Base SIP Module Block Diagram

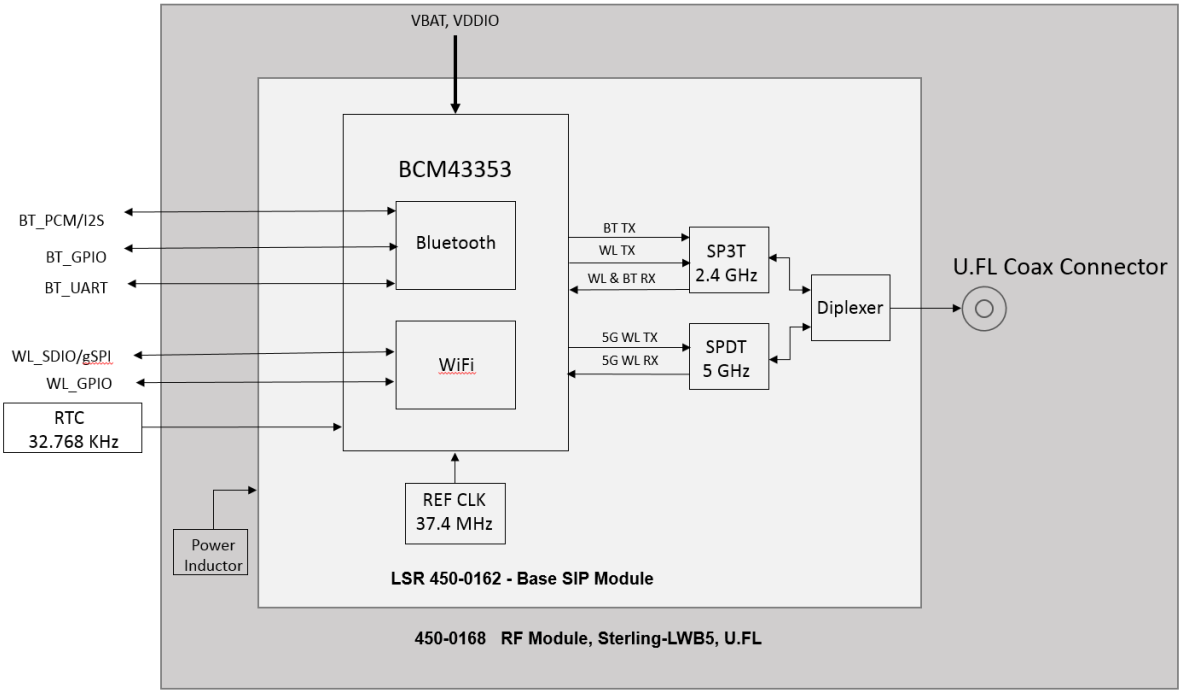

Figure 5: Sterling-LWB5 U.FL Module Block Diagram

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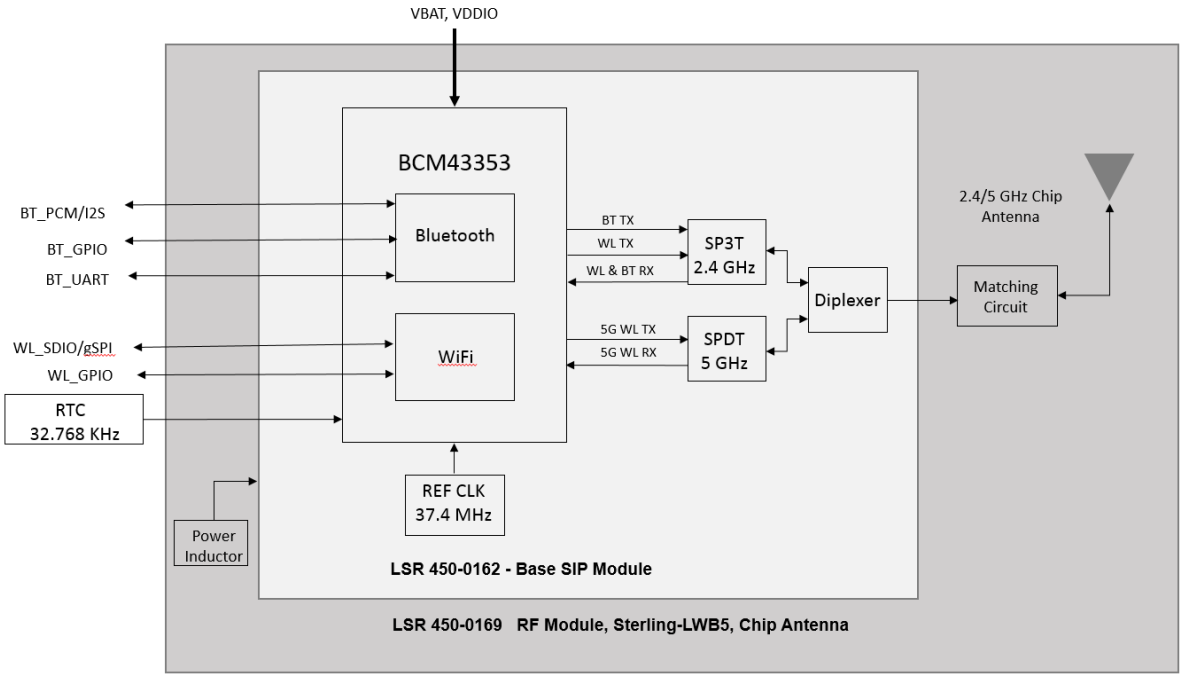

Figure 6: Sterling-LWB5 Chip Antenna Module Block Diagram

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7 SIP Module Footprint and Pin Definitions

Note that the following footprint and pin definition applies to the Sterling-LWB5 Base SIP Module (450-0162). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.

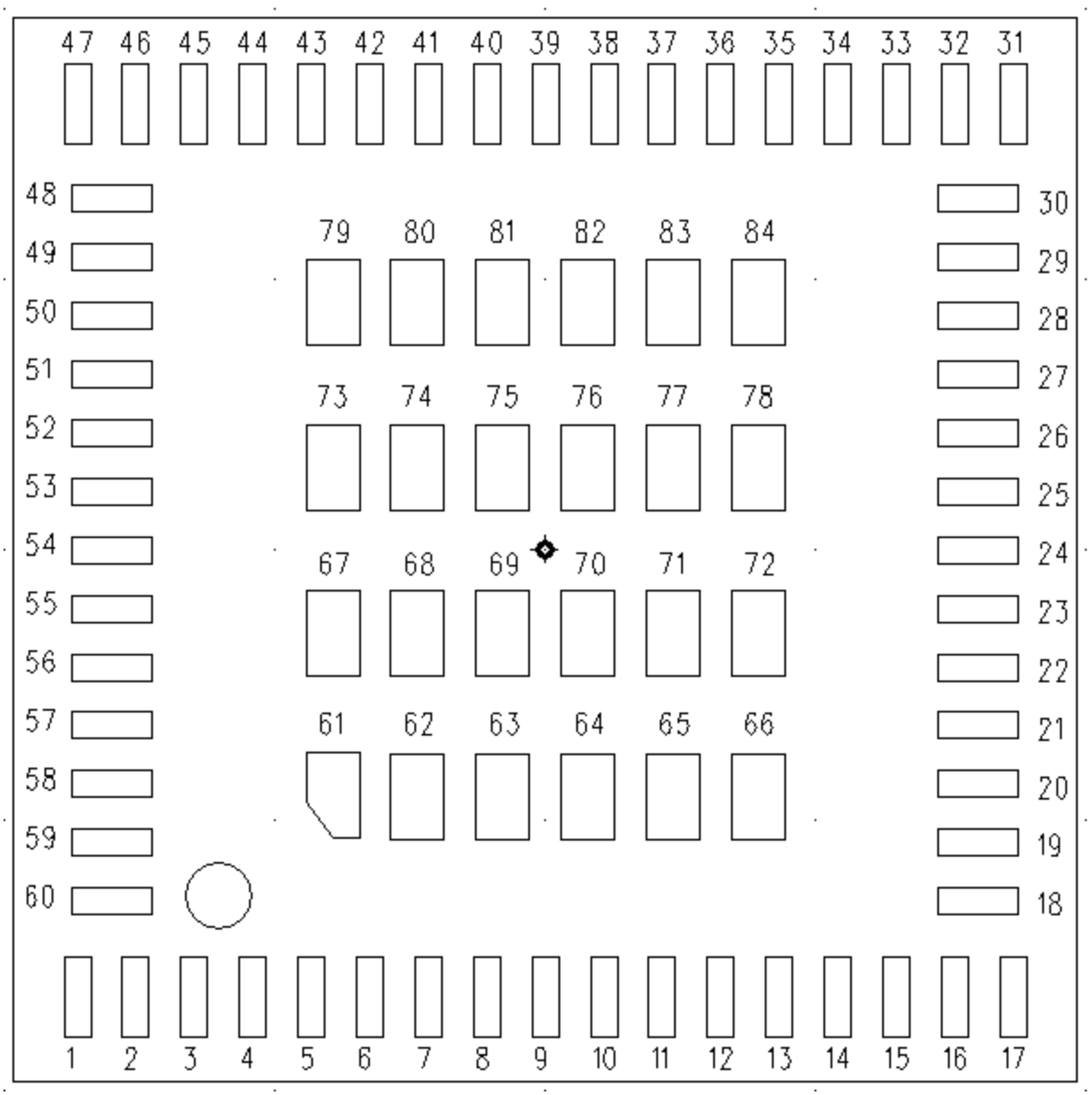

Figure 7: Sterling-LWB5 SIP Module Pinout (Top View)

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8 SIP Module Pin Descriptions

Module Pin	Name	I/O Type	Description
1	GND	-	GROUND
2	GND	-	GROUND
3	GND	-	GROUND
4	GND	-	GROUND
5	GND	-	GROUND
6	RF_SW_CTRL_9	O	External RF SW control
7	RF_SW_CTRL_8	O	External RF SW control
8	GND	-	GROUND
9	GND	-	GROUND
10	GND	-	GROUND
11	GND	-	GROUND
12	GND	-	GROUND
13	GPIO_3	I/O	LTE Coexistence GPIO for 3-wire
14	GPIO_5	I/O	LTE Coexistence GPIO
15	GPIO_4	I/O	LTE Coexistence GPIO
16	GND	-	GROUND
17	WLAN_HOST_WAKE/GPIO_0	O	Output from WLAN to wake module
18	GND	GND	GROUND
19	SDIO_CLK	I	WLAN SDIO clock
20	GND	-	GROUND
21	SDIO_CMD	I	WLAN SDIO command line
22	SDIO_DATA_0	I/O	WLAN SDIO data line 0
23	SDIO_DATA_1	I/O	WLAN SDIO data line 1
24	SDIO_DATA_2	I/O	WLAN SDIO data line 2
25	SDIO_DATA_3	I/O	WLAN SDIO data line 3
26	GND	-	GROUND
27	LPO IN	I	32.768KHz Input
28	WL_REG_ON	I	PMU power up to the WLAN section
29	BT_REG_ON	I	PMU power up to the Bluetooth section
30	GND	-	GROUND
31	GND	-	GROUND
32	SR_VLX	O	CBUCK switching regulator output
33	GND	-	GROUND
34	VIN_LDO	I	CBUCK switching regulator input
35	GND	-	GROUND
36	VBAT	I	Power VBAT

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Module Pin	Name	I/O Type	Description
37	VBAT	I	Power VBAT
38	GND	-	GROUND
39	VDDIO	I	I/O Power Supply
40	GND	-	GROUND
41	BT_PCM_IN	I	Bluetooth PCM data input
42	BT_PCM_CLK	I/O	Bluetooth PCM clock
43	BT PCM SYNC	I/O	Bluetooth PCM Sync signal
44	BT_PCM_OUT	O	Bluetooth PCM data output
45	GND	-	GROUND
46	BT_HOST_WAKE	O	Output from Bluetooth to wake Host
47	BT_DEV_WAKE	I	Input from Host to wake Bluetooth
48	GND	-	GROUND
49	BT_UART_CTS	I	Bluetooth UART clear to send
50	BT_UART_RTS	O	Bluetooth UART request to send
51	BT_UART_RXD	I	Bluetooth UART serial Input
52	BT_UART_TXD	O	Bluetooth UART serial output
53	GND	-	GROUND
54	GND	-	GROUND
55	GND	-	GROUND
56	GND	-	GROUND
57	GND	-	GROUND
58	GND	-	GROUND
59	5G/2G_ANT	I/O	2.4G/5GHz RF signal input/output
60	GND	-	GROUND
61	GND	-	GROUND
62	GND	-	GROUND
63	GND	-	GROUND
64	GND	-	GROUND
65	GND	-	GROUND
66	GND	-	GROUND
67	GND	-	GROUND
68	GND	-	GROUND
69	GND	-	GROUND
70	GND	-	GROUND
71	GND	-	GROUND
72	GND	-	GROUND
73	GND	-	GROUND

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Module Pin	Name	I/O Type	Description
74	GND	-	GROUND
75	GND	-	GROUND
76	GND	-	GROUND
77	GND	-	GROUND
78	GND	-	GROUND
79	GND	-	GROUND
80	GND	-	GROUND
81	GND	-	GROUND
82	GND	-	GROUND
83	GND	-	GROUND
84	GND	-	GROUND

PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port,

RF = Bi-directional RF Port, GND = Ground

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9 U.FL and Chip Antenna Module Footprint and Pin Definitions

Note that the following footprint and pin definitions apply to the Sterling-LWB5 U.FL and Chip Antenna variants of the module (450-0168 and 450-0169). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.

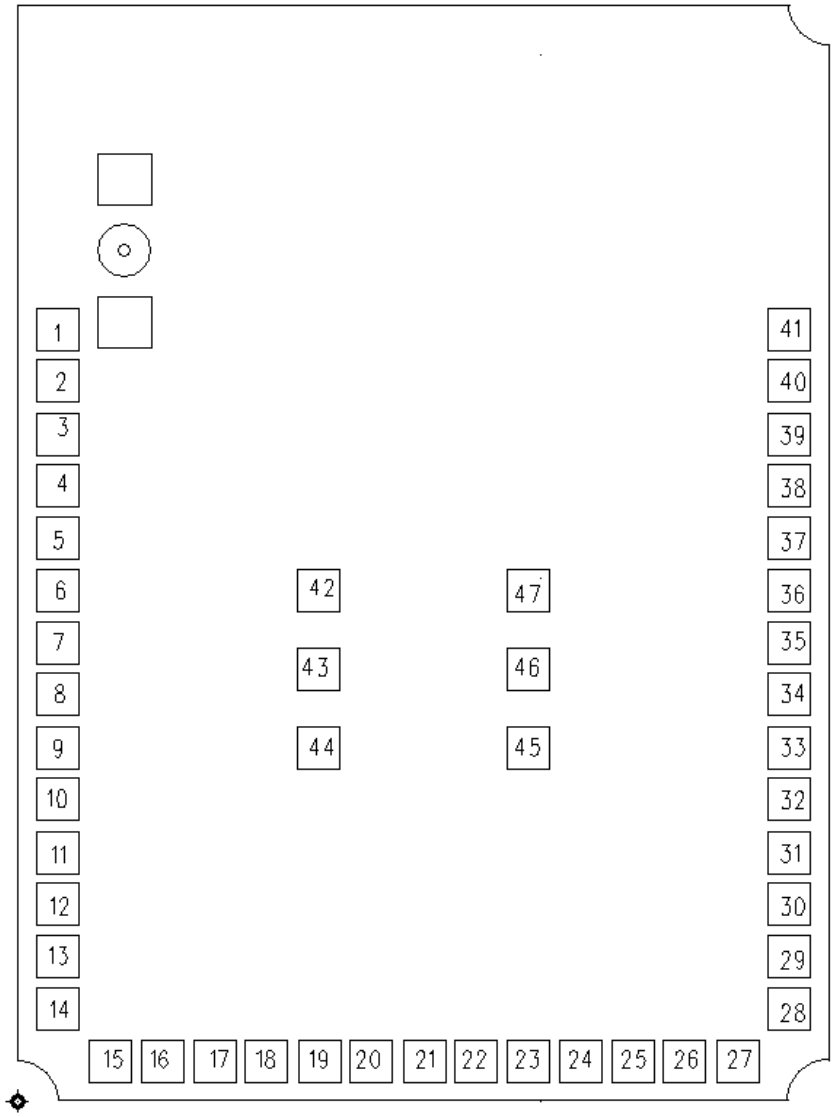

Figure 8: Sterling-LWB5 U.FL and Chip Antenna Module Pinout (Top View)

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10 U.FL AND CHIP ANTENNA MODULE PIN DESCRIPTIONS

Table 2: Sterling-LWB5 U.FL and Chip Antenna Module Pin Descriptions

Module Pin	Name	I/O Type	Description
1	GND	GND	GROUND
2	BT_PCM_SYNC	DIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
3	BT_PCM_IN	DI	PCM DATA INPUT SENSING
4	BT_PCM_OUT	DO	PCM DATA OUTPUT
5	VBAT	PI	WIFI AND BLUETOOTH POWER SUPPLY
6	GND	GND	GROUND
7	RF_SW_CTRL_9	DO	External RF SW control
8	RF_SW_CTRL_8	DO	External RF SW control
9	GPIO_3	DIO	PROGRAMMABLE GPIO PIN
10	GPIO_5	DIO	PROGRAMMABLE GPIO PIN
11	GPIO_4	DIO	PROGRAMMABLE GPIO PIN.
12	WLREG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE WLAN SECTION.
13	GPIO_0/ WLAN_HOST_WAKE	DO	PROGRAMMABLE GPIO PIN.
14	GND	GND	GROUND
15	NC	NC	NO CONNECT
16	NC	NC	NO CONNECT
17	NC	NC	NO CONNECT
18	GND	GND	GROUND
19	LPO_IN	DI	EXTERNAL SLEEP CLOCK INPUT
20	VDDIO	PI	DC SUPPLY FOR I/O
21	BT_REG_ON	DI	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE BLUETOOTH SECTION.
22	SDIO_DATA_0	DIO	SDIO DATA LINE 0
23	SDIO_DATA_1	DIO	SDIO DATA LINE 1
24	GND	GND	GROUND
25	SDIO_DATA_2	DIO	SDIO DATA LINE 2
26	SDIO_CMD	DIO	SDIO COMMAND LINE
27	SDIO_DATA_3	DIO	SDIO DATA LINE 3
28	GND	GND	GROUND
29	SDIO_CLK	DIO	SDIO CLOCK LINE
30	GND	GND	GROUND
31	BT_UART_RTS	DO	Bluetooth UART request-to-send

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Module Pin	Name	I/O Type	Description
32	BT_UART_CTS	DI	Bluetooth UART clear-to-send
33	BT_UART_TXD	DO	Bluetooth UART transmit output
34	BT_UART_RXD	DI	Bluetooth UART Receive input
35	NC	NC	NO CONNECT
36	NC	NC	NO CONNECT
37	NC	NC	NO CONNECT
38	BT_PCM_CLK	DIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
39	BT_DEV_WAKE	DI	Input from Host to wake Bluetooth
40	BT_HOST_WAKE	DO	Output from Bluetooth to wake Host
41	GND	GND	GROUND
42	GND	GND	GROUND
43	GND	GND	GROUND
44	GND	GND	GROUND
45	GND	GND	GROUND
46	GND	GND	GROUND
47	GND	GND	GROUND

PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

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11 Module Power States

The Sterling-LWB5 WLAN power states are described as follows:

- **Active mode** - All WLAN blocks in the Sterling-LWB5 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Doze mode** - The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW43353 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- **Deep-sleep mode** - Most of the chip, including both analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
- **Power-down mode** - The CYW43353 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

12 Module PIN I/O States

Table 3: I/O States

Pin #		Name	Keeper (b)	Active Mode	Low Power State/Sleep (All Power Present)	Power Down(c) WL_REG_ON =0 BT_REG_ON = 0	Out of Reset: (VDD_VIO is present)		
450-0162 (SiP)	450-0168 & 450-0169 (Modules)						WL_REG_ON =1 BT_REG_ON = 1 (before SW download)	WL_REG_ON =1 BT_REG_ON = 0	WL_REG_ON =0 BT_REG_ON = 1
43	2	BT_PCM_SYNC	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	Output	Input; PD	TBD
41	3	BT_PCM_IN	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	Input, No Pull, High-Z	Input; PD	TBD
44	4	BT_PCM_OUT	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull(d)	Output	Input; PD	TBD
13	9	WIFI_GPIO_3	Y	Input/Output: PU, PD, NoPull (Programmable) Default PD	Input/Output: PU, PD, NoPull (Programmable) Default PD	High –Z No Pull(f)	Input; PD	Input; PD	TBD
14	10	WIFI_GPIO_5	Y	Input/Output: PU, PD, NoPull (Programmable) Default PD	Input/Output: PU, PD, NoPull (Programmable) Default PD	High –Z No Pull(f)	Input; PD	Input; PD	TBD
15	11	WIFI_GPIO_4	Y	Input/Output: PU, PD, NoPull (Programmable) Default NoPull	Input/Output: PU, PD, NoPull (Programmable) Default NoPull	High –Z No Pull(f)	Input, NoPull	Input, NoPull	TBD
28	12	WLREG_ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	TBD
17	13	WIFI_GPIO_0/ WLAN_HOST_WAKE	Y	Input/Output: PU, PD, NoPull (Programmable) Default PD	Input/Output: PU, PD, NoPull (Programmable) Default PD	High –Z No Pull(f)	Input; PD	Input; PD	TBD
29	21	BT_REG_ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	TBD
22	22	SDIO_D0	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
23	23	SDIO_D1	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD

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Pin #		Name	Keeper (b)	Active Mode	Low Power State/Sleep (All Power Present)	Power Down(c) WL_REG_ON =0 BT_REG_ON = 0	Out of Reset: (VDD_VIO is present)		
450-0162 (SiP)	450-0168 & 450-0169 (Modules)						WL_REG_ON =1 BT_REG_ON = 1 (before SW download)	WL_REG_ON =1 BT_REG_ON = 0	WL_REG_ON =0 BT_REG_ON = 1
24	25	SDIO_D2	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
21	26	SDIO_CMD	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
25	27	SDIO_D3	N	SDIO MODE -> PullUp	SDIO MODE -> Input PullUp	High-Z, NoPull	SDIO MODE ->Input PullUP	SDIO MODE -> Input PullUP	TBD
19	29	SDIO_CK	N	Input: NoPull	Input: NoPull	High-Z, NoPull	Input, NoPull	Input, NoPull	TBD
50	31	BT_UART_RTS	Y	Output:NoPull	Output:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
49	32	BT_UART_CTS	Y	Input:NoPull	Input:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
52	33	BT_UART_TXD	Y	Output:NoPull	Output:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
51	34	BT_UART_RXD	Y	Input:PU	Input:NoPull	High-Z,NoPull	Input; PU	Input; PU	TBD
42	38	BT_PCM_CLK	Y	Input No Pull(d)	Input No Pull(d)	High –Z NoPull	Output	Input; PD	TBD
47	39	BT_DEV_WAKE	Y	I/O: PU,PD,NoPull (Programmable)	Input: PU,PD,NoPull (Programmable)	High-Z,NoPull	Input; PD	Input; PD	TBD
46	40	BT_HOST_WAKE	Y	I/O: PU,PD,NoPull (Programmable)	I/O: PU,PD,NoPull (Programmable)	High-Z, NoPull	Input; PU	Input; PD	TBD

The following notations are used: I = Input signal, O = Output signal, I/O = Input/Output signal, PU = Pulled Up, PD = Pulled Down, NoPull = Neither pulled up nor pulled down

Notes:
a. PU = Pulled Up, PD = Pulled Down.
b. N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad, for example, SDIO_CLK.
c. In the Power-down state (xx_REG_ON = 0): High-Z; NoPull => Pad is disabled because power is not supplied.
d. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.
e. Depending on whether the I2S interface is enabled and configuration is master or slave mode, it can be either an input or output.
f. The GPIO pull states for the active and low-power states are hardware defaults. They can all be subsequently programmed as a pull-up or pull-down.

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13 ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	Min	Max	Unit
Wi-Fi power supply (VBAT)	3.2	3.6	V
DIO Power Supply (VDDIO)	1.71	1.89	V
Voltage on digital pins	-0.5	1.89	V
Operating temperature	-40	+85	ºC
Storage temperature	-40	+85	ºC

13.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Typical	Unit
VBAT	3.3	V
VDDIO	1.8	V
Voltage on digital pins	1.8	V
Ambient temperature range	25	ºC

13.3 General Characteristics

13.3.1 DC Characteristics – General Purpose I/O

Table 6: DC Characteristics General Purpose I/O

Parameter	Test Conditions	Min	Typical	Max	Unit
`	VDDIO = 1.8V	-	-	0.35x VDD_VIO	V
Logic input high, V_{IH}	VDDIO = 1.8V	0.65x VDD_VIO	-	-	V
Logic output low, V_{OL}	VDDIO = 1.8V, 2mA	-	-	0.45	V
Logic output high, V_{OH}	VDDIO = 1.8V, 2mA	VDDIO-0.45	-	-	V

13.3.2 RF Characteristics

Table 7: 2.4 GHz RF Characteristics

Parameter	Min	Typical	Max	Unit
2.4 GHz RF frequency range	2400		2472	MHz
5 GHz RF frequency range	5180		5835	MHz
WLAN RF data rate	1	802.11ac and 802.11a/b/g/n	433.3	Mbps
BT RF frequency Range	2402		2480	MHz
BT data rate		Bluetooth 4.2 + EDR		

13.4 WLAN Power Consumption

13.4.1 - 2.4 GHZ

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

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Table 8: 2.4GHz WLAN Power Consumption

Parameter	Test Conditions	Min	Typical	Max	Unit
Sleep (idle, unassociated)		-	5	-	uA
11b TX Current	11 Mbps, 20 MHz	-	320	-	mA
11g TX Current	6 Mbps, 20 MHz	-	260	-	mA
11g TX Current	54 Mbps, 20 MHz	-	230	-	mA
11n TX Current	MCS0, 20 MHz	-	235	-	mA
11n TX Current	MCS7, 20 MHz	-	205	-	mA
11n TX Current	MCS7, 40 MHz	-	185	-	mA
11b RX Current	11 Mbps, 20 MHz	-	55	-	mA
11g RX Current	54 Mbps, 20 MHz	-	55	-	mA
11n RX Current	MCS7, 20 MHz	-	55	-	mA
11n RX Current	MCS7, 40 MHz	-	70	-	mA
Power Down (OFF) Mode		-	5	-	uA

13.4.2 - 5 GHZ

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 9: 5GHz WLAN Power Consumption

Parameter	Test Conditions	Min	Typical	Max	Unit
Sleep (idle, unassociated)		-	5	-	uA
11a TX Current	54 Mbps, 20 MHz	-	275	-	mA
11n TX Current	MCS7, 20 MHz	-	250	-	mA
11n TX Current	MCS7, 40 MHz	-	215	-	mA
11ac TX Current	MCS9, 40 MHz	-	210	-	mA
11ac TX Current	MCS9, 80 MHz	-	215	-	mA
11a RX Current	54 Mbps, 20 MHz	-	70	-	mA
11n RX Current	MCS7, 20 MHz	-	70	-	mA
11n RX Current	MCS7, 40 MHz	-	85	-	mA
11ac RX Current	MCS9, 40 MHz	-	85	-	mA
11ac RX Current	MCS9, 80 MHz	-	110	-	mA
Power Down Mode		-	5	-	uA

13.5 Bluetooth Power Consumption

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 10: Bluetooth Power Consumption

Parameter	Test Conditions	Min	Typical	Max	Unit
Sleep		-	5	-	uA
DM5/DH5 TX	1 Mbps	-	46	-	mA
3DM5/3DH5 TX	3 Mbps	-	44	-	mA

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DM5/DH5 RX	1 Mbps	-	23	-	mA
3DM5/3DH5 RX	3 Mbps	-	23	-	mA
Power Down Mode		-	5	-	uA
BLE TX		-	34	-	mA
BLE RX		-	22	-	mA

13.6 Power Supply Requirements

Table 11: Power Supply Requirements

Power Supply Requirements	Min	Typical	Max	Unit
VDDIO	1.71	1.8	1.89	V
VDDIO Current	-	<1	-	mA
VBAT	3.2	3.3	3.6	V
VBAT Current	-	-	350	mA

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13.7 Power Supply Sequencing

13.7.1 WLAN Boot-Up Sequence

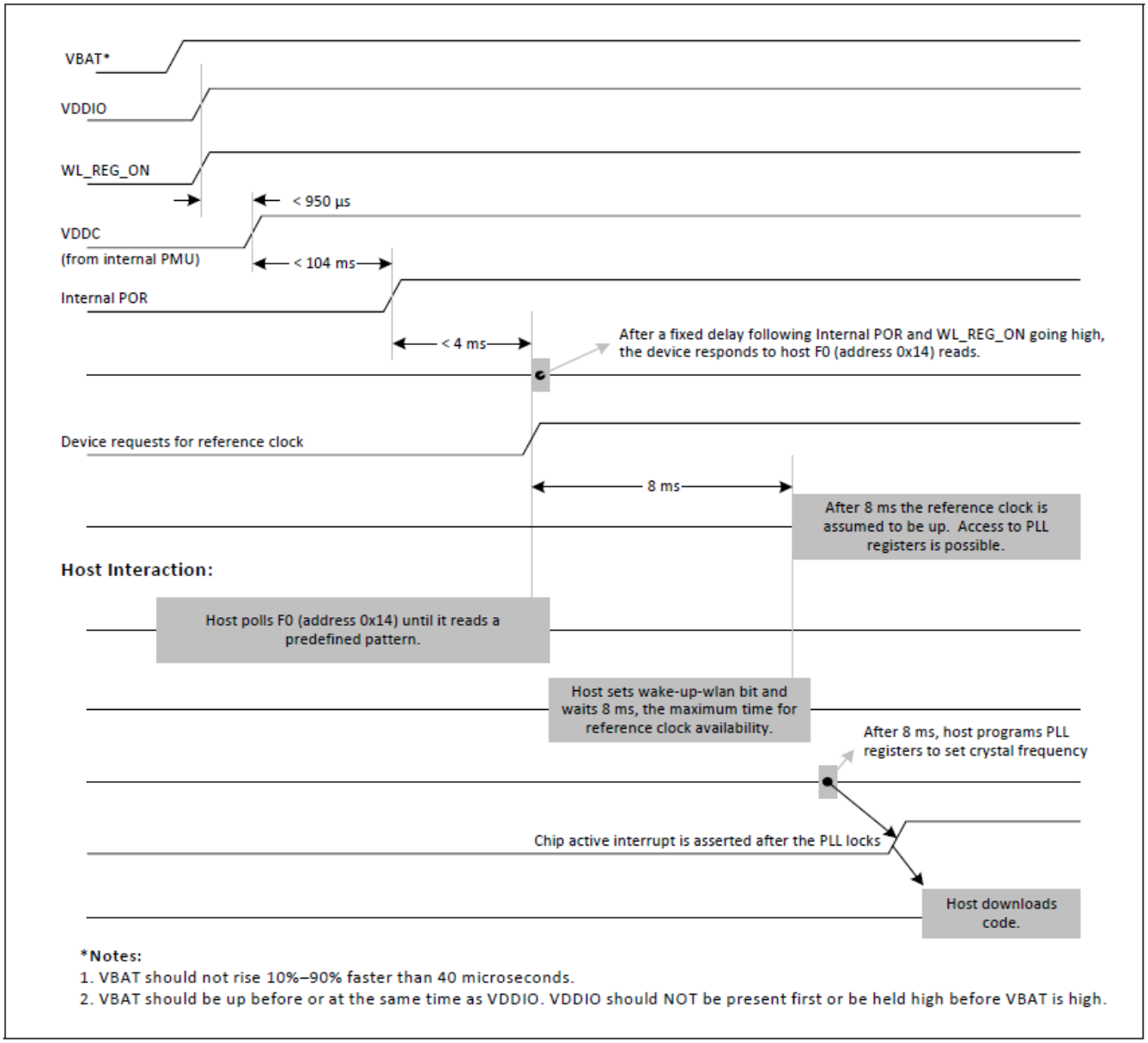

Figure 9: WLAN Boot-Up Sequence

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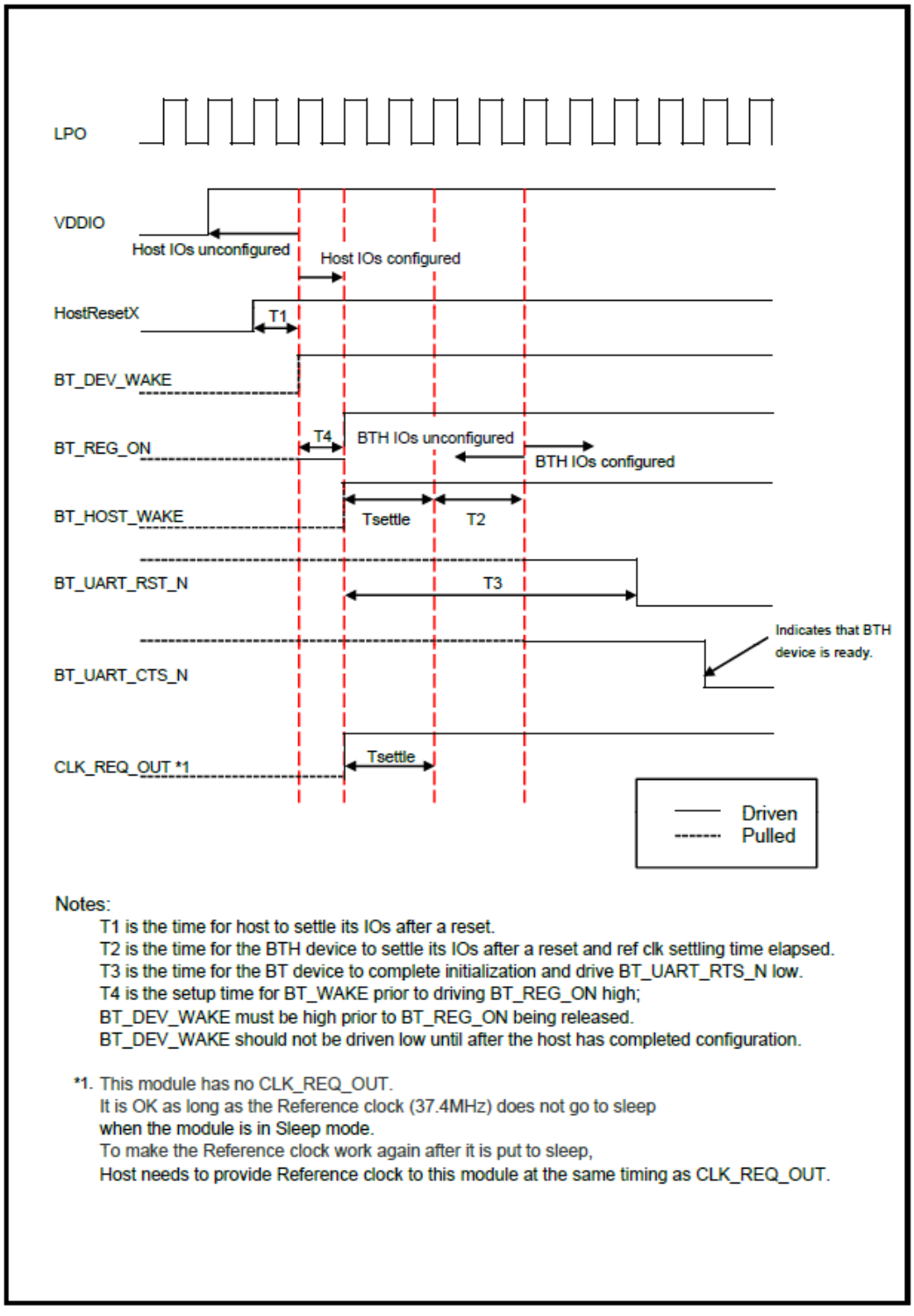

Notes:

T1 is the time for host to settle its IOs after a reset.
T2 is the time for the BTH device to settle its IOs after a reset and ref clk settling time elapsed.
T3 is the time for the BT device to complete initialization and drive BT_UART_RTS_N low.
T4 is the setup time for BT_WAKE prior to driving BT_REG_ON high;
BT_DEV_WAKE must be high prior to BT_REG_ON being released.
BT_DEV_WAKE should not be driven low until after the host has completed configuration.

*1. This module has no CLK_REQ_OUT.
It is OK as long as the Reference clock (37.4MHz) does not go to sleep
when the module is in Sleep mode.
To make the Reference clock work again after it is put to sleep,
Host needs to provide Reference clock to this module at the same timing as CLK_REQ_OUT.

Figure 10: Bluetooth Boot-UP Sequence

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13.7.2 Control Signal Sequencing

The Sterling-LWB5 has two signals that allow host to control power consumption by enabling or disabling the WLAN, Bluetooth and internal regulator blocs. The timing values indicated are minimum required values; longer delays are also acceptable.

- **WL_REG_ON**: Used by the Power Management Unit (PMU) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal DWM-W097 regulators. When this pin is high, the regulators are enabled, and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both WL_REG_ON and BT_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the Power Management Unit (PMU) (OR-gated with WL_REG_ON) to power up the internal DWM-W097 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low the Bluetooth section is in reset.

Note: For both pins, there should be at least a 10ms time delay between consecutive toggles (when both signals have been driven low). This is to allow timer for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36mA during next PMU cold start. The Sterling-LWB5 has an internal power on reset (POR) circuit. The device will be held in reset for a maximum of 110ms after VBAT and VDDIO have both passed the POR threshold. Wait at least 150ms after VBAT and VDDIO are available before initiating SDIO access.

13.7.3 Calibration Current Profile

Although the Max continuous supply current to the module is <320 mA, when providing power to the module, a power source capable of supplying 750 mA peak current for a duration of ~20 msec is required by the module transmitter during calibration.

Figure 11 shows the current profile of the Sterling-LWB5 module during calibration. If current is limited to <750mA during this process, the module will fail to calibrate.

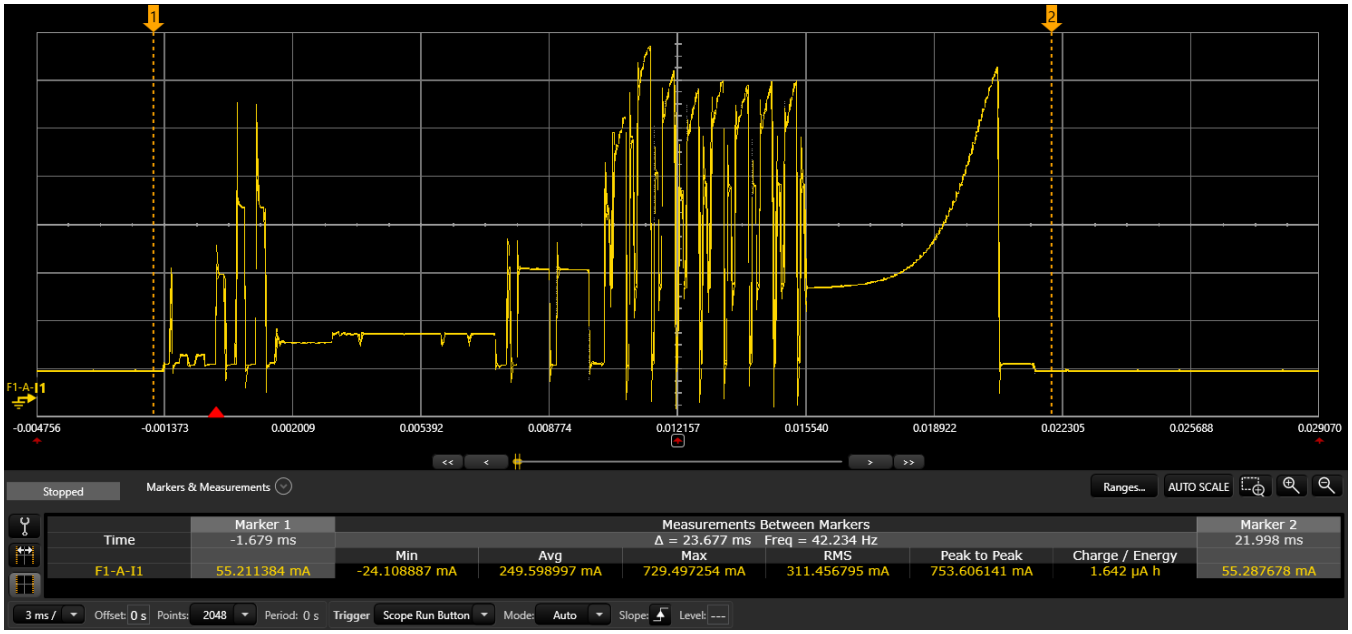

Figure 11: Module RF Calibration Current Profile

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14 Crystal Oscillator Requirements

Table 12: Oscillator Requirements

32.768 KHz Oscillator	
Frequency Accuracy	± 200 ppm
Duty Cycle	30% - 70%
Input Signal Amplitude	200 – 1800 mV, p-p
Signal Type	Square or Sine Wave
Clock Jitter	<10,000 ppm

Note: A 32.768 KHz crystal is required in order for the module to be fully functional. The module will not boot without it.

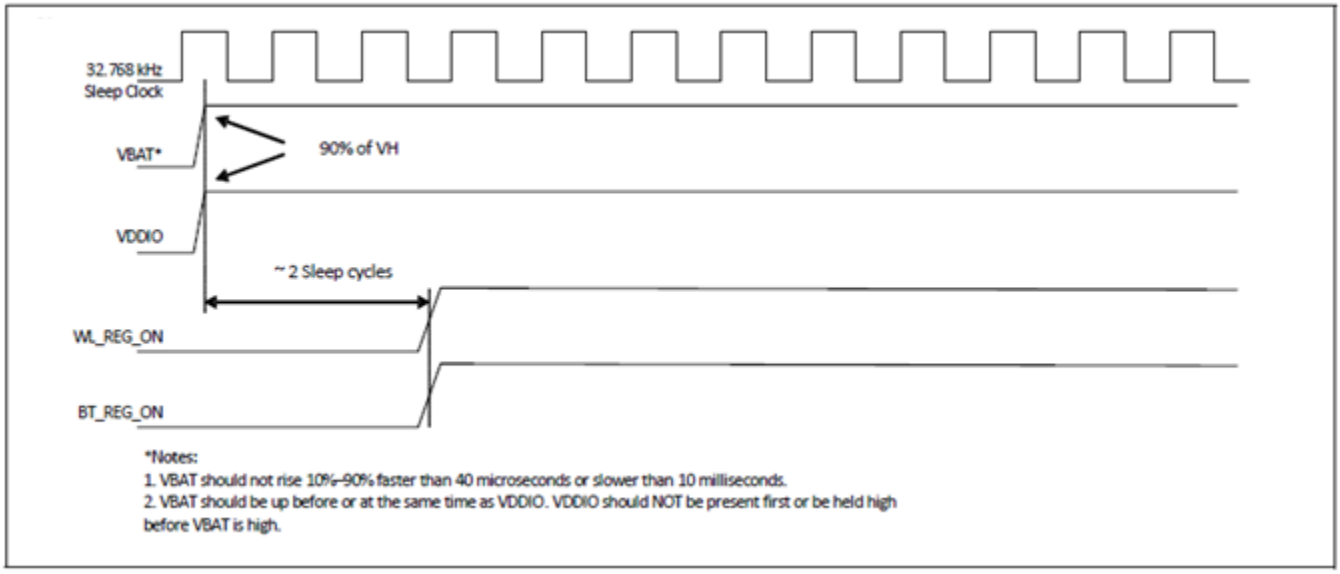

Figure 12: WLAN = ON, Bluetooth = ON

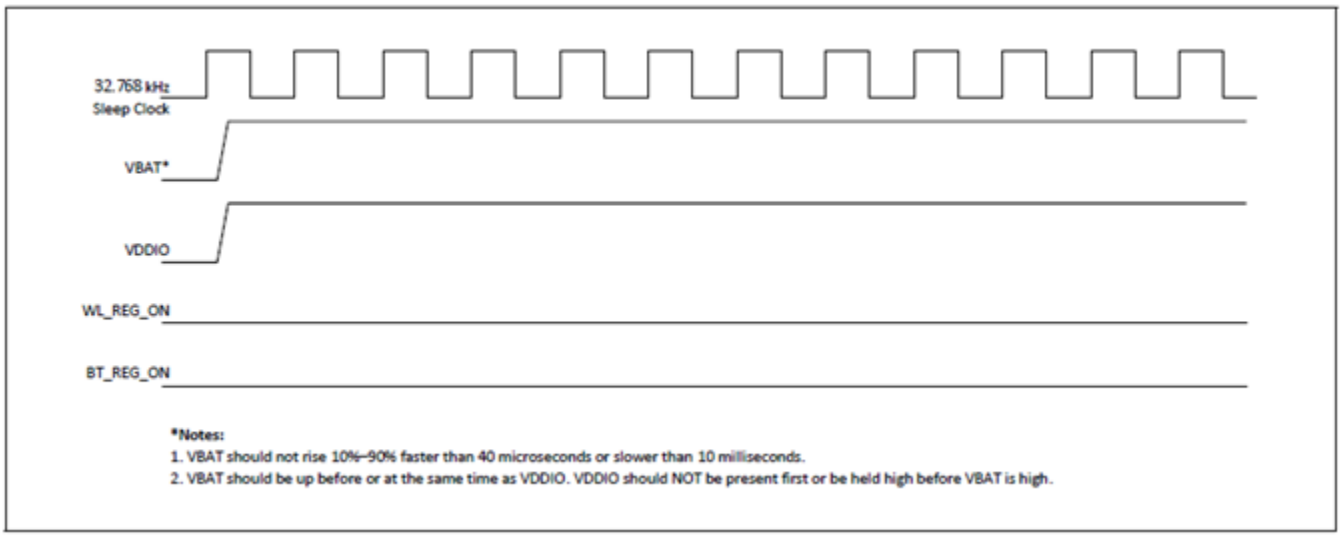

Figure 13: WLAN = OFF, Bluetooth = OFF

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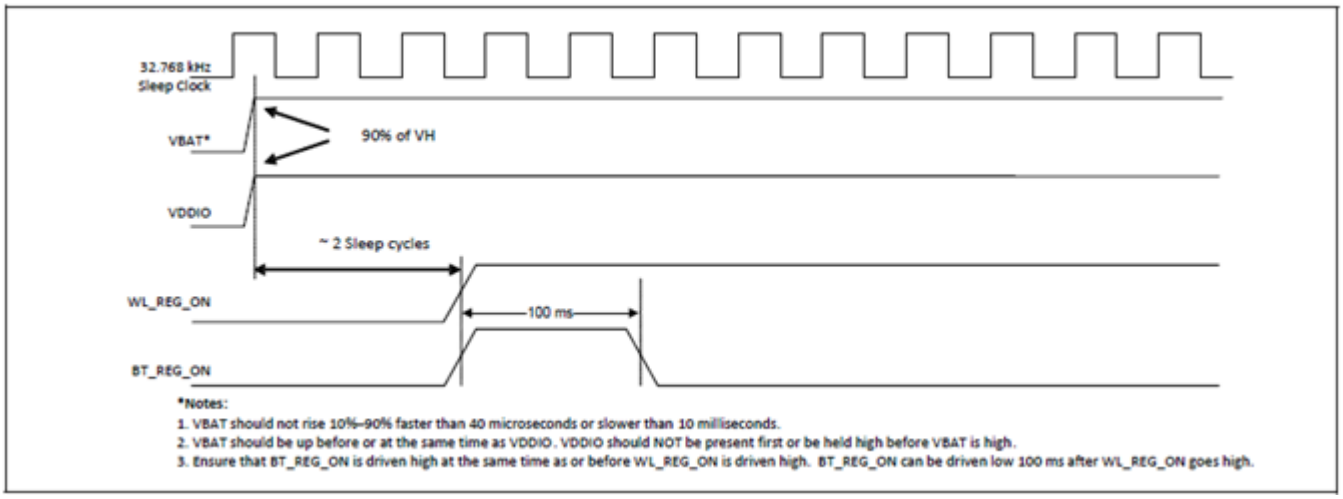

Figure 14: WLAN = ON, Bluetooth = OFF

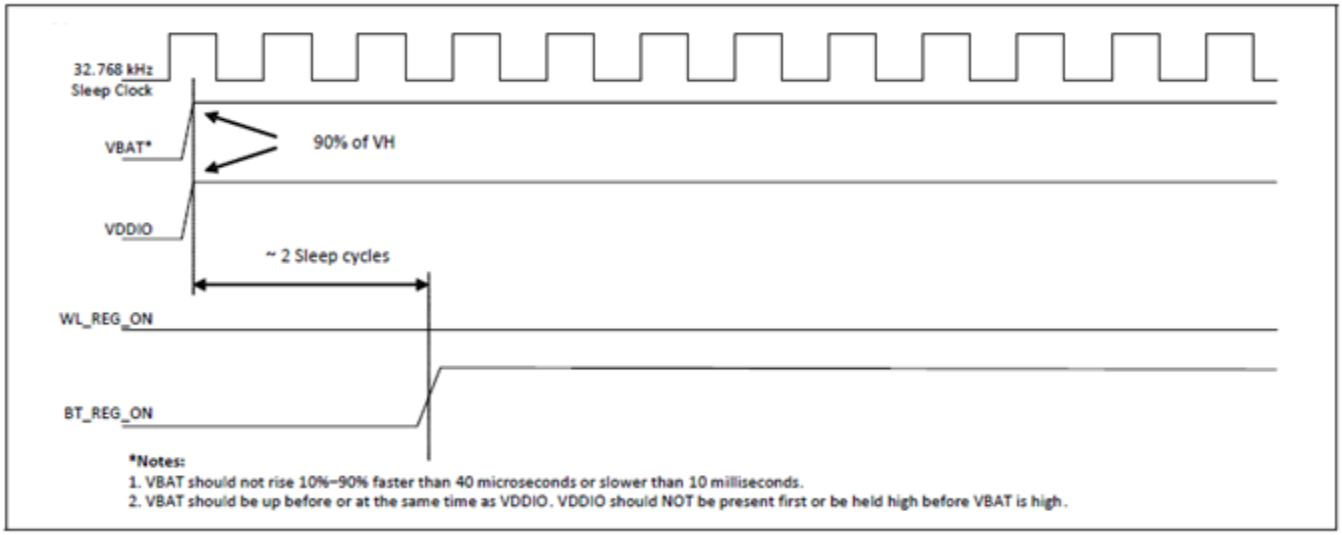

Figure 15: WLAN = OFF, Bluetooth = ON

14.1 WLAN RF Characteristics

2.4 GHz WLAN Transmitter Characteristics (TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 13: 2.4 GHz WLAN Transmitter RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps BPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet, 20 MHz	-	16	-	dBm
2 Mbps DSSS (b) TX Output Power	2 Mbps QPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet, 20 MHz	-	16	-	dBm
5.5 Mbps DSSS (b) TX Output Power	5.5 Mbps QPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet, 20 MHz	-	16	-	dBm
11 Mbps DSSS (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet, 20 MHz	-	16	-	dBm

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Parameter	Test Conditions	Min	Typ	Max	Unit
6 Mbps OFDM (g) TX Output Power	6 Mbps BPSK 802.11(g) Mask Compliance -5 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
9 Mbps OFDM (g) TX Output Power	9 Mbps BPSK 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
12 Mbps OFDM (g) TX Output Power	12 Mbps QPSK 802.11(g) Mask Compliance -10 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
18 Mbps OFDM (g) TX Output Power	18 Mbps QPSK 802.11(g) Mask Compliance -13 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
24 Mbps OFDM (g) TX Output Power	24 Mbps 16-QAM 802.11(g) Mask Compliance -16 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
36 Mbps OFDM (g) TX Output Power	36 Mbps 16-QAM 802.11(g) Mask Compliance -19 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
48 Mbps OFDM (g) TX Output Power	48 Mbps 64-QAM 802.11(g) Mask Compliance -22 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps 64-QAM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS0 OFDM (n) TX Output Power, 20 MHz	6.5 Mbps BPSK 802.11(n) Mask Compliance -5 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm
MCS1 OFDM (n) TX Output Power, 20 MHz	13 Mbps QPSK 802.11(n) Mask Compliance -10 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm
MCS2 OFDM (n) TX Output Power, 20 MHz	19.5 Mbps QPSK 802.11(n) Mask Compliance -13 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm
MCS3 OFDM (n) TX Output Power, 20 MHz	26 Mbps 16-QAM 802.11(n) Mask Compliance -16 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm
MCS4 OFDM (n) TX Output Power, 20 MHz	39 Mbps 16-QAM 802.11(n) Mask Compliance -19 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm
MCS5 OFDM (n) TX Output Power, 20 MHz	52 Mbps 64-QAM 802.11(n) Mask Compliance -22 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm
MCS6 OFDM (n) TX Output Power, 20 MHz	58.5 Mbps 64-QAM 802.11(n) Mask Compliance -25 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm

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Parameter	Test Conditions	Min	Typ	Max	Unit
MCS7 OFDM (n) TX Output Power, 20 MHz	65 Mbps 64-QAM 802.11(n) Mask Compliance -27 dB EVM RMS power over TX packet, 20 MHz	-	11	-	dBm

14.1.1 5 GHz WLAN Transmitter Characteristics

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 14: 5 GHz WLAN Transmitter RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
6 Mbps OFDM (a) TX Output Power	6 Mbps BPSK 802.11(a) Mask Compliance -5 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
9 Mbps OFDM (a) TX Output Power	9 Mbps BPSK 802.11(a) Mask Compliance -8 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
12 Mbps OFDM (a) TX Output Power	12 Mbps QPSK 802.11(a) Mask Compliance -10 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
18 Mbps OFDM (a) TX Output Power	18 Mbps QPSK 802.11(a) Mask Compliance -13 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
24 Mbps OFDM (a) TX Output Power	24 Mbps 16-QAM 802.11(a) Mask Compliance -16 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
36 Mbps OFDM (a) TX Output Power	36 Mbps 16-QAM 802.11(a) Mask Compliance -19 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
48 Mbps OFDM (a) TX Output Power	48 Mbps 64-QAM 802.11(a) Mask Compliance -22 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
54 Mbps OFDM (a) TX Output Power	54 Mbps 64-QAM 802.11(a) Mask Compliance -25 dB EVM RMS power over TX packet, 20 MHz	-	15	-	dBm
MCS0 OFDM (n/ac) TX Output Power	6.5 Mbps BPSK 802.11(n/ac) Mask Compliance -5 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS1 OFDM (n/ac) TX Output Power	13 Mbps QPSK 802.11(n/ac) Mask Compliance -10 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS2 OFDM (n/ac) TX Output Power	19.5 Mbps QPSK 802.11(n/ac) Mask Compliance -13 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS3 OFDM (n/ac) TX Output Power	26 Mbps 16-QAM 802.11(n/ac) Mask Compliance -16 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS4 OFDM (n/ac) TX Output Power	39 Mbps 16-QAM 802.11(n/ac) Mask Compliance -19 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS5 OFDM (n/ac) TX Output Power	52 Mbps 64-QAM 802.11(n/ac) Mask Compliance -22 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS6 OFDM (n/ac) TX Output Power	58.5 Mbps 64-QAM 802.11(n/ac) Mask Compliance -25 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm

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Parameter	Test Conditions	Min	Typ	Max	Unit
MCS7 OFDM (n/ac) TX Output Power	65 Mbps 64-QAM 802.11(n/ac) Mask Compliance -27 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS8 OFDM (ac) TX Output Power	78 Mbps 64-QAM 802.11(n/ac) Mask Compliance -30 dB EVM RMS power over TX packet, 20 MHz	-	13	-	dBm
MCS0 OFDM (ac) TX Output Power	13.5/29.3 Mbps BPSK 802.11(ac) Mask Compliance -5 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS1 OFDM (ac) TX Output Power	27/58.5 Mbps QPSK 802.11(ac) Mask Compliance -10 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS2 OFDM (ac) TX Output Power	40.5/87.8 Mbps QPSK 802.11(ac) Mask Compliance -13 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS3 OFDM (ac) TX Output Power	54/117 Mbps 16-QAM 802.11(ac) Mask Compliance -16 dB EVM RMS power over TX packet, 40/80 MHz	-	8.5	-	dBm
MCS4 OFDM (ac) TX Output Power	81/175.5 Mbps 16-QAM 802.11(ac) Mask Compliance -19 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS5 OFDM (n) TX Output Power	108/234 Mbps 64-QAM 802.11(ac) Mask Compliance -22 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS6 OFDM (n) TX Output Power	121.5/263.3 Mbps 64-QAM 802.11(ac) Mask Compliance -25 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS7 OFDM (n) TX Output Power	135/292.5 Mbps 64-QAM 802.11(ac) Mask Compliance -27 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS8 OFDM (n) TX Output Power	162/351Mbps 256-QAM 802.11(ac) Mask Compliance -30 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm
MCS9 OFDM (n) TX Output Power	180/390 Mbps 256-QAM 802.11(ac) Mask Compliance -32 dB EVM RMS power over TX packet, 40/80 MHz	-	9.5	-	dBm

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14.1.2 2.4 GHz WLAN Receiver Characteristics

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 15: 2.4 GHz WLAN Receiver RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) RX Sensitivity	8% PER, 20 MHz	-	-93	-	dBm
2 Mbps DSSS (b) RX Sensitivity	8% PER, 20 MHz	-	-91	-	dBm
5.5 Mbps DSSS (b) RX Sensitivity	8% PER, 20 MHz	-	-90	-	dBm
11 Mbps DSSS (b) RX Sensitivity	8% PER, 20 MHz	-	-87	-	dBm
6 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-90	-	dBm
9 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-89	-	dBm
12 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-87	-	dBm
18 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-85	-	dBm
24 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-82	-	dBm
36 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-78	-	dBm
48 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-74	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER, 20 MHz	-	-73	-	dBm
MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-90	-	dBm
MCS1 (13 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-88	-	dBm
MCS2 (19.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-85	-	dBm
MCS3 26 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-82	-	dBm
MCS4 39 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-78	-	dBm
MCS5 52 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-74	-	dBm
MCS6 58.5 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-72	-	dBm
MCS7 65 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-71	-	dBm
802.11b RX Overload Level – 20 MHz	8% PER, 11 Mbps	-10	-	-	dBm
802.11g RX Overload Leve l – 20 MHz	10% PER, 54 Mbps	-20	-	-	dBm
802.11n RX Overload Level – 20 MHz	10% PER, MCS7	-20	-	-	dBm

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14.1.3 5 GHz WLAN Receiver Characteristics

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 16: 5 GHz WLAN Receiver RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
6 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-90	-	dBm
9 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-89	-	dBm
12 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-87	-	dBm
18 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-85	-	dBm
24 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-82	-	dBm
36 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-78	-	dBm
48 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-74	-	dBm
54 Mbps OFDM (a) RX Sensitivity	10% PER, 20 MHz	-	-73	-	dBm
MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-90	-	dBm
MCS1 (13 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-87	-	dBm
MCS2 (19.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-85	-	dBm
MCS3 26 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-82	-	dBm
MCS4 39 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-78	-	dBm
MCS5 52 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-74	-	dBm
MCS6 58.5 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-73	-	dBm
MCS7 65 Mbps OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-71	-	dBm
MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-88	-	dBm
MCS1 (13 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-85	-	dBm
MCS2 (19.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-82	-	dBm
MCS3 26 Mbps OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-79	-	dBm
MCS4 39 Mbps OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-76	-	dBm
MCS5 52 Mbps OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-71	-	dBm
MCS6 58.5 Mbps OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-70	-	dBm
MCS7 65 Mbps OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-68	-	dBm
802.11(ac) MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-89	-	dBm
802.11(ac) MCS1 (13 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-87	-	dBm
802.11(ac) MCS2 (19.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-85	-	dBm
802.11(ac) MCS3 (26 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-82	-	dBm
802.11(ac) MCS4 (39 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-78	-	dBm
802.11(ac) MCS5 (52 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-74	-	dBm
802.11(ac) MCS6 (58.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-72	-	dBm
802.11(ac) MCS7 (65 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-71	-	dBm
802.11(ac) MCS8 (78 Mbps) OFDM (n) RX Sensitivity	10% PER, 20 MHz	-	-65	-	dBm

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Parameter	Test Conditions	Min	Typ	Max	Unit
802.11(ac) MCS0 (13.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-88	-	dBm
802.11(ac) MCS1 (27 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-85	-	dBm
802.11(ac) MCS2 (40.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-82	-	dBm
802.11(ac) MCS3 (54 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-79	-	dBm
802.11(ac) MCS4 (81 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-76	-	dBm
802.11(ac) MCS5 (108 Mbps OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-71	-	dBm
802.11(ac) MCS6 (121.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-70	-	dBm
802.11(ac) MCS7 (135 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-67	-	dBm
802.11(ac) MCS8 (162 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-64	-	dBm
802.11(ac) MCS9 (180 Mbps) OFDM (n) RX Sensitivity	10% PER, 40 MHz	-	-61	-	dBm
MCS0 (29.3 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-84	-	dBm
MCS1 (58.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-81	-	dBm
MCS2 (87.8 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-78	-	dBm
MCS3 (117 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-75	-	dBm
MCS4 (175.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-72	-	dBm
MCS5 (234 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-68	-	dBm
MCS6 (263.3 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-65	-	dBm
MCS7 (292.5 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-64	-	dBm
MCS8 (351 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-59	-	dBm
MCS9 (390 Mbps) OFDM (n) RX Sensitivity	10% PER, 80 MHz	-	-56	-	dBm
802.11a RX Overload Level – 20 MHz	10% PER, All Rates	-30	-	-	dBm
802.11n RX Overload Level– 20 MHz	10% PER, All Rates	-30	-	-	dBm
802.11n RX Overload Level– 40 MHz	10% PER, All Rates	-30	-	-	dBm
802.11ac RX Overload Level – 20 MHz	10% PER, All Rates	-30	-	-	dBm
802.11ac RX Overload Level– 40 MHz	10% PER, All Rates	-30	-	-	dBm
802.11ac RX Overload Level– 80 MHz	10% PER, All Rates	-30	-	-	dBm

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14.2 Bluetooth RF Characteristics

14.2.1 Bluetooth Transmitter Characteristics

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 17: Bluetooth Transmitter RF Characteristics

Parameter	Test Conditions	Min	Typical	Max	Unit
Transmit Frequency	T_{amb} = +25°C, 3.3V	2402	-	2480	MHz
Bluetooth 1 Mbps GFSK Transmit Power	T_{amb} = +25°C, 3.3V	-	8	-	dBm
Bluetooth EDR Transmit Power	T_{amb} = +25°C, 3.3V	-	7	-	dBm
Bluetooth EDR Relative Transmit Power	T_{amb} = +25°C, 3.3V	-4		1	dB
Bluetooth Low Energy (BLE) Transmit Power	T_{amb} = +25°C, 3.3V	-	6	-	dBm

14.2.2 Bluetooth Receiver Characteristics

(TA = +25°C, VBAT = 3.3V, VDDIO = 1.8V)

Table 18: Bluetooth Receiver RF Characteristics

Parameter	Test Conditions	Min	Typical	Max	Unit
Receive Frequency	T_{amb} = +25°C, 3.3V	2402	-	2480	MHz
Bluetooth 1 Mbps GFSK Sensitivity	BER=0.1%	-	-88	-	dBm
Bluetooth 2 Mbps EDR Sensitivity	BER=0.01%	-	-90	-	dBm
Bluetooth 3 Mbps EDR Sensitivity	BER=0.01%	-	-84.5	-	dBm
Bluetooth Low Energy (BLE) Sensitivity	T_{amb} = +25°C, 3.3V	-	-92	-	dBm

15 WLAN Host Interface

15.1 SDIO Interface

The Sterling-LWB5 module SDIO interface supports SDIO Version 3.0, including the UHS-1 modes.

Table 19: SDIO Pins

PIN	4 Bit Mode	1 Bit Mode
18	DATA0	DATA
19	DATA1	IRQ
20	DATA2	RW
21	DATA3	N/C
15	CLK	CLK
17	CMD	CMD

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15.1.1 DC Characteristics – SDIO Interface Pins

Table 20: DC Characteristics SDIO I/O

Parameter	Test Conditions	Min	Typical	Max	Unit
Logic input low, V_{IL}	VDDIO = 1.8V	-	-	0.58	V
Logic input high, V_{IH}	VDDIO = 1.8V	1.27	-	-	V
Logic output low, V_{OL}	VDDIO = 1.8V, 2mA	-	-	0.45	V
Logic output high, V_{OH}	VDDIO = 1.8V, 2mA	1.4	-	-	V

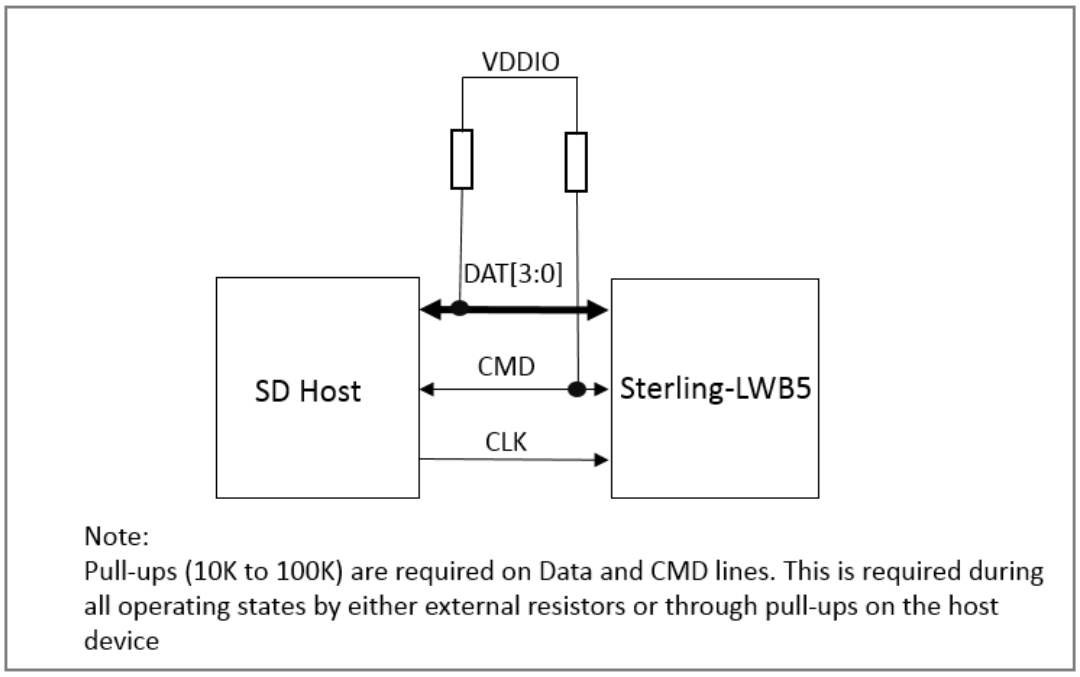

Figure 16: Signal Connections to SDIO Host (SD 4-Bit Mode)

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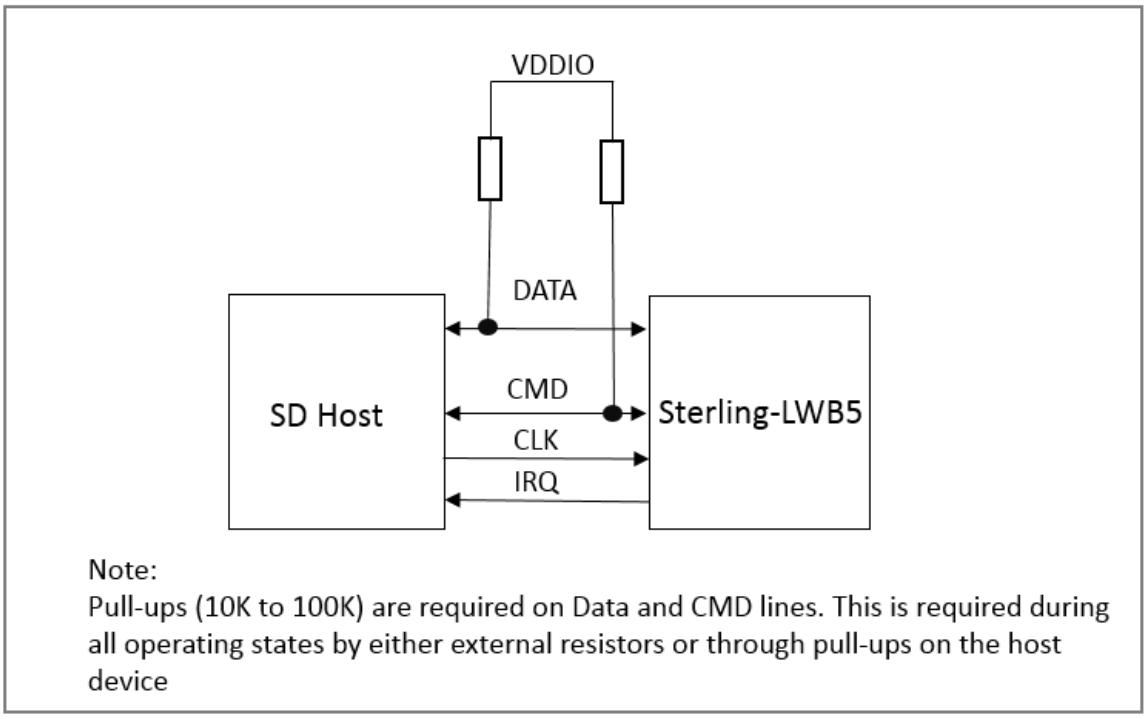

Figure 17: Signal Connections to SDIO Host (SD 1-Bit Mode)

16 Bluetooth UART Host Interface

16.1 Overview

The Sterling-LWB5 uses a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command. The UART also supports the 3-wire *UART Transport Layer* which reduces the number of signal lines required by eliminating the CTS and RTS signals.

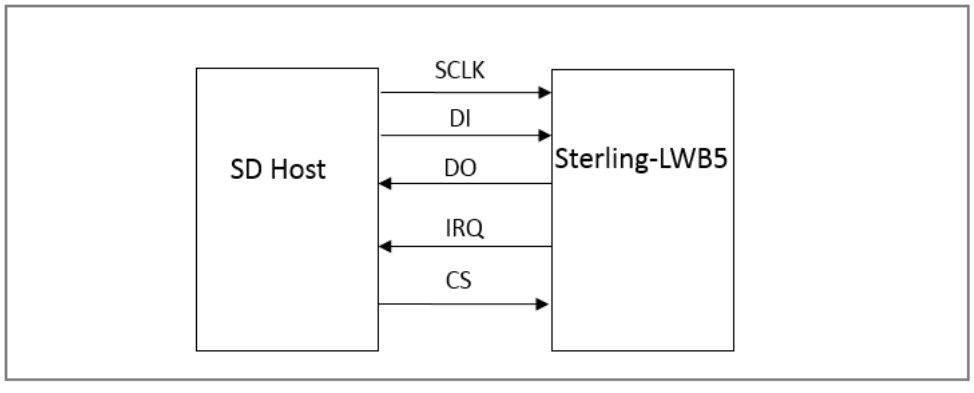

Figure 18: UART Connection from Sterling-LWB5 to Host

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16.1.1 DC Characteristics – SDO Interface Pins

Table 21: Bluetooth (UART) DC Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Input high voltage	VDDIO = 1.8V	1.7	-		V
Input low voltage	VDDIO = 1.8V	-	-	0.63	V
Output high voltage @2mA	VDDIO = 1.8V	1.4	-		V
Output low voltage @2mA	VDDIO = 1.8V	-	-	0.45	V

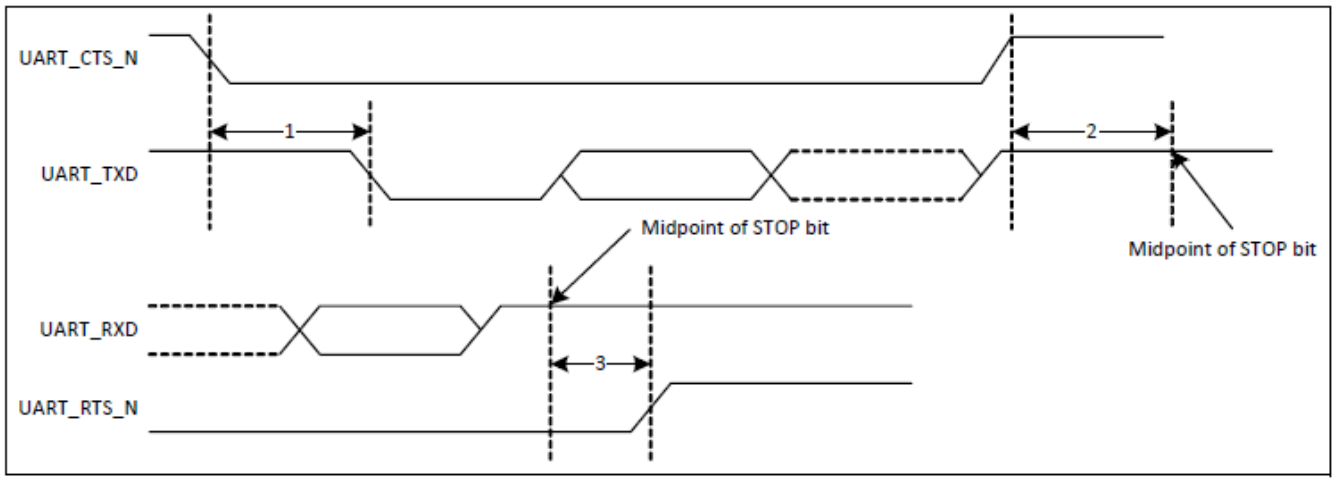

Figure 19: UART Timing

16.2 Soldering Recommendations

16.2.1 Reflow for Lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

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16.3 Recommended Reflow Profile for Lead Free Solder

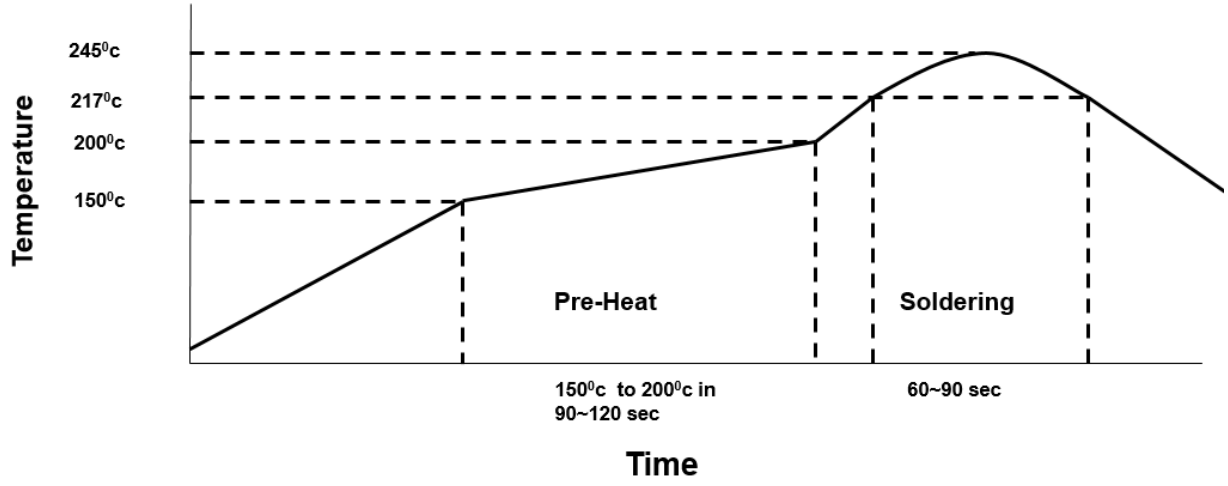

Figure 20: Recommended Soldering Profile

Note: The quality of solder joints on the surface mount pads where they contact the host board should meet the appropriate IPC Specification. See IPC-A-610-D Acceptability of Electronic Assemblies, section 8.2.1 “Bottom Only Terminations.”

17 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

18 Optical Inspection

After soldering the Module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads, or vias.

19 Rework

The Sterling-LWB5 module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Note: Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage.

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20 Shipping, Handling, and Storage

20.1 Shipping

Bulk orders of the Sterling-LWB5 SIP module are delivered in reels of 1000. Bulk orders for the U.FL and chip antenna modules are delivered in reels of 1000.

20.2 Handling

The Sterling-LWB5 modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

20.3 Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

20.4 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40ºC and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX.

Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

20.5 Repeated Reflow Soldering

Note: Only a single reflow soldering process is encouraged for host boards.

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21 REGULATORY

Note: For complete regulatory information, refer to the Sterling-LWB5 Regulatory Information document which is also available from the Sterling-LWB5 product page.

The Sterling-LWB5 holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	TFB-1004
EU	N/A
Canada (ISED)	5969A-1004
Japan (MIC)	201-180720

22 BLUETOOTH SIG QUALIFICATION

22.1 Overview

The Sterling LWB5 module is listed on the Bluetooth SIG website as a qualified Controller Subsystem.

Design Name	Owner	Declaration ID	Link to listing on the SIG website
450-0162	Laird	D057228	Sterling LWB5 450-0162 (Base Module)
450-0169	Laird	D057228	Sterling LWB5 450-0169 (Chip Antenna Module)
450-0168	Laird	D057228	Sterling LWB5 450-0168 (U.FL Module)
450-0171	Laird	D057228	Sterling LWB5 450-0171 (U.FL Dev Board)
450-0172	Laird	D057228	Sterling LWB5 450-0171 (Chip Antenna Dev Board)

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.org

The following is a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document, (login is required to views this document):

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

22.2 Qualification Steps When Referencing a Laird Controller Subsystem Design

To qualify your product when referencing a Laird Controller Subsystem design, follow these steps:

1. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

Note: A user name and password are required to access this site.

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2. In step 1, select the option, New Listing and Reference a Qualified Design.
3. Enter ***185913*** in the Controller Subsystem table entry.
4. Enter your complimentary Host Subsystem and optional Profile Subsystem in the table entry.
5. Select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page.

Note: Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

---

6. Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document accessible from the site.

Your new design will be listed on the SIG website and you can print your Certificate and DoC.

For further information please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

If you require assistance with the qualification process please contact our recommended Bluetooth Qualification Expert (BQE), Steve Flooks, steve.flook@eurexuk.com.

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23 Chip Antenna Performance

23.1 Summary of Antenna Performance

Table 22: Typical Antenna Performance

Item	Channel	Frequency (MHz)	Ptx (dBm)	TRP (dBm)	Power Gain (dB)	Expected Power Gain (dB)
1	1	2412	12.4	10.6	-1.8	-3.5
2	6	2437	12.1	10.4	-1.7	-3.5
3	11	2462	11.9	9.6	-2.3	-3.5
4	36	5180	10.6	7.2	-3.3	-2.5
5	100	5500	11.8	7.6	-4.2	-2.5
6	165	5825	11.1	3.1	-8.0	-2.5

Item	Channel	Frequency (MHz)	Ptx (dBm)	Peak EIRP (dBm)	Peak Gain (dB)	Expected Peak Gain (dB)
1	1	2412	12.4	13.6	1.2	1.0
2	6	2437	12.1	13.3	1.2	1.0
3	11	2462	11.9	12.2	0.4	1.0
4	36	5180	10.6	9.9	-0.7	4.0
5	100	5500	11.8	10.6	-1.2	4.0
6	165	5825	11.1	6.3	-4.8	4.0

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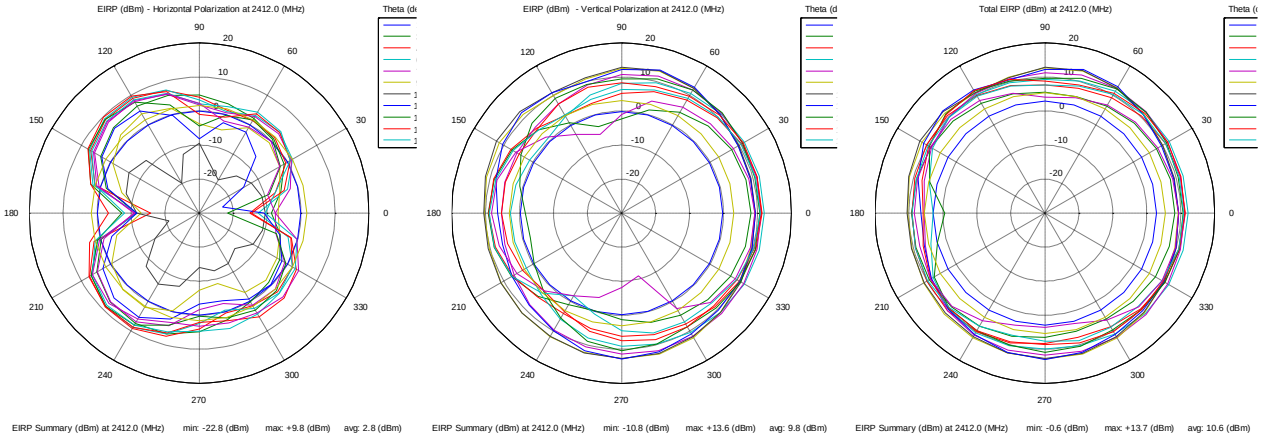
23.2 - 2.4 GHz Radiated Performance

EIRP Azimuth Cut



3D Plots:

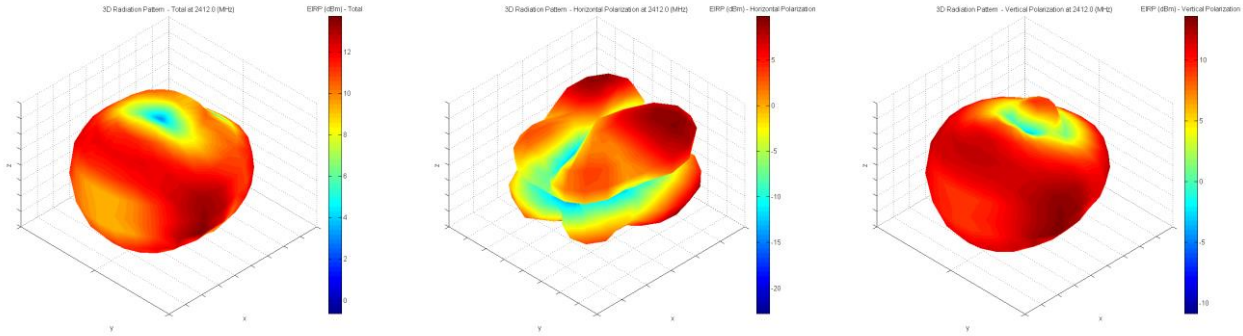


Figure 21: Channel 1 - 2412 MHz Vertical, Horizontal, and Total Patterns

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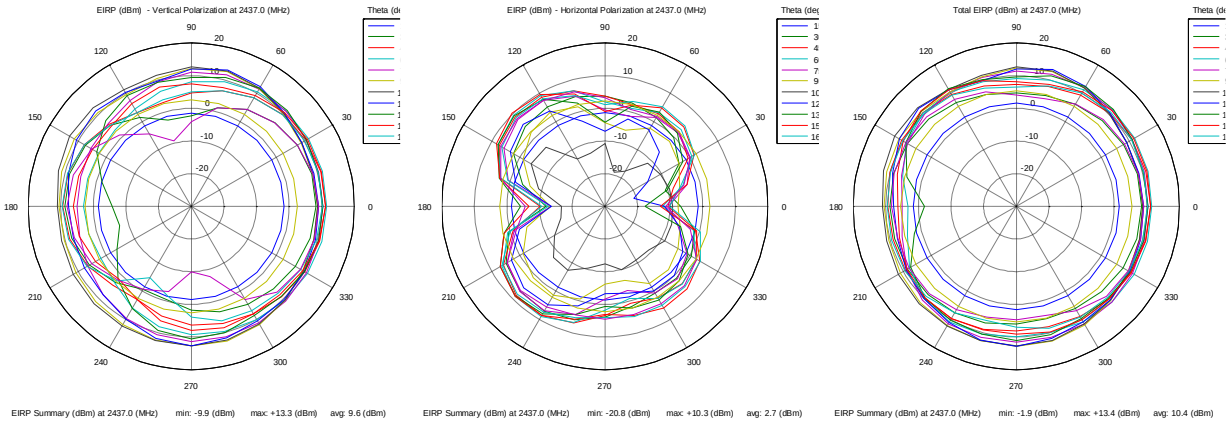
EIRP Azimuth Cut



3D Plots:

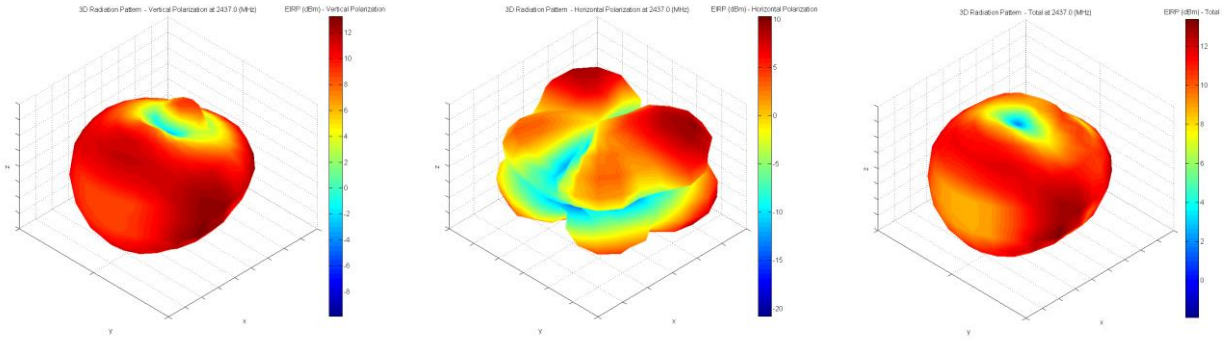


Figure 22: Channel 6 - 2437 MHz Vertical, Horizontal, and Total Plots

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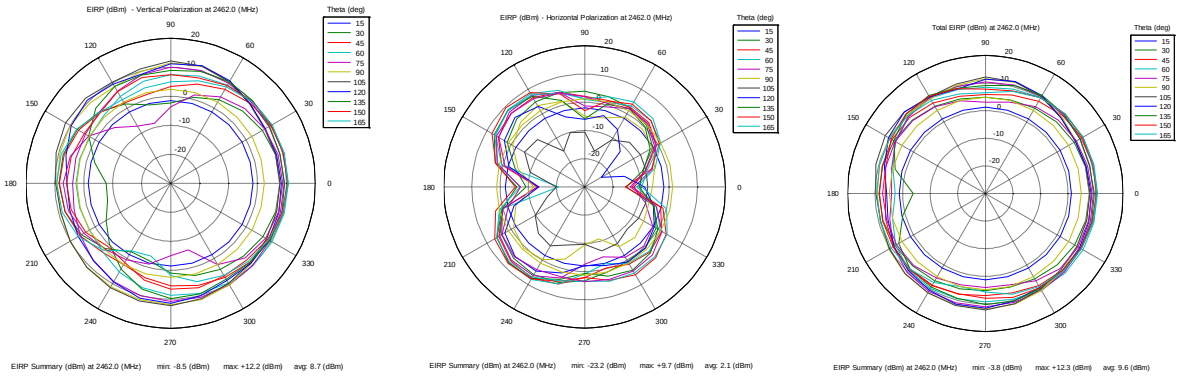
EIRP Azimuth Cut



3D Plots:

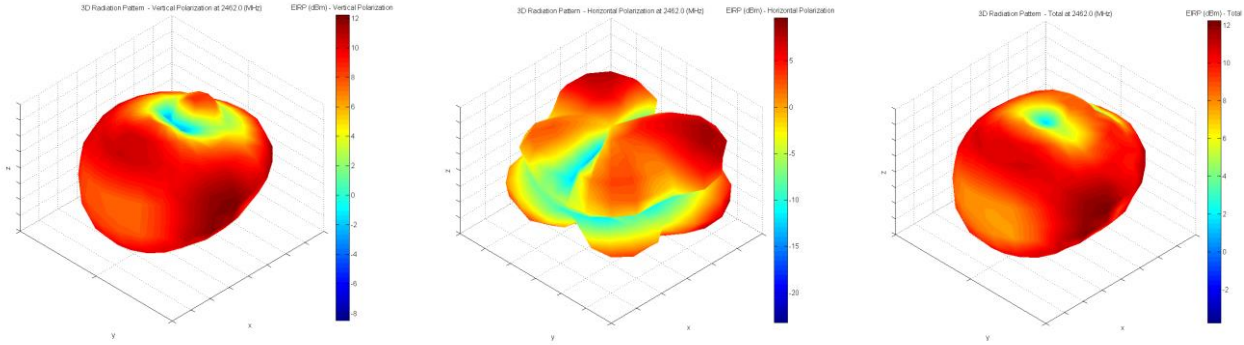


Figure 23: Channel 11 - 2462 MHz Vertical, Horizontal, and Total Patterns

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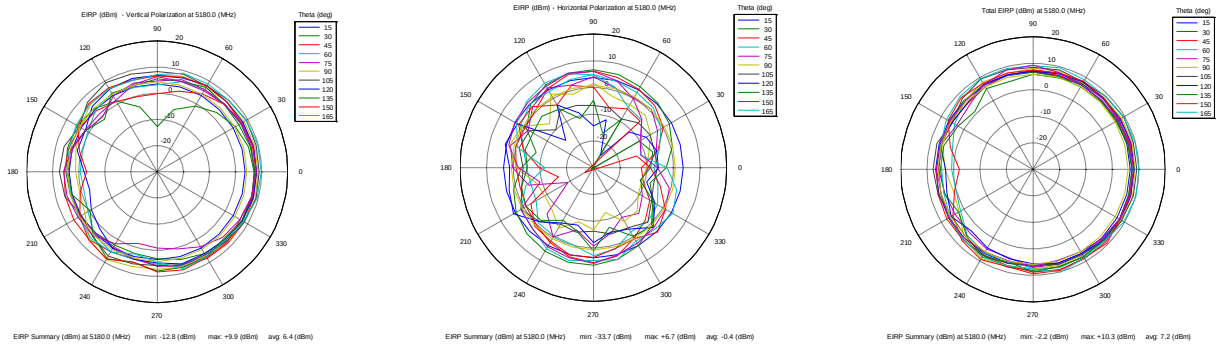
23.3 5 GHz Radiated Performance

Channel 36: 5180 MHz

EIRP Azimuth Cut



3D Plots:

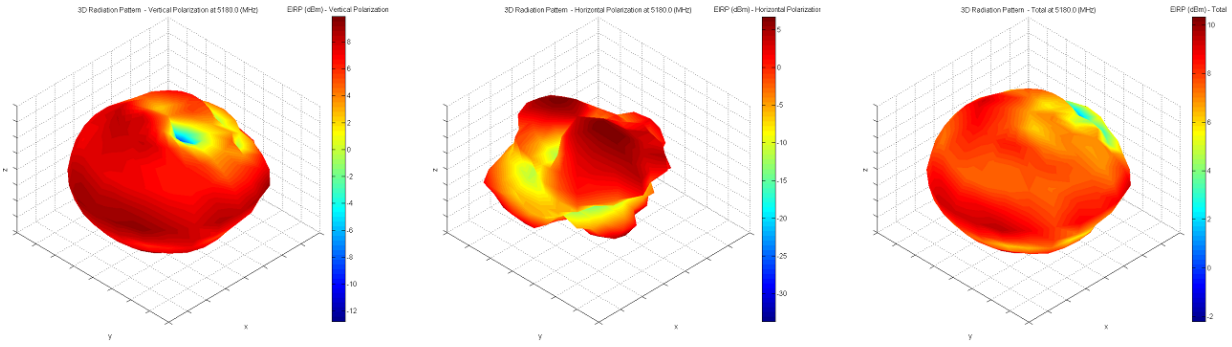
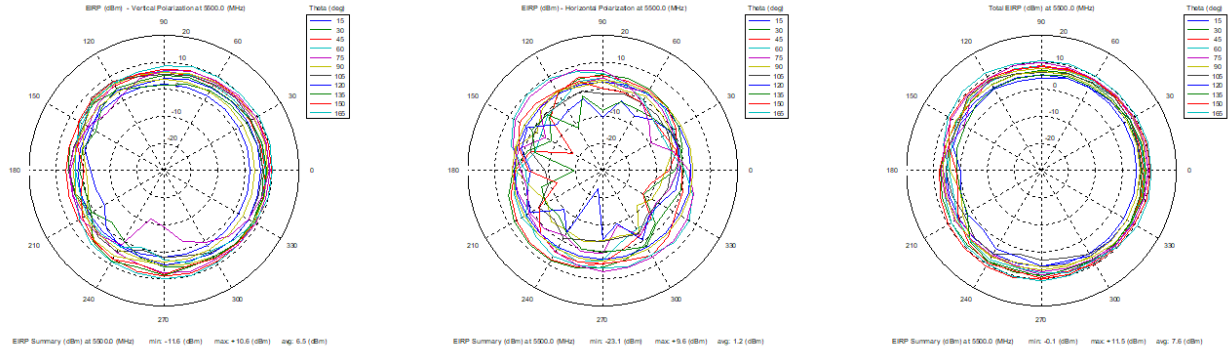


Figure 24: Channel 36 – 5180 MHz Vertical, Horizontal, and Total Patterns

EIRP Azimuth Cut



3D Plots:

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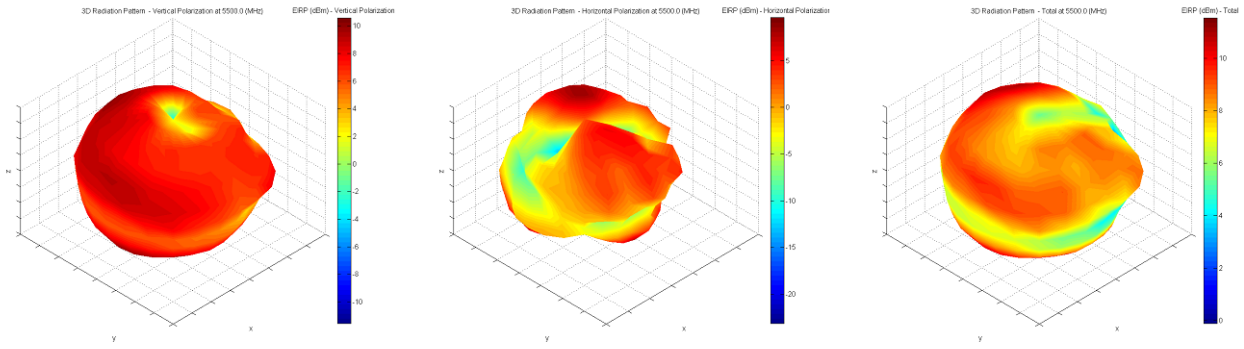
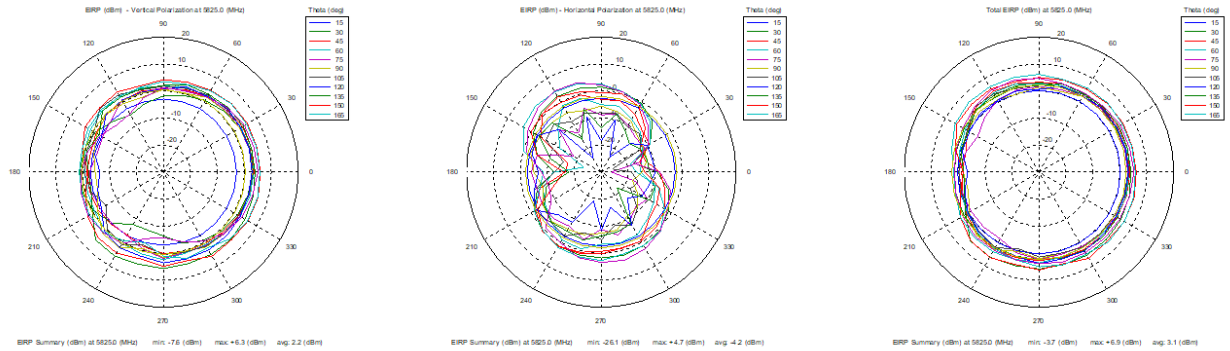


Figure 25: Channel 100 – 5500 MHz Vertical, Horizontal, and Total Patterns

EIRP Azimuth Cut



3D Plots:

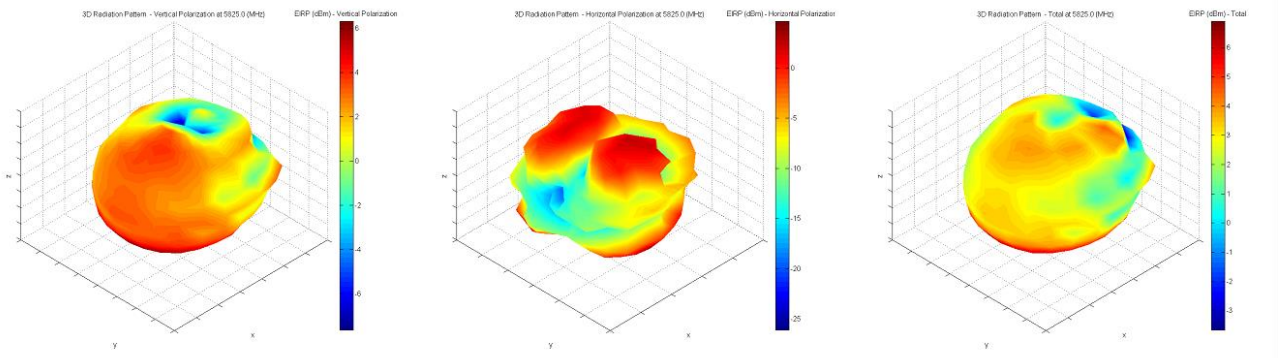


Figure 26: Channel 165 – 5825 MHz Vertical, Horizontal, and Total Patterns

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2762 4823

24 Base SIP Module Mechanical Data

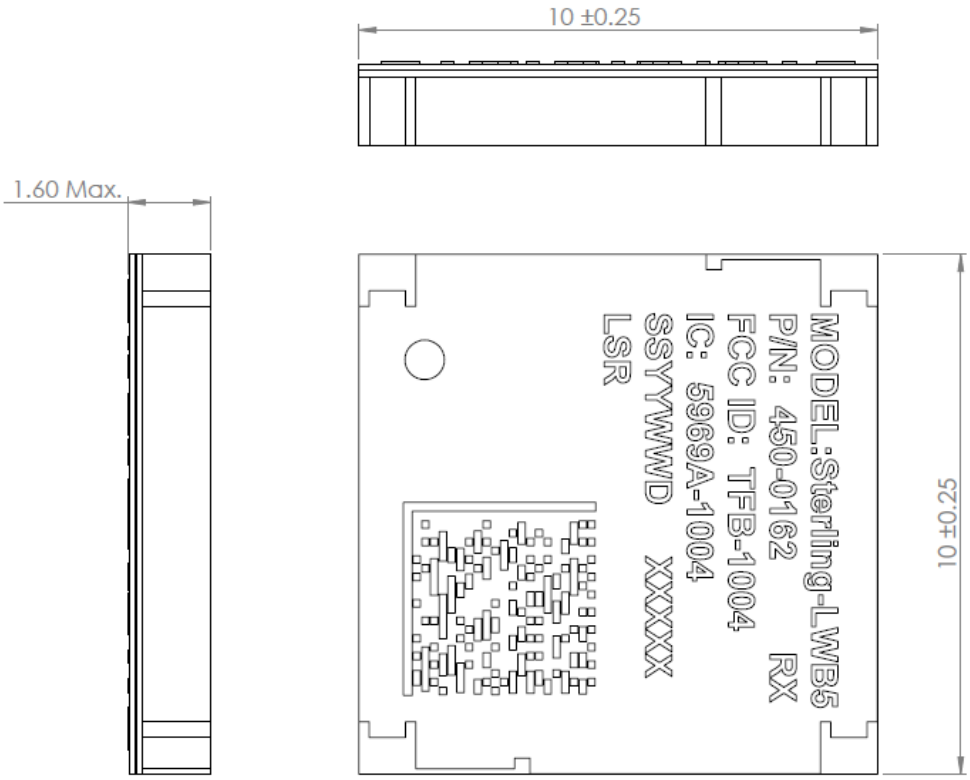


Figure 27: Base SIP Module Mechanical Dimensions

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Hong Kong: +852 2762 4823

25 Base SIP Module PCB Footprint

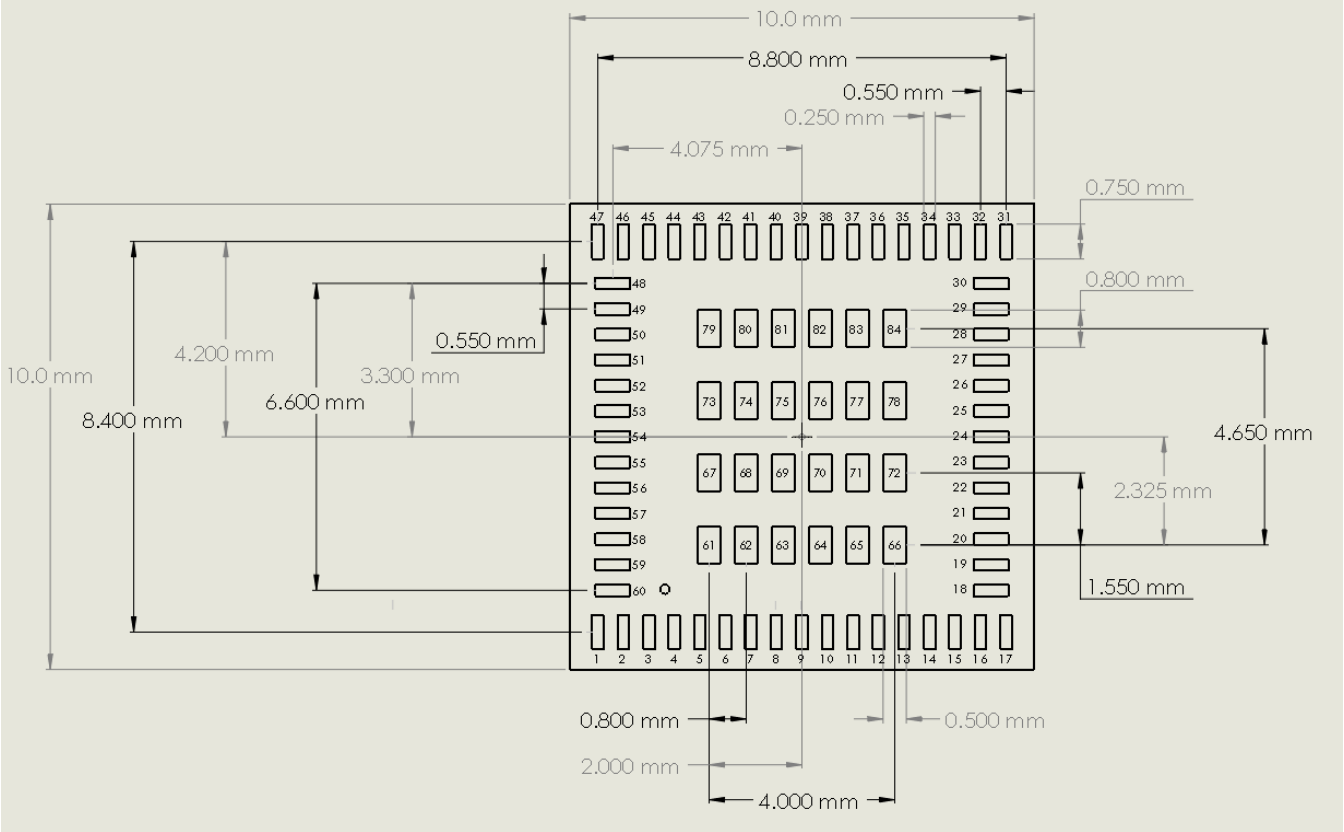

Figure 28: Base SIP Module Footprint (Top View)

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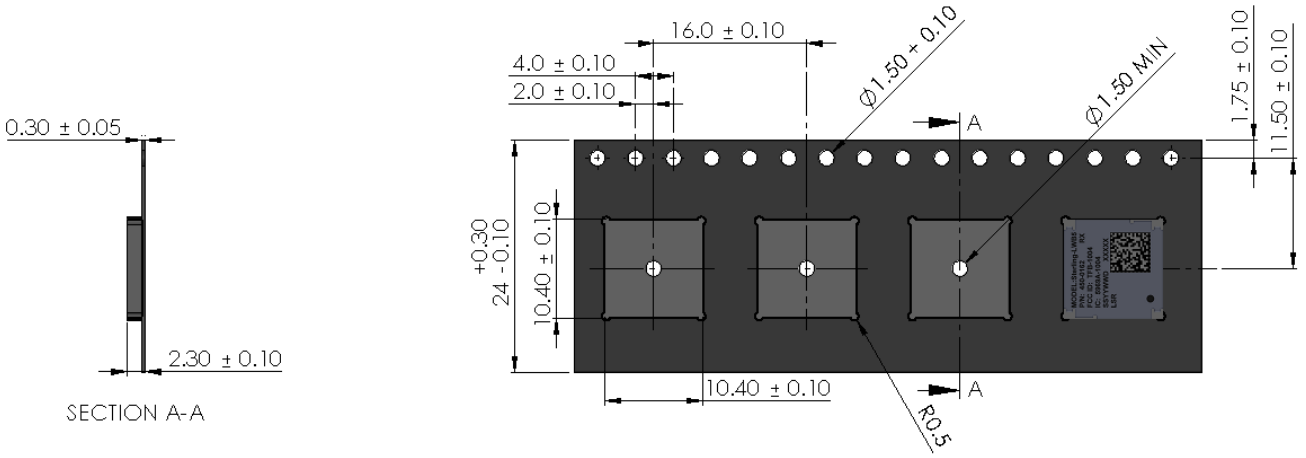
26 BASE SIP MODULE TAPE AND REEL PACKAGING

Tape Dimensions



NOTES:
1. DIM in mm.
2. 10 Sprocket Hole Pitch Cumulative Tolerance ± 0.10 mm.
3. Pocket Position Relative to Sprocket Hole Measured as True Position of Pocket, not Pocket Hole
4. A Full Reel contains 1000 modules.

Figure 29: Base SIP Module Tape and Reel Specification

Note: (Module must be in this Orientation when Feeding Tape)

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27 U.FL AND CHIP ANTENNA MECHANICAL DATA

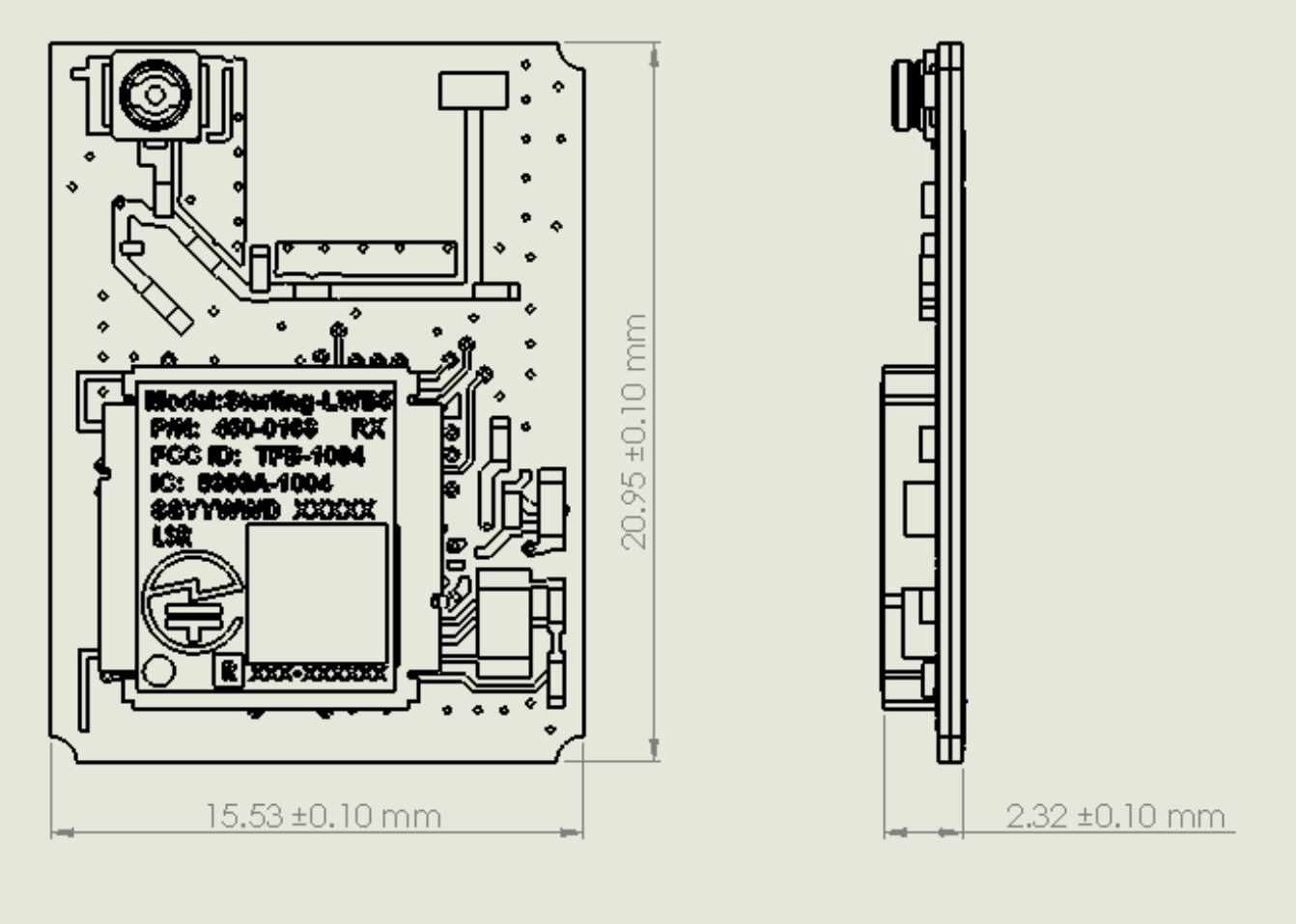

Figure 30: U.FL and Chip Antenna Mechanical Dimensions

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28 U.FL AND CHIP ANTENNA PCB FOOTPRINT

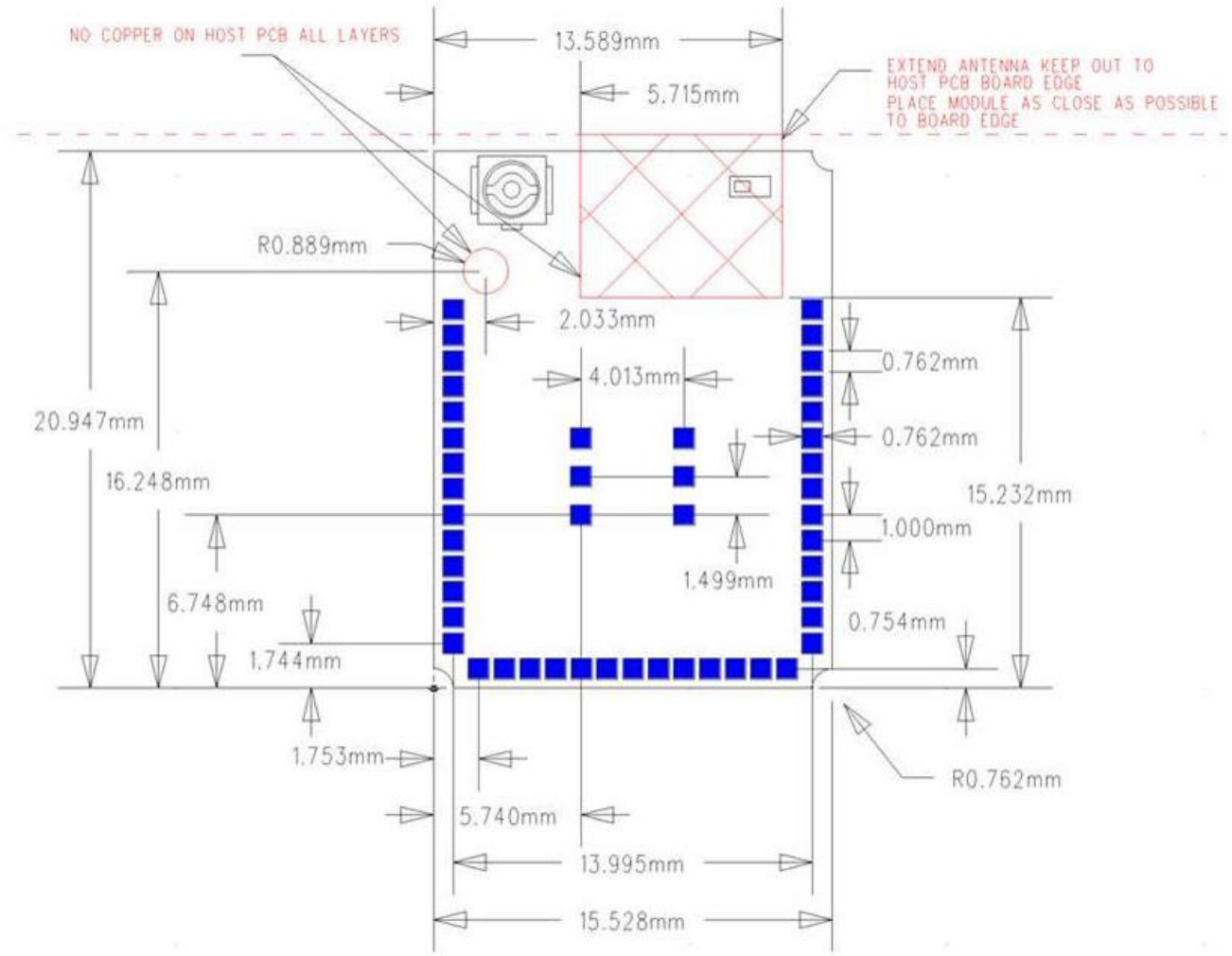

Figure 31: U.FL and Chip Antenna PCB Footprint

Note: All Pads .762mm x .762mm Square. Solder Mask and Paste Mask to be adjusted according to end user's assembly process.

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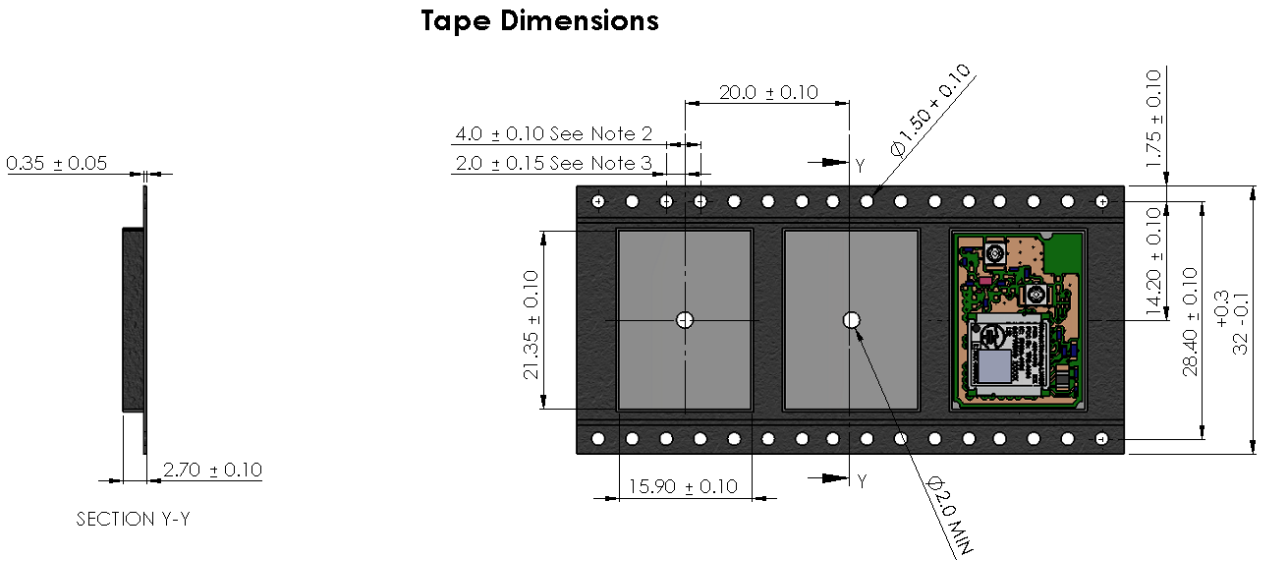
29 U.FL AND CHIP ANTENNA TAPE AND REEL PACKAGING



NOTES:
1. DIM in mm.
2. 10 Sprocket Hole Pitch Cumulative Tolerance ± 0.1mm.
3. Pocket Position Relative to Sprocket Hole Measured as True Position of Pocket, not Pocket Hole
4. A Full Reel contains 1000 modules.

Figure 32: U.FL and Chip Antenna Modules Tape and Reel Specification

Note: Module must be in this Orientation when Feeding Tape.

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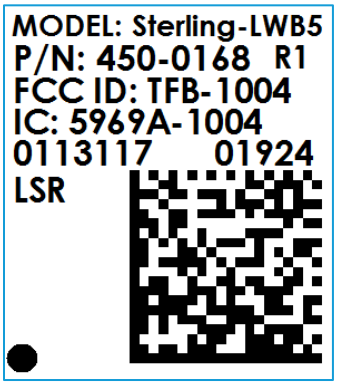
30 Device Markings

30.1 Rev 1 Devices

- Initial Release

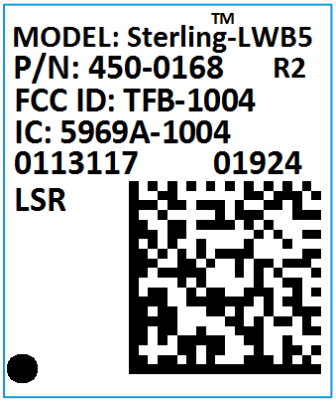


The shield on the 450-0162, 450-0168, and 450-0169 modules contains the following information:

- LSR Model: Sterling-LWB5 (All Caps and Trademark (TM) only on the SiP Module)
- Part Number and Revision:
  - Part Number: 450-0162, 450-0168, or 450-0169
  - R1 = Revision 1
- FCC ID: TFB-1004
- IC: 5969A-1004
- SSYYWWD = Date Code (SS=Manufacturer, YY=Year, WW=Week, D=Day)
- XXXXX = Incremental Serial Number
- 2D Barcode Format is Data Matrix Standard
- Pin 1 Marking

30.2 Rev 2 Devices

- Added Trademark (TM) Logo to part numbers 450-0168 and 450-0169.



31 Additional Information

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity Support Centre: https://www.lairdconnect.com/resources/support
Email: wireless.support@lairdconnectivity.com

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Europe: +44-1628-858-940
Hong Kong: +852 2923 0610
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.

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