CMOS Comparators

Comparator

V_o

"1"

V_{th}

V_i

"0"
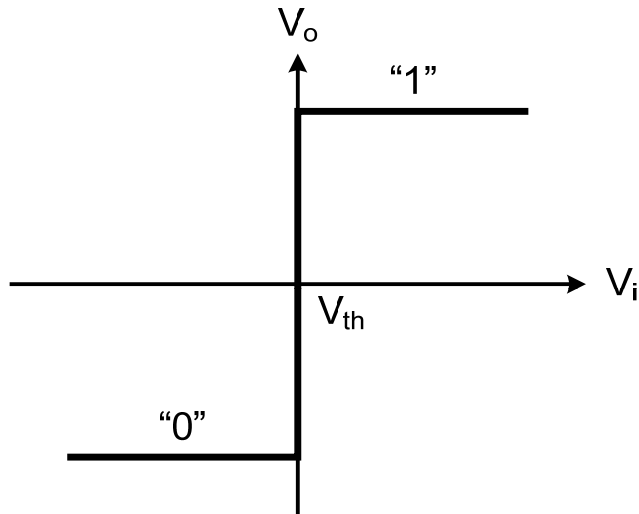
Transfer characteristic
(ideal)

V_i +

V_{th} −

V_o ("Digital")

Φ
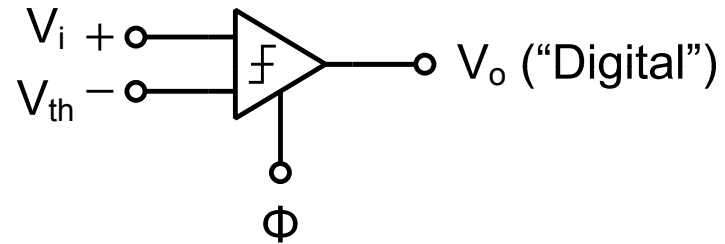
Circuit symbol

Detects the polarity of the analog input signal and produces a digital output (1 or 0) correspondingly – zero-crossing detector

Applications

- Voltage/current level comparison (A/D conversion)

- Digital communication receivers ("slicer" or decision circuit)

- Memory sense amplifier

- DC-DC converter with digital control

Design Considerations

- Accuracy (offset, resolution)

- Sensitivity (gain)

- Metastability (gain)

- Settling time (small-signal BW, slew rate)

- Overdrive recovery (memory)

- CMRR

- Power consumption

Comparator

Amplification   Clipping
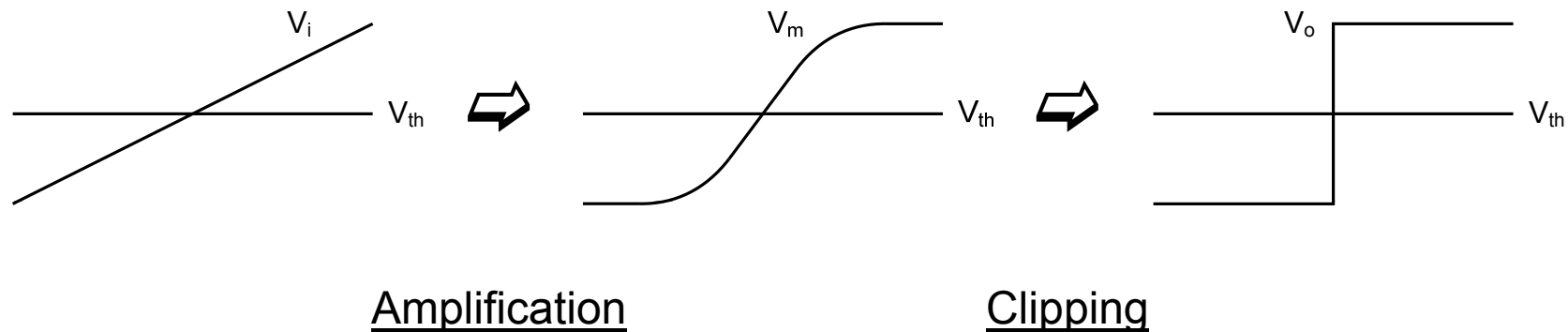
- Precise gain and linearity are unnecessary → simple, low-gain, open-loop, wideband amplifiers + latch (positive feedback).

- More gain can be derived by cascading multiple gain stages.
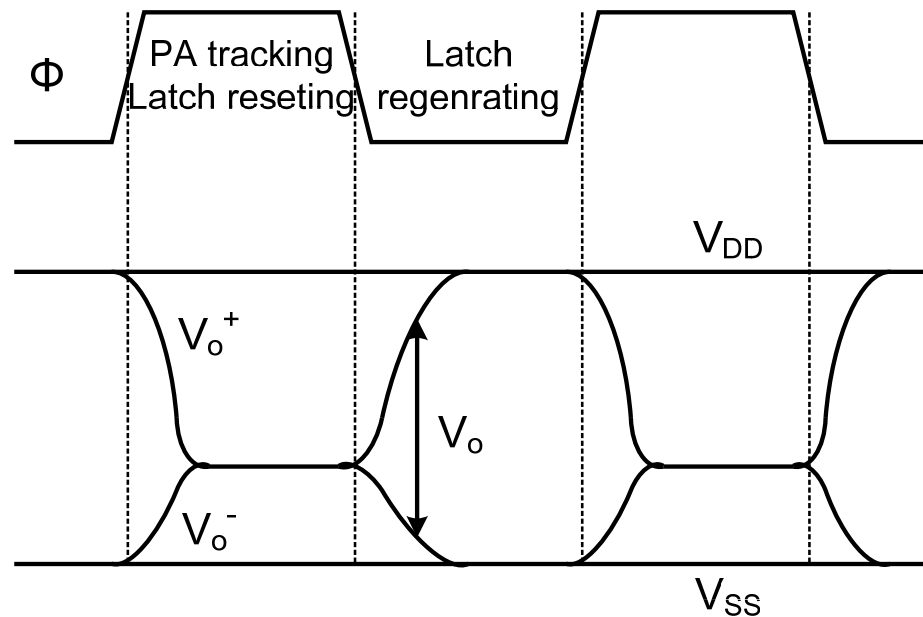
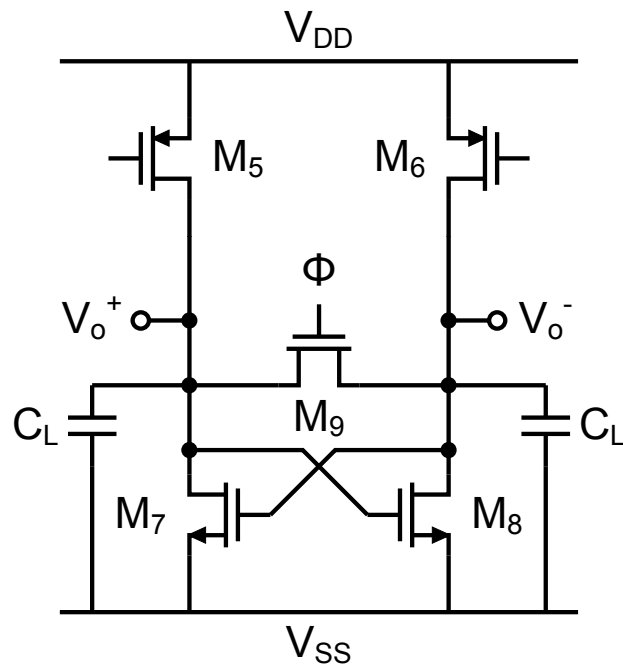- Built-in sampling function with latched comparators.

A Typical CMOS Comparator
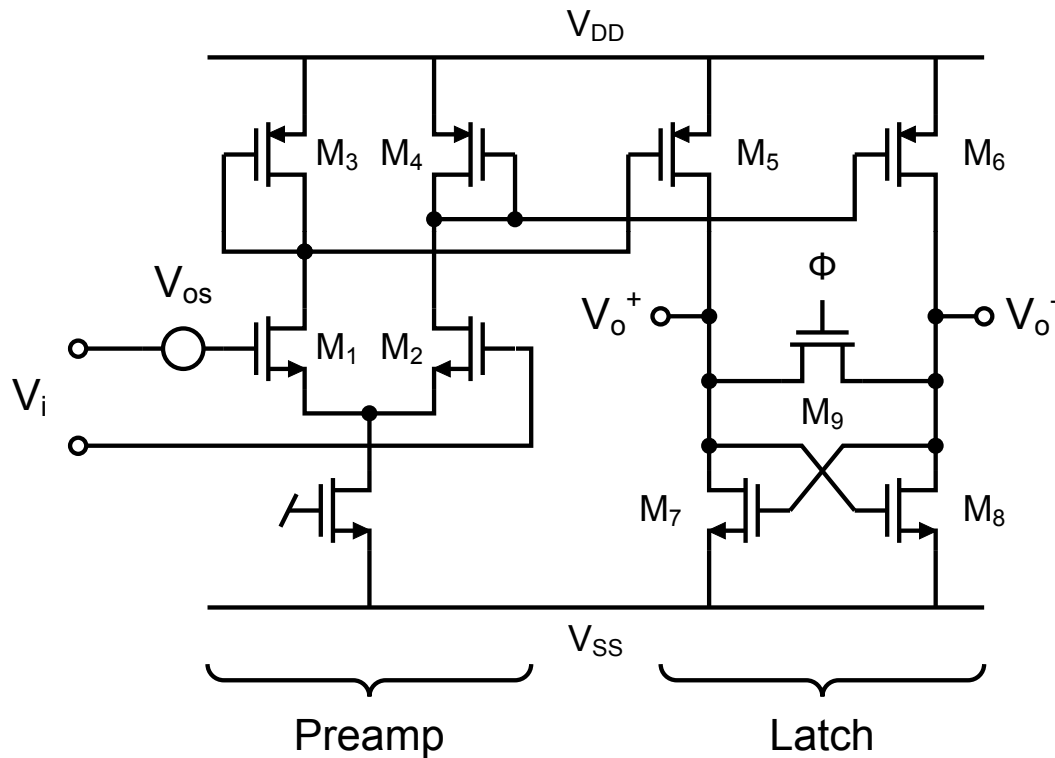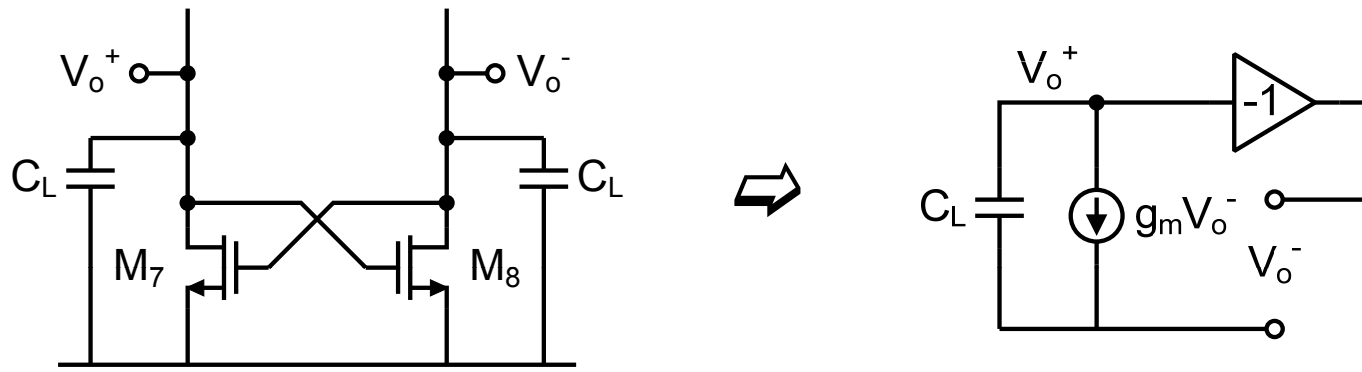

V_{os} derives from:

- Preamp diff. pair mismatch (V_{th},W,L)

- PMOS loads and current mirror

- Latch mismatch

- CI / CF imbalance of M_9

- Clock routing

- Parasitics

Latch Regeneration

Exponential regeneration due to positive feedback of M_7 and M_8
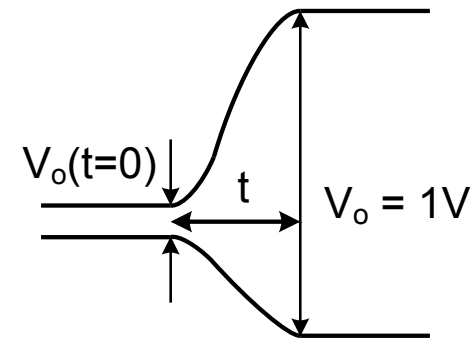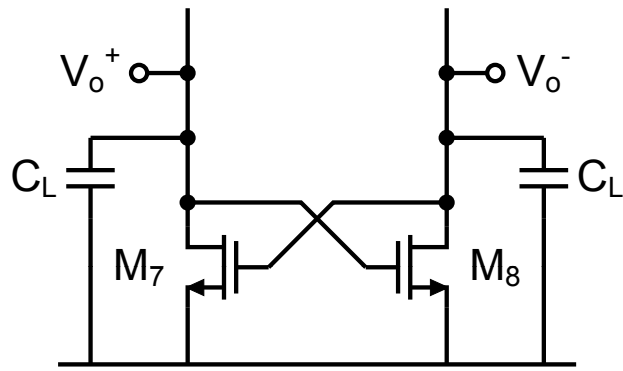
Reg. Speed – Linear Model

$$\begin{cases} V_o^+ = -V_o^- \\ V_o^+ = -g_m \cdot V_o^- / sC_L \end{cases} \Rightarrow \begin{pmatrix} 1 & 1 \\ 1 & g_m/sC_L \end{pmatrix} \begin{pmatrix} V_o^+ \\ V_o^- \end{pmatrix} = 0$$

$$\Delta(s) = g_m/sC_L - 1 = 0 \quad \Rightarrow \quad s_p = g_m/C_L, \quad \text{single RHP pole,}$$

$$\boxed{V_o(t>0) = V_o(t=0) \cdot \exp(t \cdot g_m/C_L).}$$

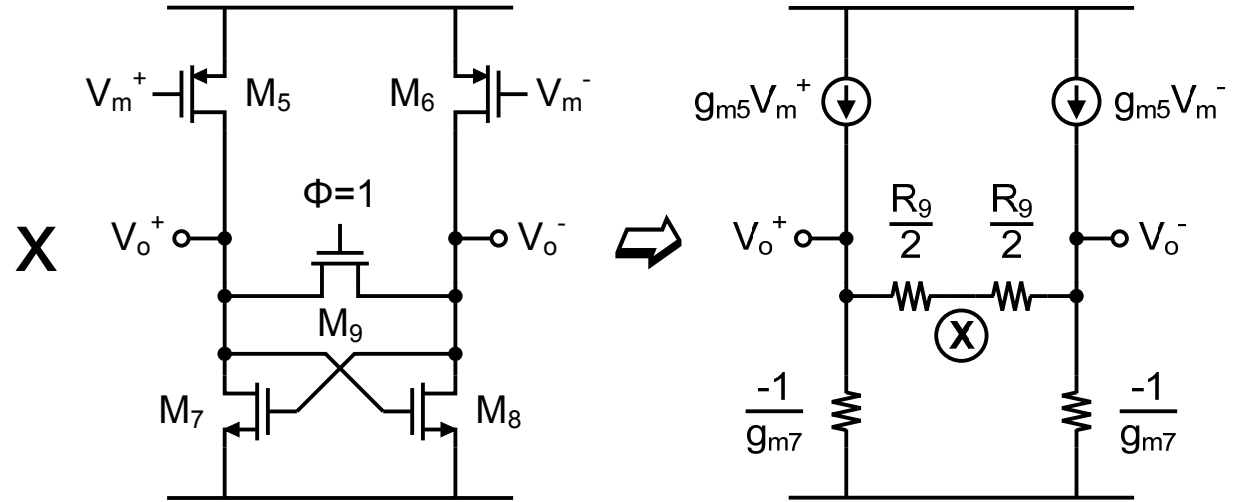# Reg. Speed – Linear Model

V_o	$V_o(t=0)$	$t/(C_L/g_m)$
1V	100mV	2.3
1V	10mV	4.6
1V	1mV	6.9
1V	100µV	9.2

$$t = \frac{C_L}{g_m} \cdot \ln\left[\frac{V_o(t)}{V_o(t=0)}\right]$$

Reg. Speed – Linear Model
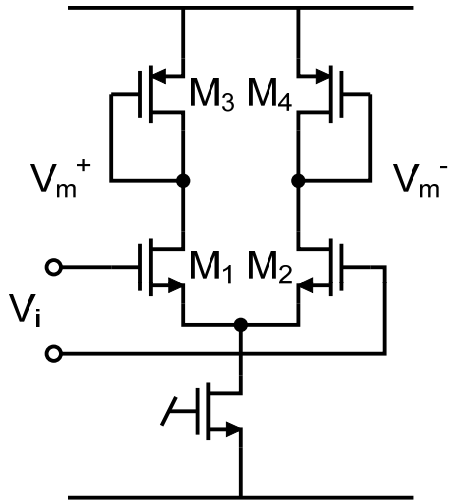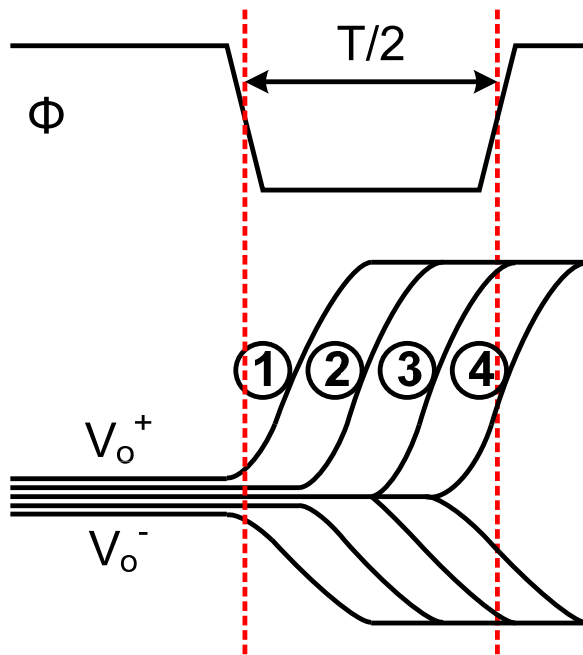
$$\left|A_{V1}\right| = \frac{g_{m1}}{g_{m3}}$$

$$\left|\mathbf{A}_{\mathbf{V2}}\right| = \frac{\mathbf{g}_{\mathbf{m5}}\mathbf{R}_{\mathbf{9}}}{\mathbf{2} - \mathbf{g}_{\mathbf{m7}}\mathbf{R}_{\mathbf{9}}}, \quad \mathbf{g}_{\mathbf{m7}}\mathbf{R}_{\mathbf{9}} < 2 \text{ for positive gain.}$$

$$\mathbf{V}_{\mathbf{o}}(\mathbf{0}) = \mathbf{V}_{\mathbf{i}}(\mathbf{0}) \cdot \mathbf{A}_{\mathbf{V}} = \mathbf{V}_{\mathbf{i}}(\mathbf{0}) \cdot \mathbf{A}_{\mathbf{V1}}\mathbf{A}_{\mathbf{V2}}$$

$$\boxed{V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp\left(t \cdot g_m / C_L\right)}$$

Comparator Metastability

$$V_o(t) = V_i(0) \cdot A_{V1} A_{V2} \cdot \exp\left(t \cdot g_m / C_L\right)$$

Curve	$A_{V1}A_{V2}$	$V_i(t=0)$
①	10	10mV
②	10	1mV
③	10	100μV
④	10	10μV

Comparator fails to produce valid logic outputs within T/2 when input falls into a region that is sufficiently close to the comparator threshold.
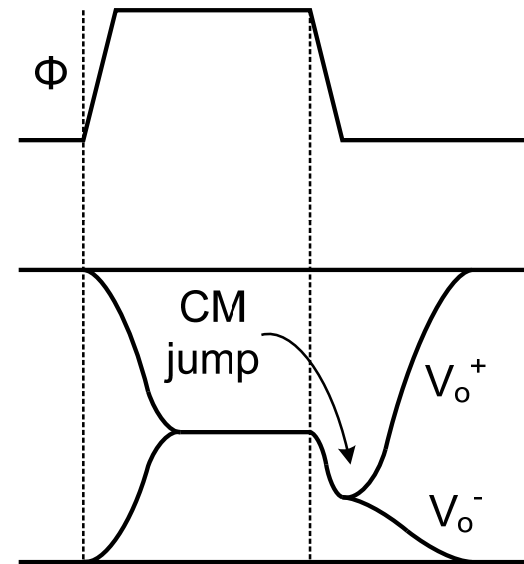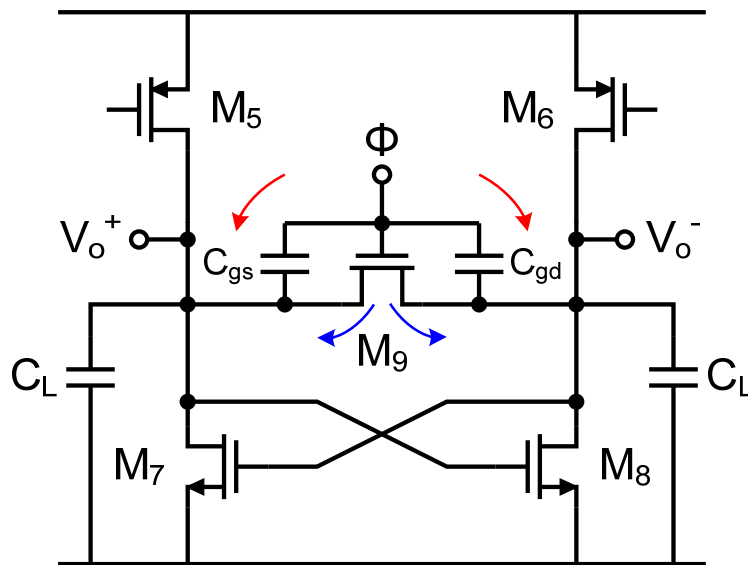
Metastability
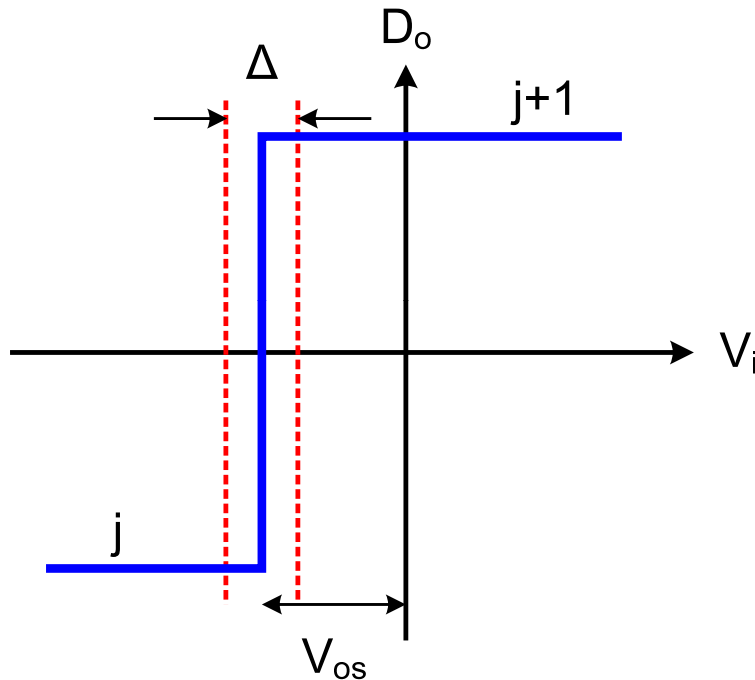
$$BER = \frac{\Delta}{1LSB}$$

$$V_o(t) = V_i(0) \cdot A_{V1} A_{V2} \cdot \exp(t \cdot g_m / C_L)$$

- Cascade preamp stages (typical flash comparator has 2-3 PA stages).

- Use pipelined multi-stage latches; PA can be pipelined too.

- Avoid branching off the comparator logic output.

CI and CF in Latches

- Charge injection and clock feedthrough introduce CM jump in V_o^+ and V_o^-.

- Dynamic latches are more susceptible to CI and CF errors.
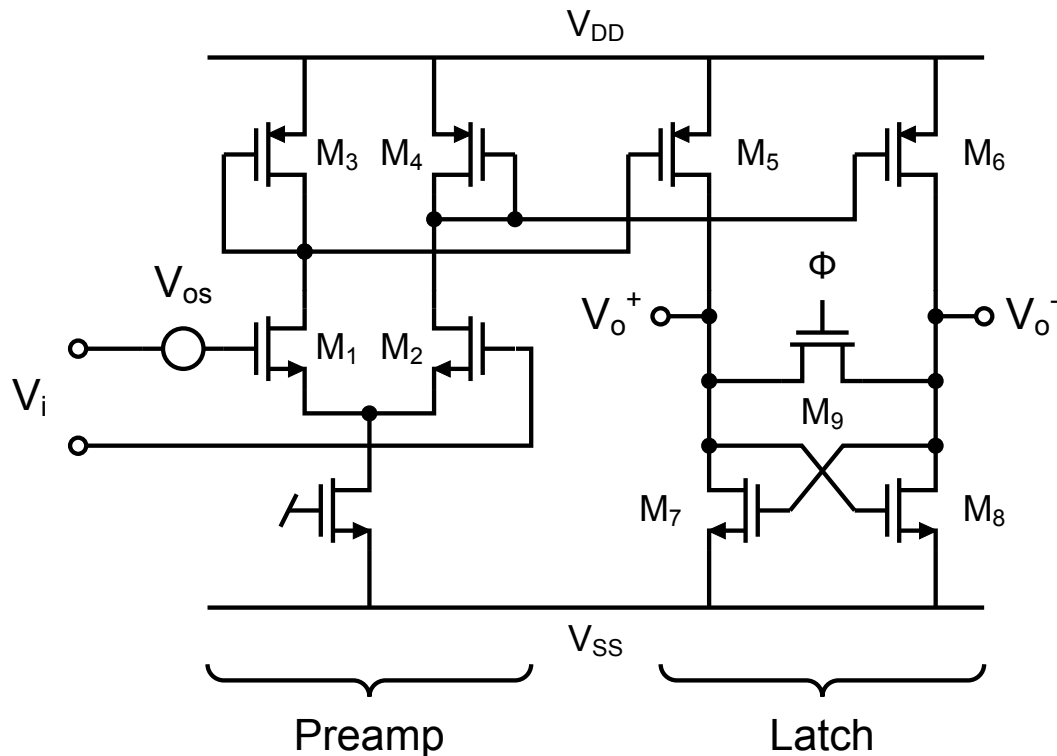
Dynamic Offset of Latches
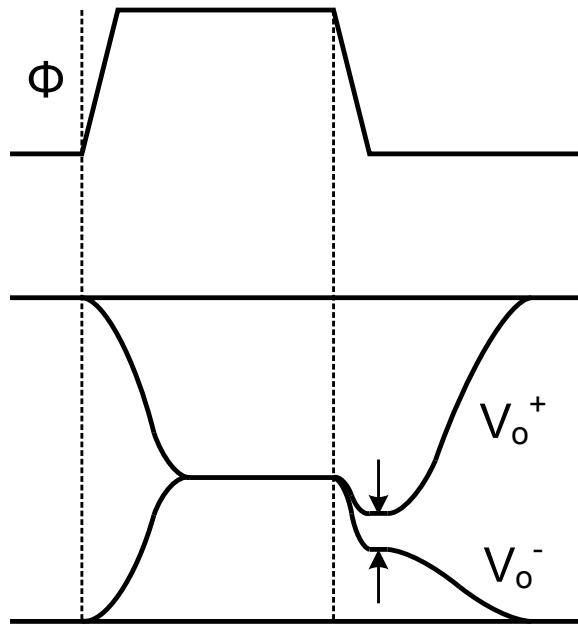
Dynamic offset derives from:

- Imbalanced CI and CF

- Imbalanced load capacitance

- Mismatch b/t M_7 and M_8

- Mismatch b/t M_5 and M_6

- Clock routing

0.5V CM jump

10% imbalance $\Big\}$ $\Rightarrow$ 50mV offset

Dynamic offset is usually the dominant offset in latches.
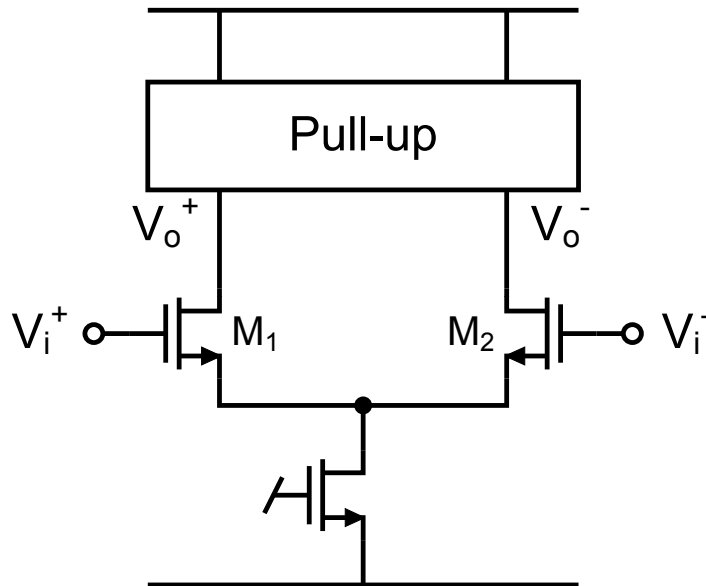
Typical CMOS Comparator

- Input-referred latch offset gets divided by the gain of PA.

- Preamp introduces its own offset (mostly static due to V_{th}, W, and L mismatches).

- PA also reduces kickback noise.

Kickback noise disturbs the reference voltages, must settle before next T.

CMOS Preamplifier

Pull-Up

- NMOS diode pull $-$ up :

$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{(W/L)_1}{(W/L)_L}}$$
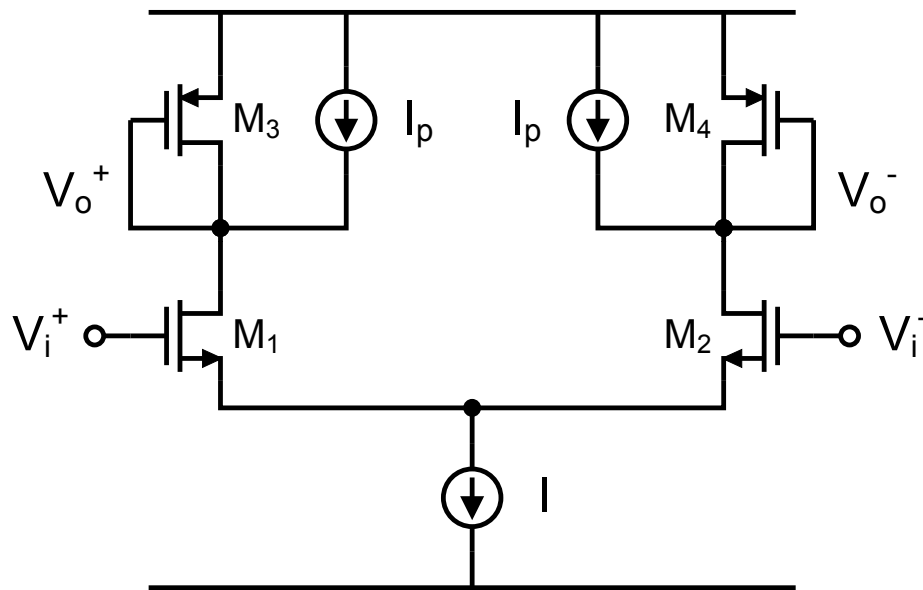
- PMOS diode pull $-$ up :

$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{\mu_n}{\mu_p}\frac{(W/L)_1}{(W/L)_L}}$$

- Resistor pull $-$ up :

$$A_V = -g_{m1} \cdot R_L$$

- NMOS pull-up suffers from body effect, affecting gain setting accuracy.

- PMOS pull-up has no body effect, but is subject to P/N matching.

- Gain accuracy is the worst for resistive pull-up as resistors (poly, diffusion, well, and etc.) don't track transistors.
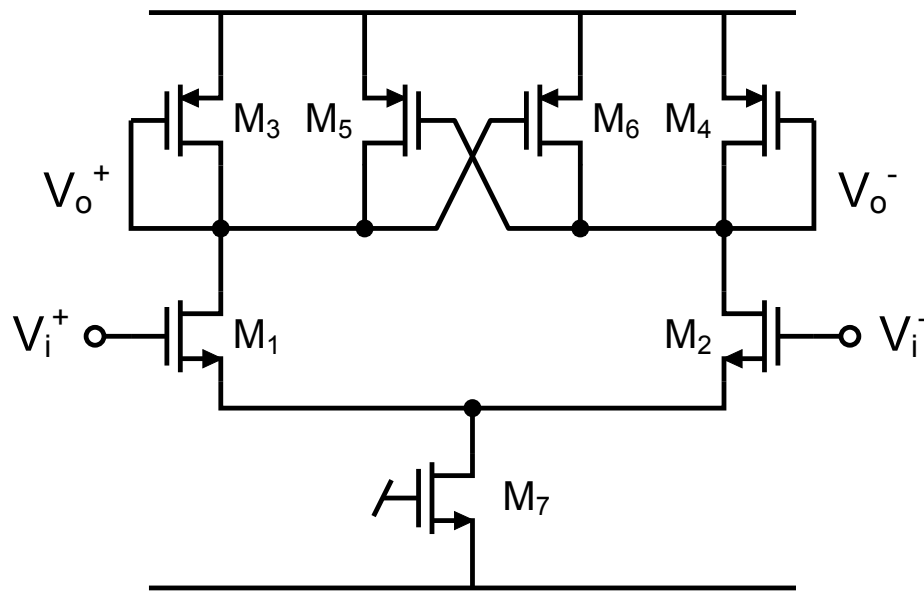
To Obtain More Gain

- I_p diverts current away from PMOS diodes (M_3 & M_4), reducing $(W/L)_3$.

- Higher gain, no CMFB

- Needs biasing for I_p

- M_3 & M_4 may cut off for large V_{in}, resulting in long recovery time.

$$A_V = -\frac{g_{m1}}{g_{m3}} \approx -\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{I/2}{I/2-I_p}\right)\frac{(W/L)_1}{(W/L)_3}}$$
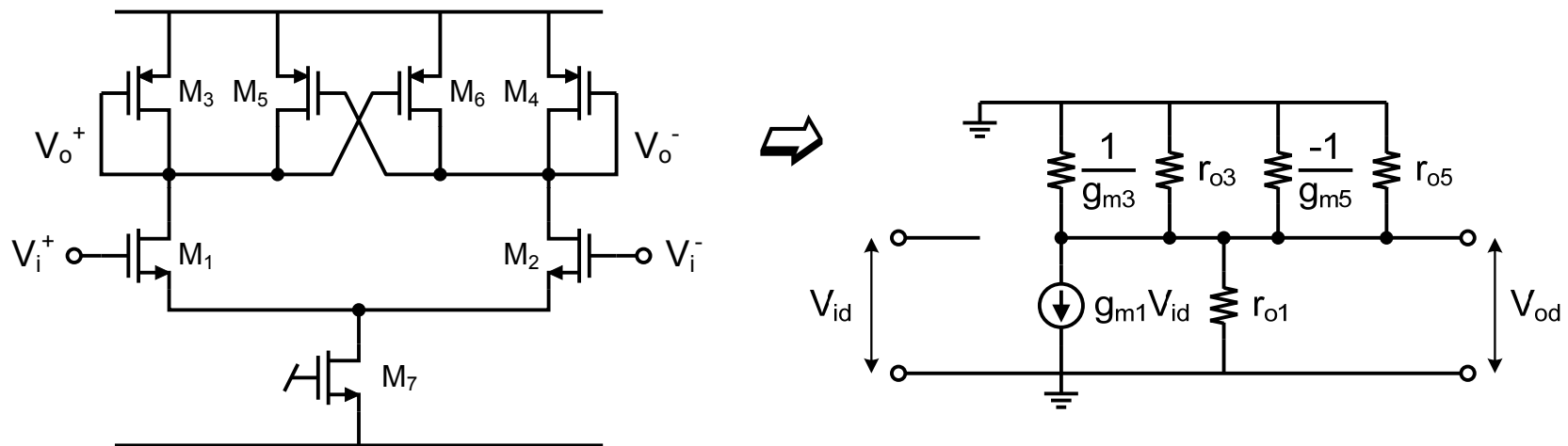
Bult's Preamp

- NMOS diff. pair loaded with PMOS diodes and PFB PMOS pair

- High DM gain, low CM gain, good CMRR

- Simple, no CMFB

- $(W/L)_{34} > (W/L)_{56}$ needs to be ensured for stability.
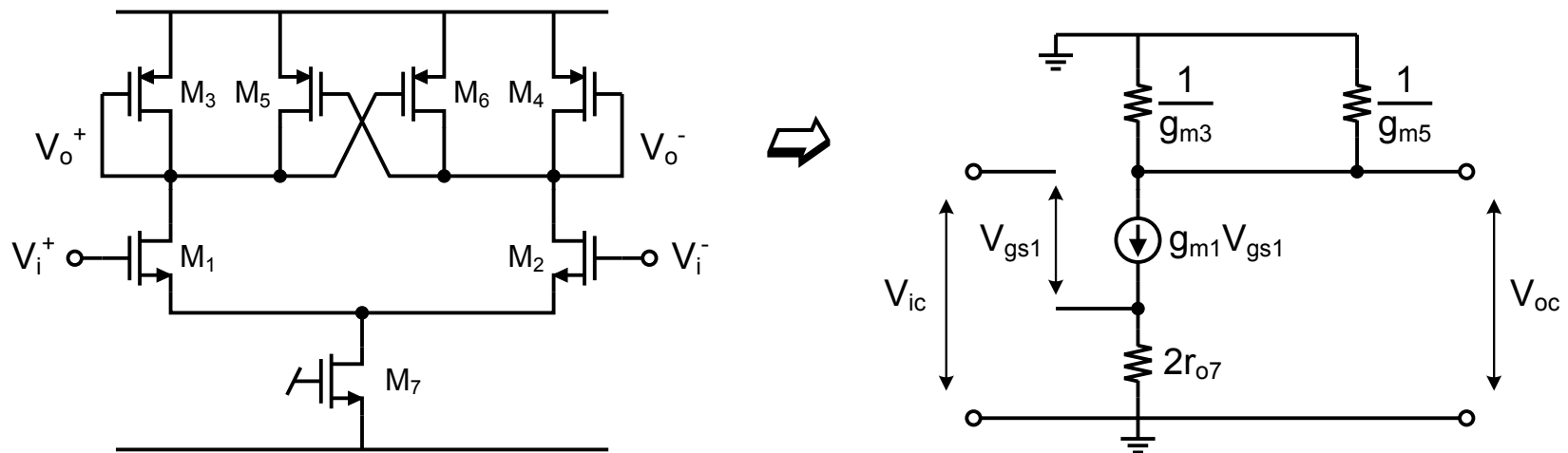
Ref: K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1887-1895, issue 12, 1997.
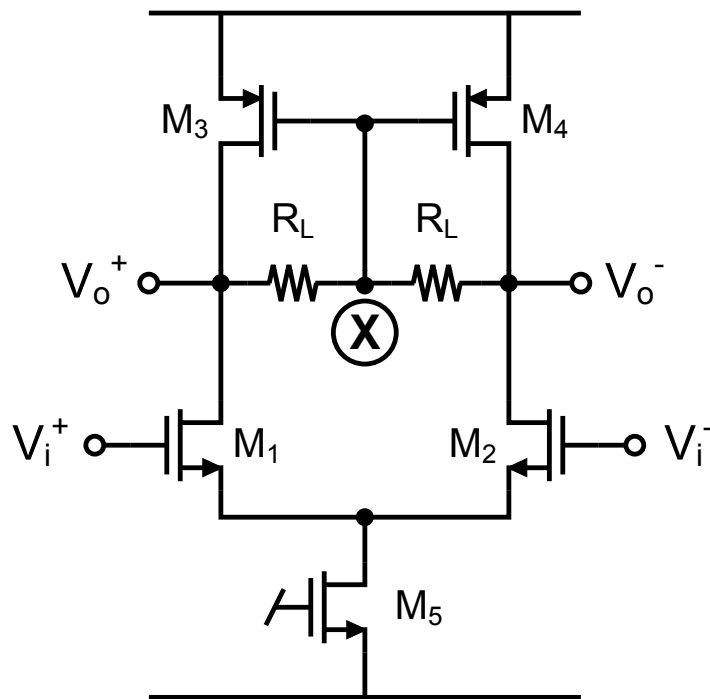
Bult's Preamp (DM)

DM gain: $A_V^{dm} = -g_{m1} \cdot \left[\dfrac{1}{g_{m3}} // \left(-\dfrac{1}{g_{m5}} \right) // r_{o1} // r_{o3} // r_{o5} \right] \approx -\dfrac{g_{m1} r_{o1}}{3}$

Bult's Preamp (CM)

CM gain:
$$A_V^{cm} = -\frac{g_{m1}}{1 + 2g_{m1}r_{o7}} \cdot \left(\frac{1}{g_{m3}} // \frac{1}{g_{m5}}\right) \approx -\frac{1}{2(g_{m3} + g_{m5})r_{o7}}$$
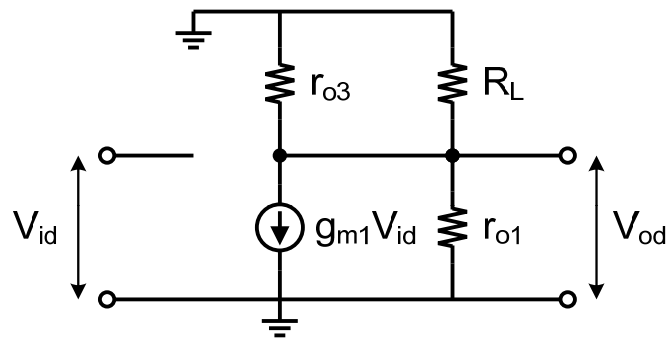
Song's Preamp

- NMOS diff. pair loaded with PMOS diodes and a pair of resistors
- High DM gain, low CM gain, good CMRR
- Simple, no CMFB
- Gain depends on precision of R_L

Ref: B.-S. Song et al., "A 1 V 6 b 50 MHz current- interpolating CMOS ADC," in *Symposium on VLSI Circuits Digest of Technical Papers*, 1999, pp. 79-80.
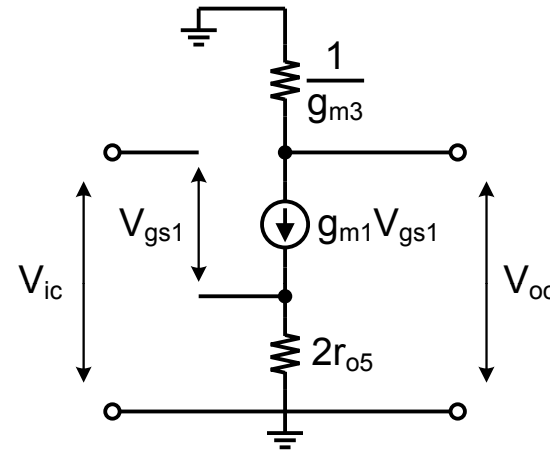
Song's Preamp (CM)

DM

CM

$$A_V{}^{dm} = -g_{m1} \cdot \left(r_{o1} \,//\, r_{o3} \,//\, R_L\right)$$
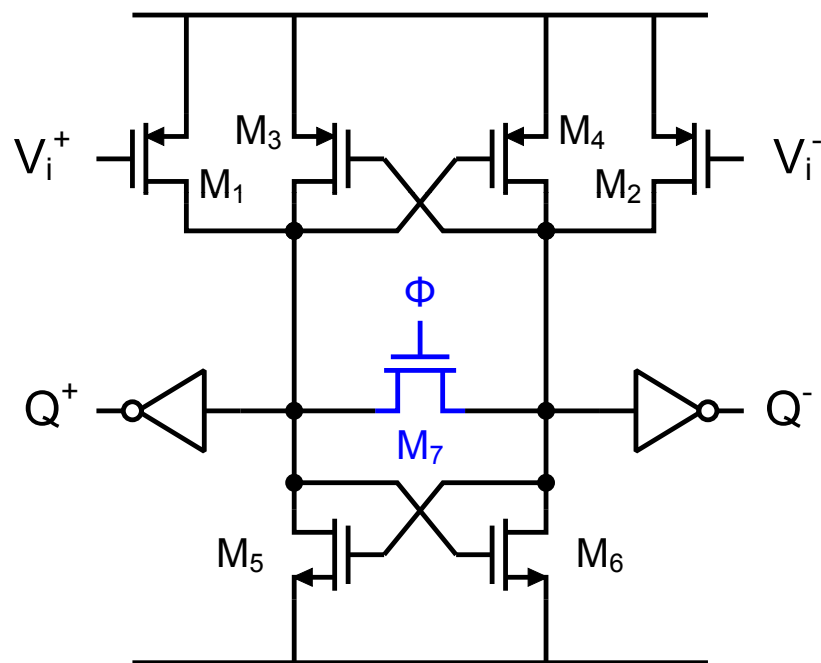$$\approx -g_{m1} R_L$$

$$A_V{}^{cm} = -\frac{g_{m1}}{1 + 2g_{m1}r_{o5}} \cdot \frac{1}{g_{m3}}$$
$$\approx -\frac{1}{2g_{m3}r_{o5}}$$

CMOS Latch
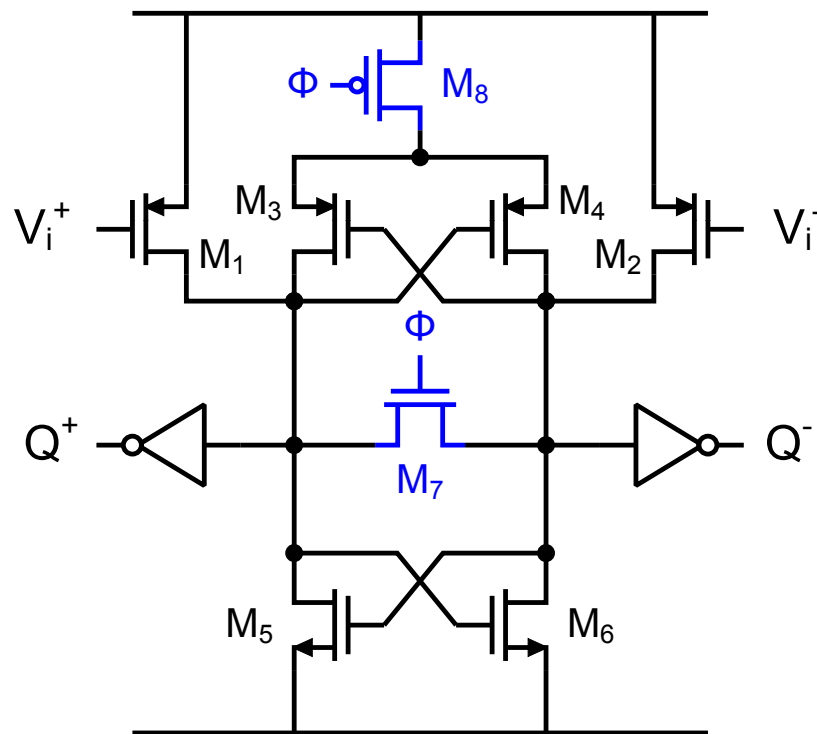
# Static Latch

- Active pull-up and pull-down → full CMOS logic levels
- Very fast!
- Q^+ and Q^- are not well defined in reset mode ($\Phi = 1$).
- Large short-circuit current in reset mode.
- Zero DC current after full regeneration
- Very noisy

# Semi-Dynamic Latch

- Diode divider disabled in reset mode → less short-circuit current

- Pull-up not as fast

- Q^+ and Q^- are still not well defined in reset mode ($\Phi = 1$).

- Zero DC current after full regeneration

- Still very noisy

Current-Steering Latch
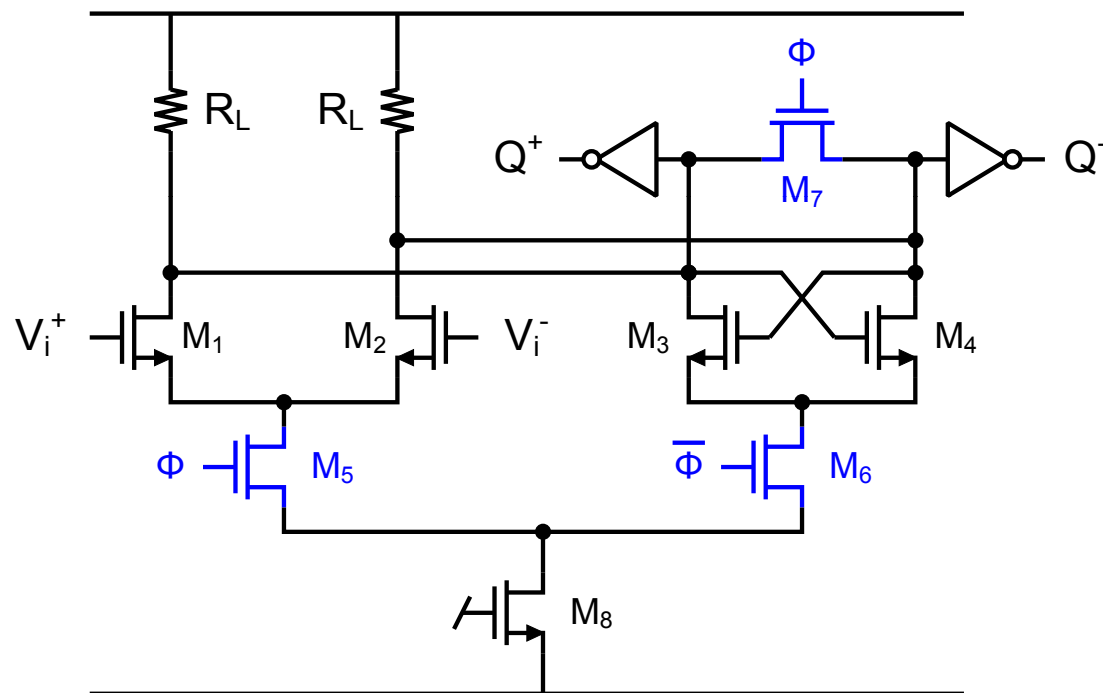
- Constant current → very quite

- Higher gain in tracking mode

- Cannot produce full logic levels

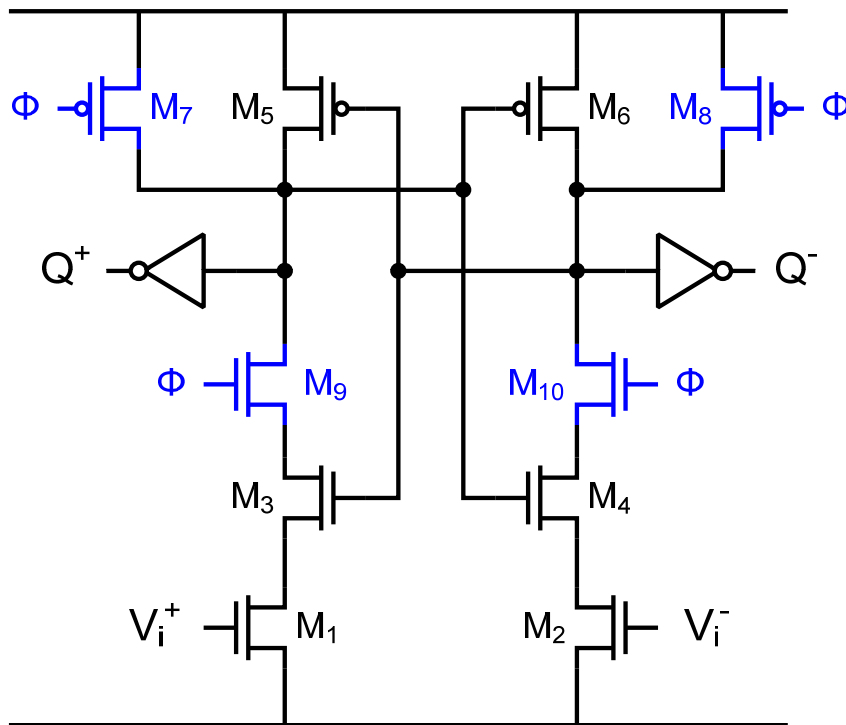- Fast

- Trip point of the inverters

Dynamic Latch
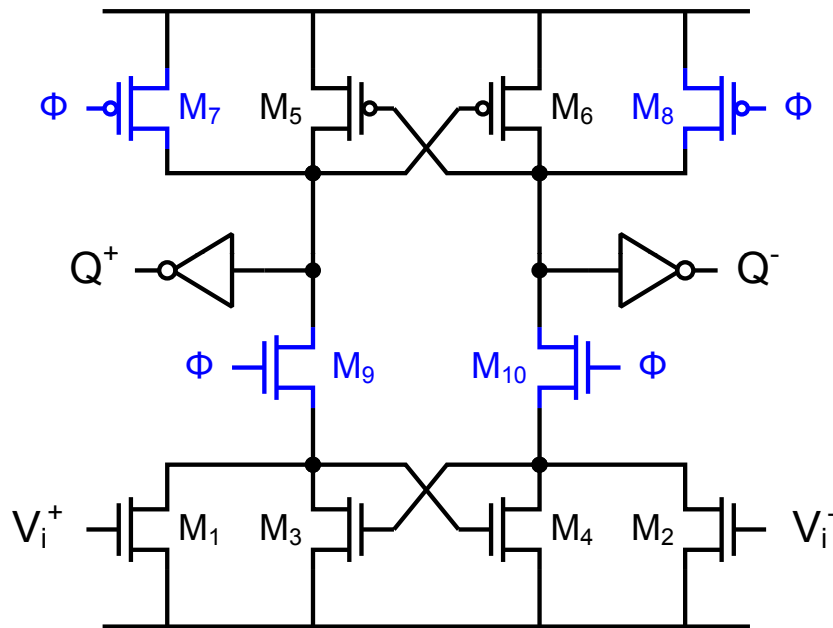
- Zero DC current in reset mode

- Q^+ and Q^- are both precharged to "0".

- Full logic level after regeneration stability.

- Slow

Ref: A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," *IEEE Journal of Solid-State Circuits*, vol. 20, pp. 775-779, issue 3, 1985.
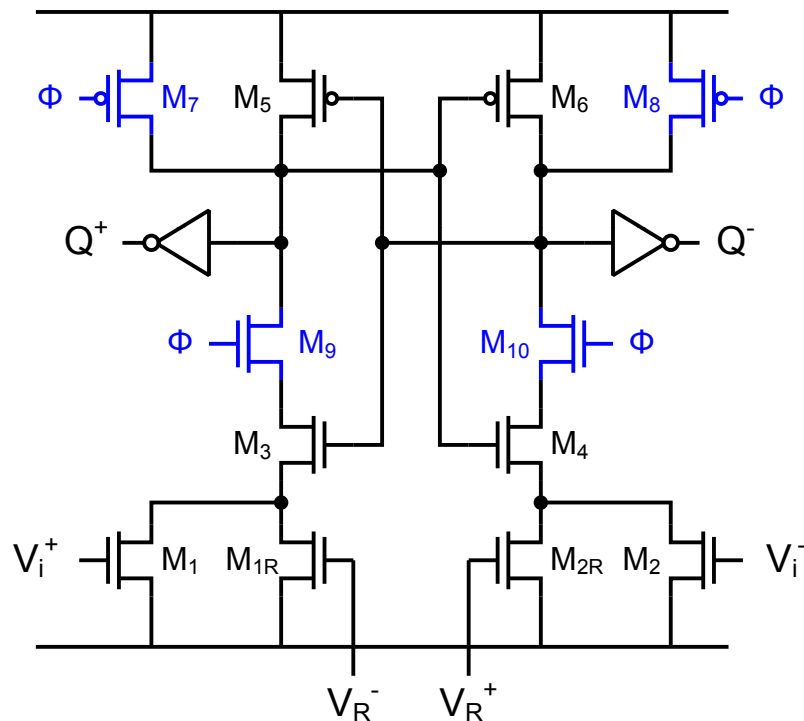
Modified Dynamic Latch

- Zero DC current in reset mode
- Q^+ and Q^- are both precharged to "0".
- Full logic level after regeneration stability.
- Slow

Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 166-172, issue 3, 1995.

Cho's Comparator

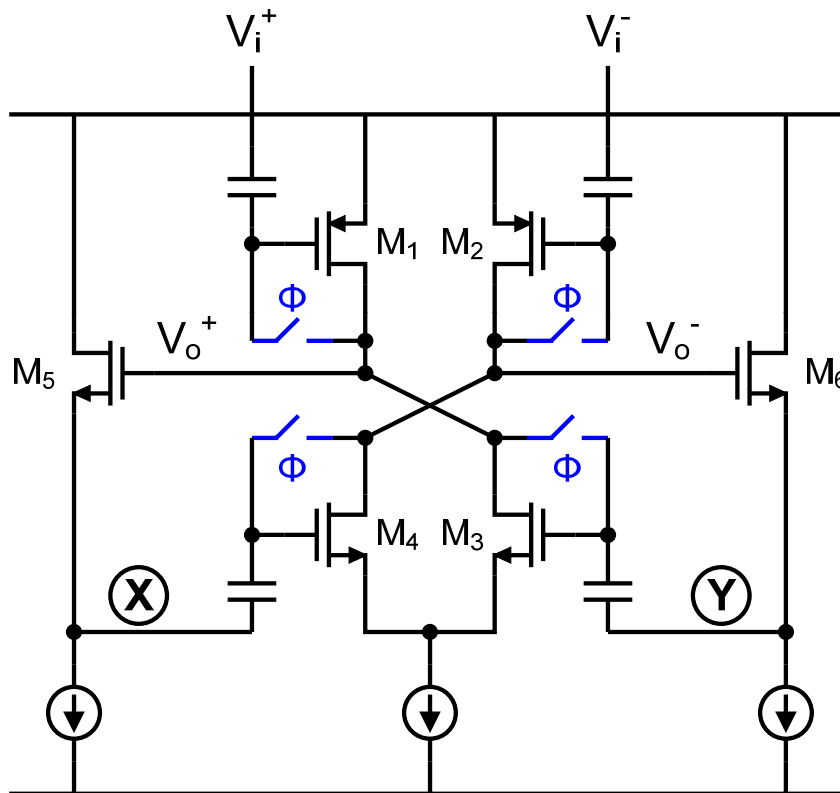$$G_1 = k'\left[\frac{W_i}{L}\left(V_i^+ - V_{th}\right) + \frac{W_R}{L}\left(V_R^- - V_{th}\right)\right]$$

$$G_2 = k'\left[\frac{W_i}{L}\left(V_i^- - V_{th}\right) + \frac{W_R}{L}\left(V_R^+ - V_{th}\right)\right]$$

$$\text{Threshold} = \frac{W_R}{W_i}\cdot\left(V_R^+ - V_R^-\right)$$

M_{1R} and M_{2R} added to set the decision threshold
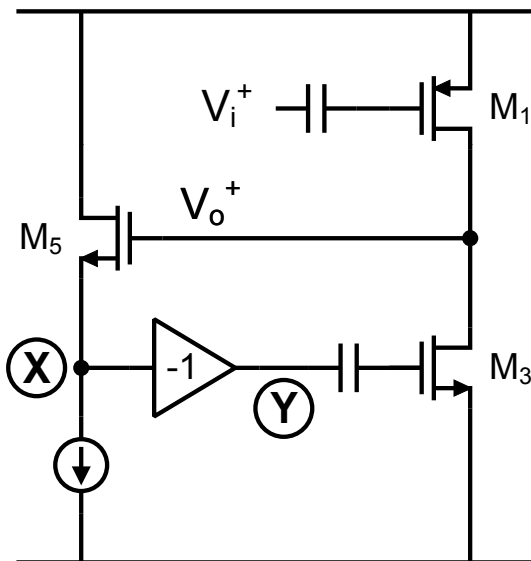
Regenerative Sense Amplifier (RSA)

- Offset cancellation
- Fast
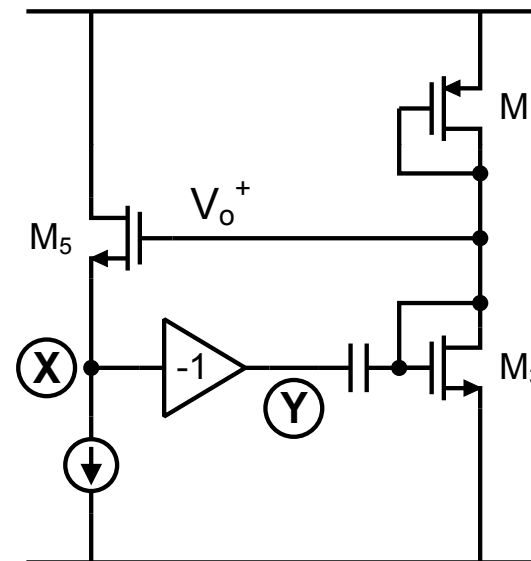- AC coupling reduces signal gain.
- CM feedback?

Ref: J.-T. Wu and B. A. Wooley, "A 100-MHz pipelined CMOS comparator," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 1379-1385, issue 6, 1988.
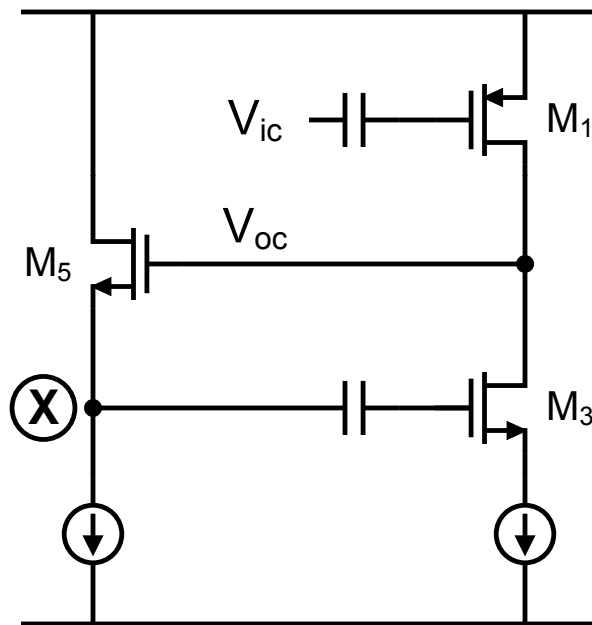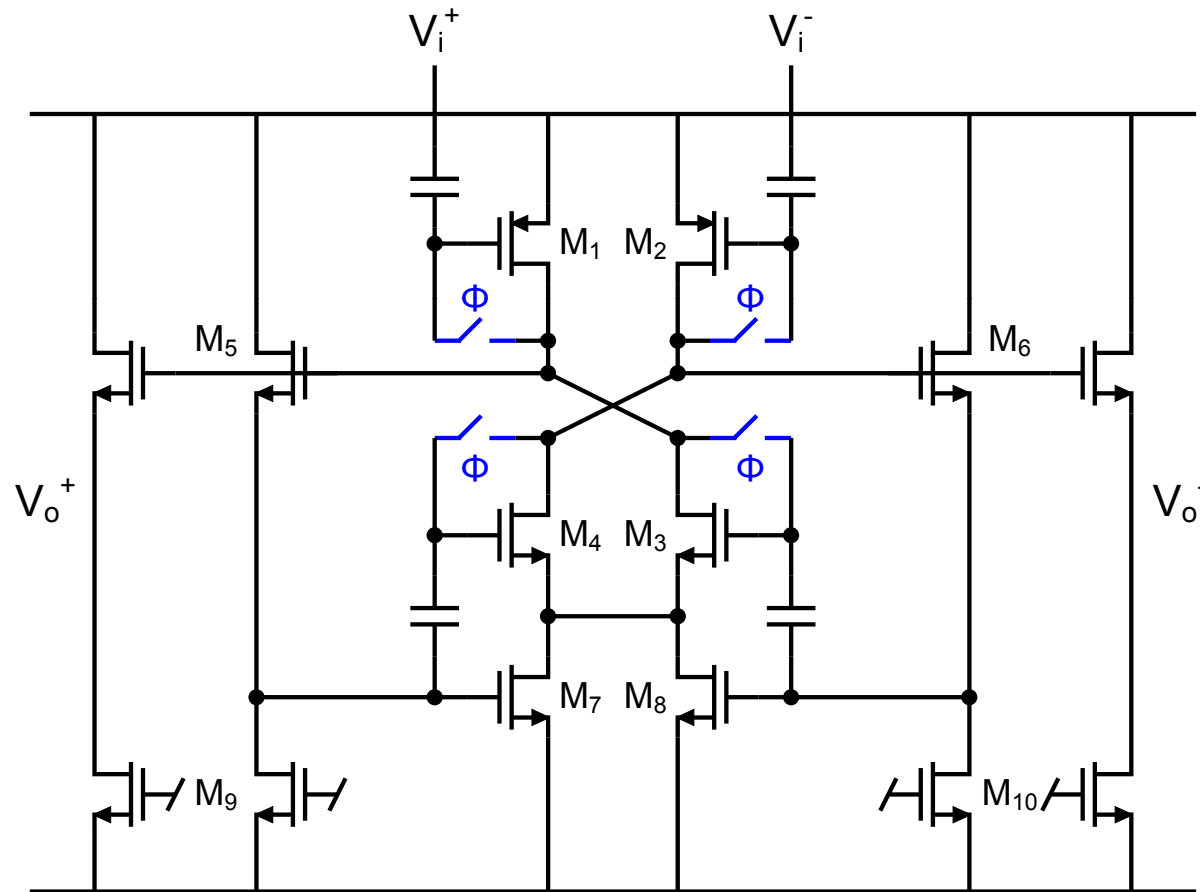
DM Equivalent Circuit

Sensing

Resetting

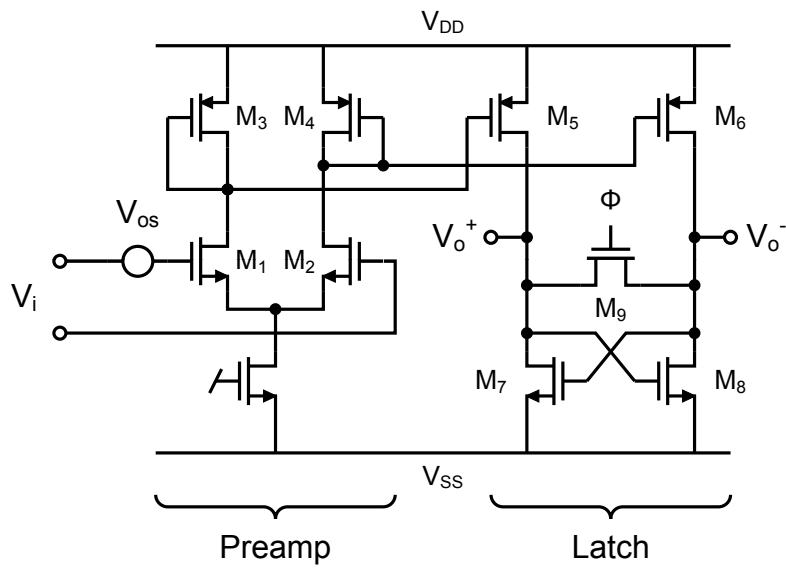DM loopgain in resetting mode is less than 1.

CM Equivalent Circuit

- M3 degenerated
- Loopgain < 1 ?
- Needs CMFB

RSA Common-Mode Feedback

S. Hoyos-ELEN-610

Comparator Offset

Differential pair mismatch:

$$V_{os}^{\;2} = \left(\Delta V_{th}\right)^2 + \frac{1}{4}V_{ov}^{\;2}\left[\left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta L}{L}\right)^2\right]$$

$$\left|A_{V1}\right| = \frac{g_{m1}}{g_{m3}} \qquad \left|A_{V2}\right| = \frac{g_{m5}R_9}{2 - g_{m7}R_9}$$

<u>Total input-referred comparator offset:</u>

$$V_{os}^{\;2} = V_{os,12}^{\;\;2} + \frac{V_{os,34}^{\;\;2} + V_{os,56}^{\;\;2}}{A_{V1}^{\;2}} + \frac{V_{os,78}^{\;\;2}}{A_{V1}^{\;2}A_{V2}^{\;2}} + \frac{V_{os,dyn}^{\;\;2}}{A_{V1}^{\;2}A_{V2}^{\;2}}$$

Matching Properties

The variance of parameter ΔP b/t two rectangular devices:

$$\sigma^2(\Delta P) = \frac{A_P{}^2}{WL} + S_P{}^2 D^2,$$
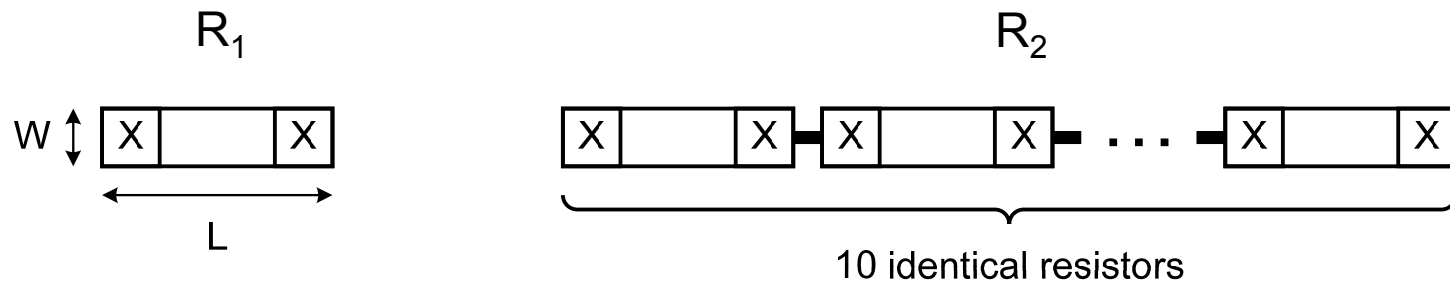
1st term dominates for small devices.

where, W and L are the effective width and length, D is distance.

Threshold: $\sigma^2(V_{T0}) = \dfrac{A_{VT0}{}^2}{WL} + S_{VT0}{}^2 D^2,$

Current factor: $\dfrac{\sigma^2(\beta)}{\beta^2} = \dfrac{A_\beta{}^2}{WL} + S_\beta{}^2 D^2.$

Ref: M. J. M. Pelgrom, et al., "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 1433-1439, issue 5, 1989.

Why Large Devices Match Better?

$$R_1 = R_S \cdot \frac{L}{W}, \text{ with std } \sigma_{R1}.$$

$$R_2 = R_S \cdot 10\left(\frac{L}{W}\right) = 10R_1, \text{ with std } \sigma_{R2},$$

$$\sigma_{R2}^2 = \sum_{j=1}^{10} \sigma_{R_j}^2 = 10\sigma_{R1}^2 \Rightarrow \sigma_{R2} = \sqrt{10}\sigma_{R1}.$$

$$\frac{\sigma_{R2}}{R_2} = \frac{\sqrt{10}\sigma_{R1}}{10R_1} = \frac{1}{\sqrt{10}}\left(\frac{\sigma_{R1}}{R_1}\right) \Rightarrow \frac{\sigma_R}{R} \propto \frac{1}{\sqrt{A}} = \frac{1}{\sqrt{WL}}.$$

"Spatial averaging"

ADC Input Capacitance

$$\sigma^2(V_{T0}) = \frac{A_{VT0}^2}{WL} \qquad C_g = 10\,fF/\mu m^2$$

- N = 6 bits $\rightarrow$ 63 comparators
- V_{FS} = 1V $\rightarrow$ 1 LSB = 16mV
- σ = LSB/4 $\rightarrow$ σ = 4mV
- A_{VT0} = 10mV·μm $\rightarrow$ L = 0.24μm, W = 26μm

N (bits)	# of comp.	C_{in} (pF)
6	63	3.9
8	255	250
10	1023	??!

- Small V_{os} leads to large device sizes, hence large area and power.
- Large comparator leads to large input capacitance, difficult to drive and difficult to maintain bandwidth.

Multi-Stage Preamp
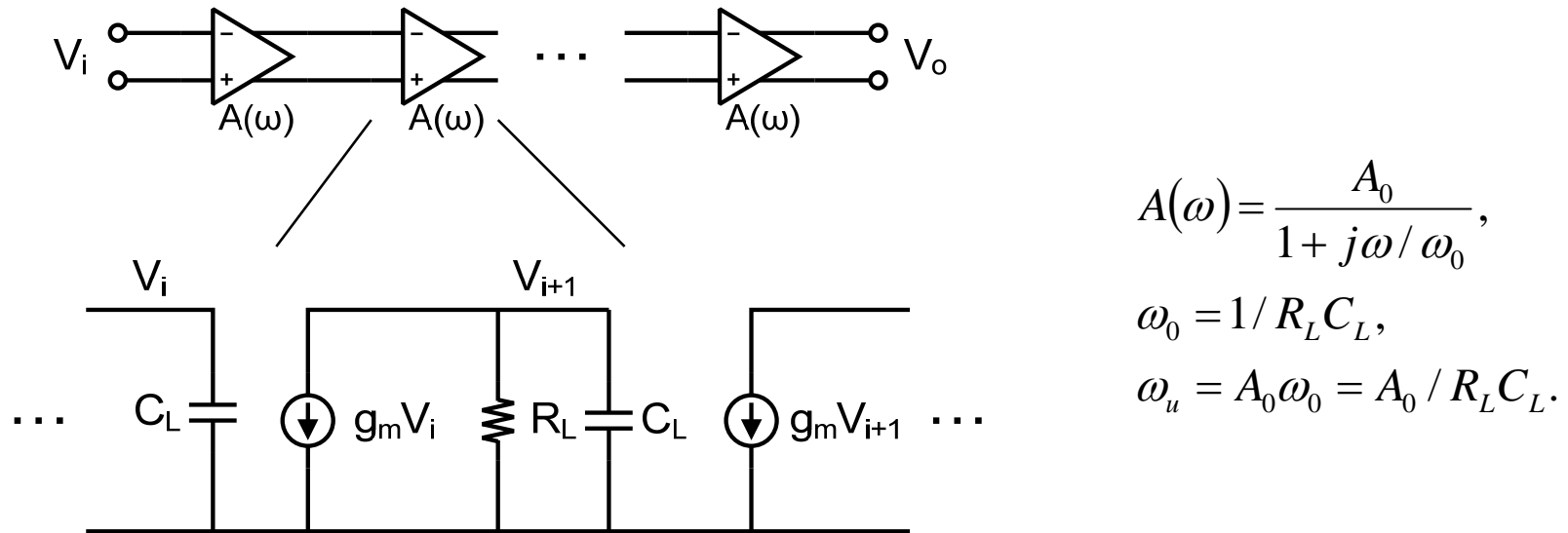
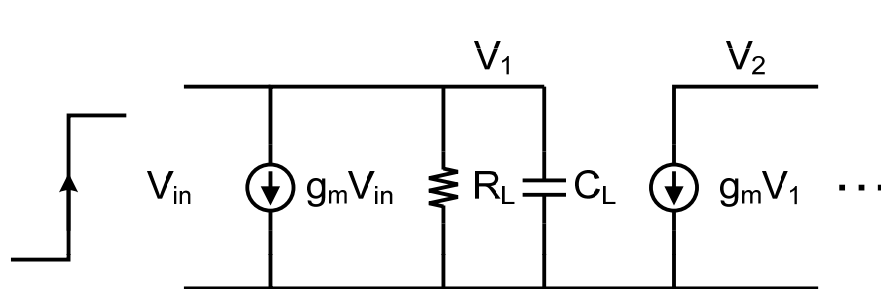$$A(\omega) = \frac{A_0}{1 + j\omega/\omega_0},$$

$$\omega_0 = 1/R_L C_L,$$

$$\omega_u = A_0 \omega_0 = A_0 / R_L C_L.$$

N stages:

$$\left|A_N(\omega)\right| = \left|\left(\frac{A_0}{1 + j\omega/\omega_0}\right)^N\right| = \left(\frac{A_0}{\sqrt{1 + (\omega/\omega_0)^2}}\right)^N,$$

$$\left|A_N(\omega = \omega_{-3dB})\right| = \frac{A_0^{\,N}}{\sqrt{2}}, \quad \omega_{-3dB} = \omega_0 \sqrt{2^{\frac{1}{N}} - 1}.$$
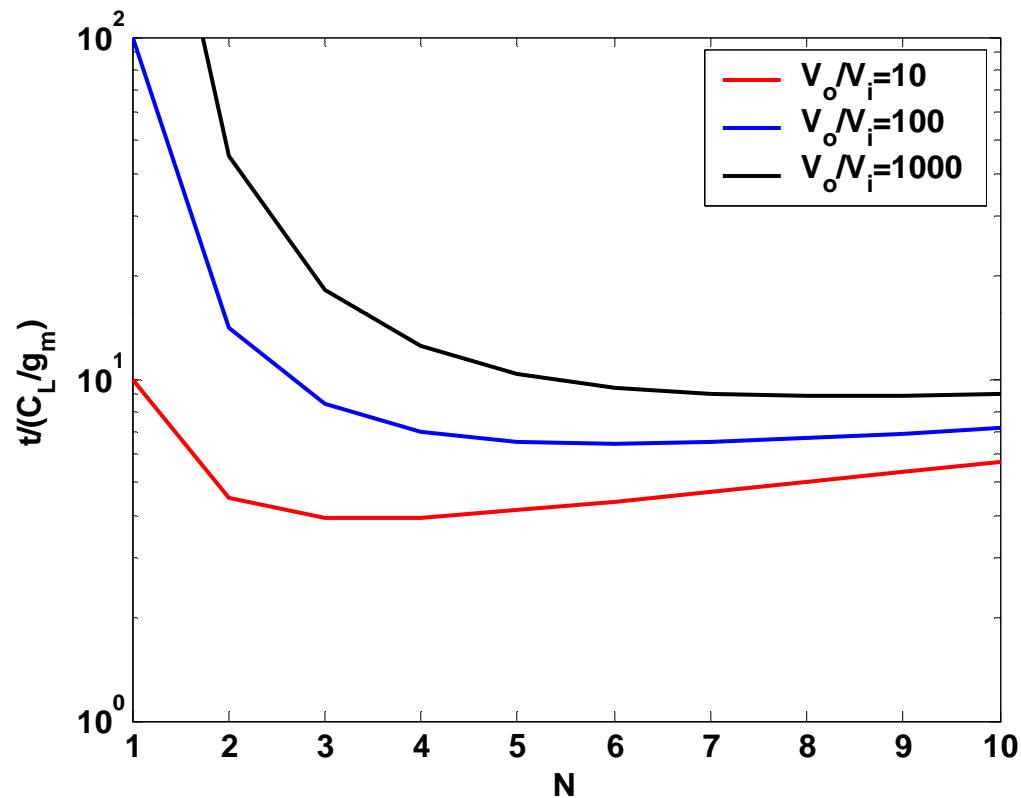
Step Response

$$V_1 = V_{in} \cdot A_0 \left(1 - e^{-t/\tau} \right)$$

$$\approx V_{in} \cdot A_0 (t/\tau), \quad for \ \ t \ll \tau$$

$$= V_{in} \cdot g_m R_L \cdot \frac{t}{R_L C_L}$$

$$= V_{in} \cdot \frac{g_m}{C_L} t$$

Ignore R_L in all stages:

$$V_1 = \frac{1}{C_L} \int_0^t g_m V_{in} dt = \frac{g_m}{C_L} V_{in} \cdot t, \quad V_2 = \frac{1}{C_L} \int_0^t g_m V_1 dt = \frac{1}{2} \left(\frac{g_m}{C_L} \right)^2 V_{in} \cdot t^2,$$

$$for \ smal \ V_N, \quad V_N = \frac{1}{C_L} \int_0^t g_m V_{N-1} dt = \frac{t^N}{N!} \left(\frac{g_m}{C_L} \right)^N V_{in}.$$
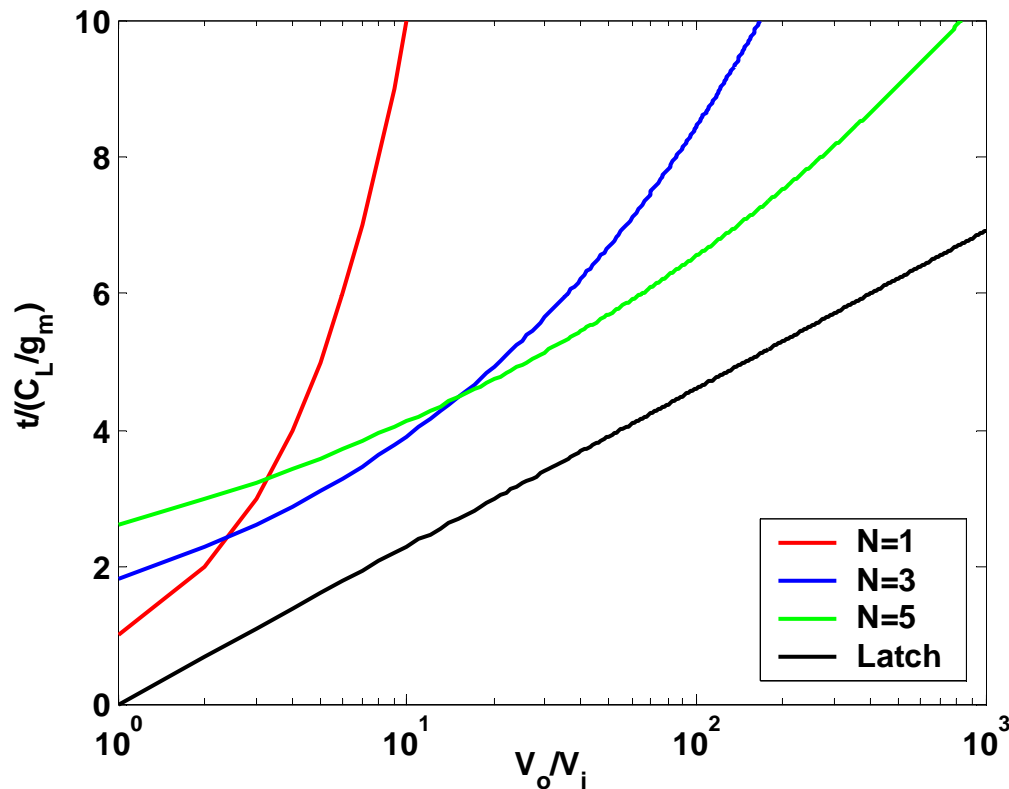
Optimum N

For small V_o,

$$V_o = \frac{t^N}{N!}\left(\frac{g_m}{C_L}\right)^N V_i$$

$$t = \frac{C_L}{g_m} \cdot \left[N!\left(\frac{V_o}{V_i}\right) \right]^{\frac{1}{N}}$$

- Given $A_0 = V_o/V_i$, N_{opt} can be determined with the above equation.
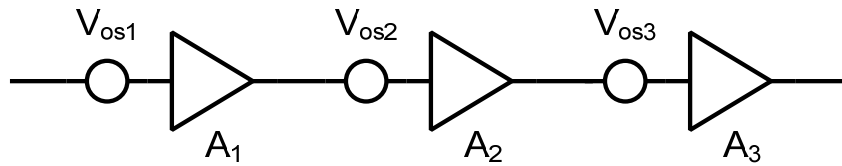- For $A_0 < 100$, typical N value ranges between 2 and 4.

Comparison

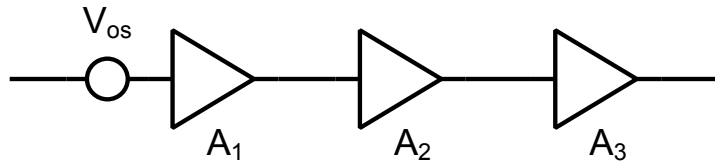$$t = \frac{C_L}{g_m} \cdot \left[N! \left(\frac{V_o}{V_i} \right) \right]^{\frac{1}{N}}$$

$$\text{latch}: \quad t = \frac{C_L}{g_m} \cdot \ln \left(\frac{V_o}{V_i} \right)$$

- A higher A_0 (= V_o/V_i) requires a larger N.

- In comparison, latches regenerate (PFB) faster than preamp.
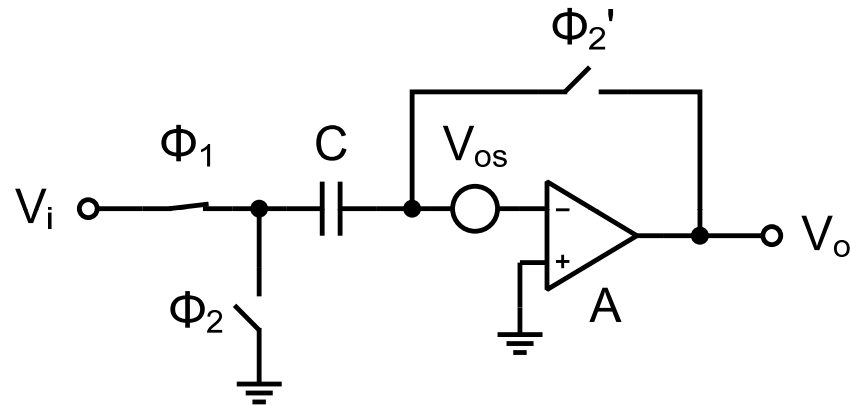
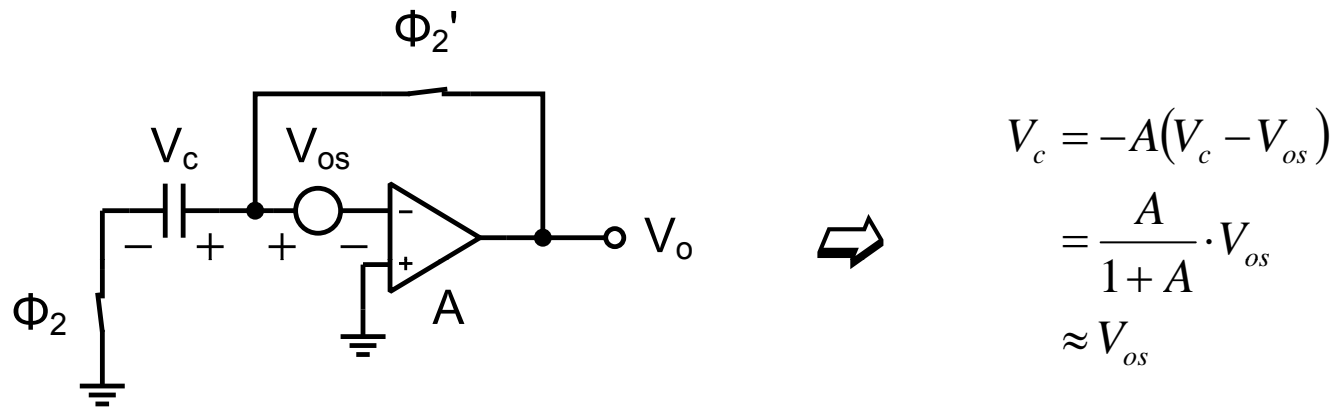# Multi-Stage PA Offset

Individual stage

Total input-referred

$$A_T = A_1 \cdot A_2 \cdot A_3,$$

$$V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}.$$

Input Offset Cancellation

- AC coupling at input with input-referred offset stored in C.

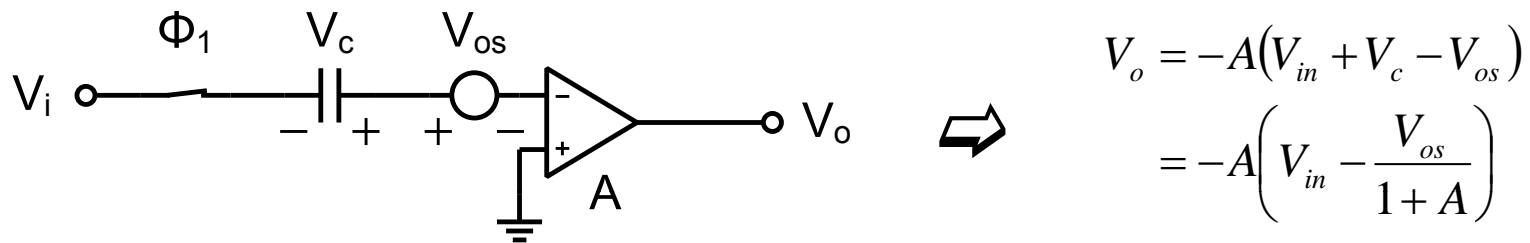- Two-phase operation, one phase (Φ_2) is used to store offset.

Offset Storage – Φ_2

$$V_c = -A(V_c - V_{os})$$

$$= \frac{A}{1+A} \cdot V_{os}$$

$$\approx V_{os}$$

Closed-loop stability (amplifier in unity-gain feedback)

Ref: J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," *IEEE Journal of Solid-State Circuits*, vol. 10, pp. 371-379, issue 6, 1975.
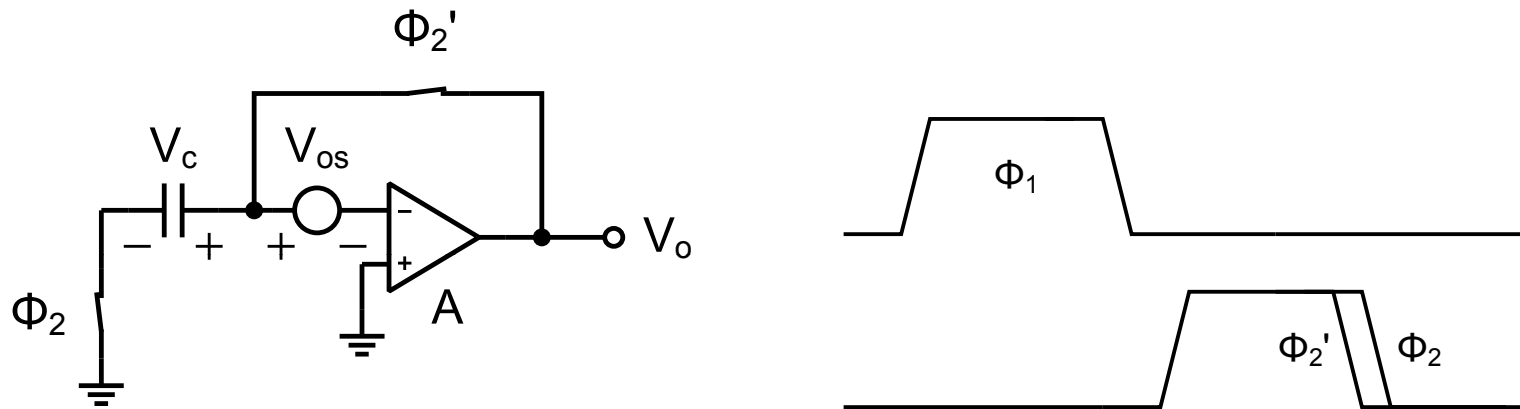
Amplifying Phase – Φ_1

$$V_o = -A(V_{in} + V_c - V_{os})$$

$$= -A\left(V_{in} - \frac{V_{os}}{1+A}\right)$$

$$\boxed{\text{Input} - \text{referred offset} \ = \ \frac{V_{os}}{1+A}}$$
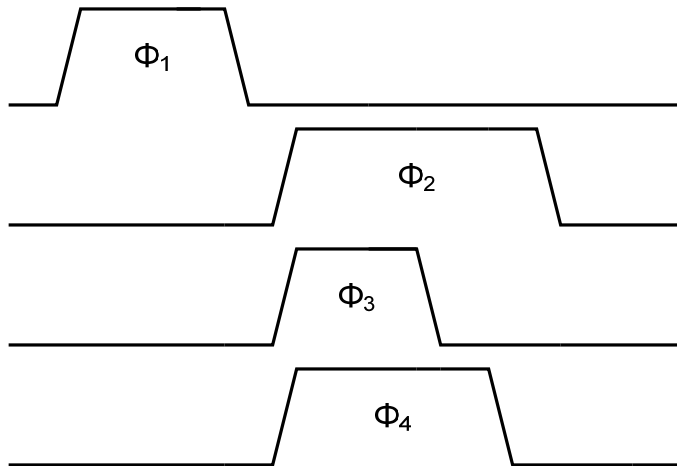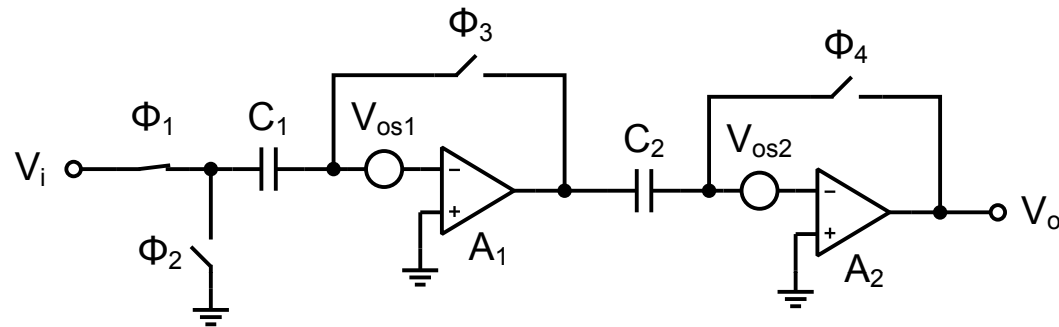
- Offset cancellation is incomplete if A is finite.

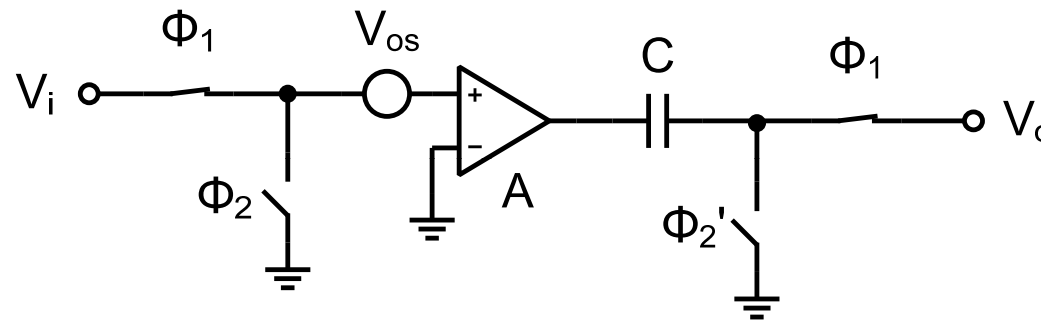- AC coupling at input attenuates signal gain.

CF and CI of Switches

- What's the optimum phase relationship between Φ_2 and Φ_2'?

- Bottom-plate sampling $\rightarrow$ Φ_2' switches off slightly before Φ_2.

Multi-Stage Input Offset Cancellation

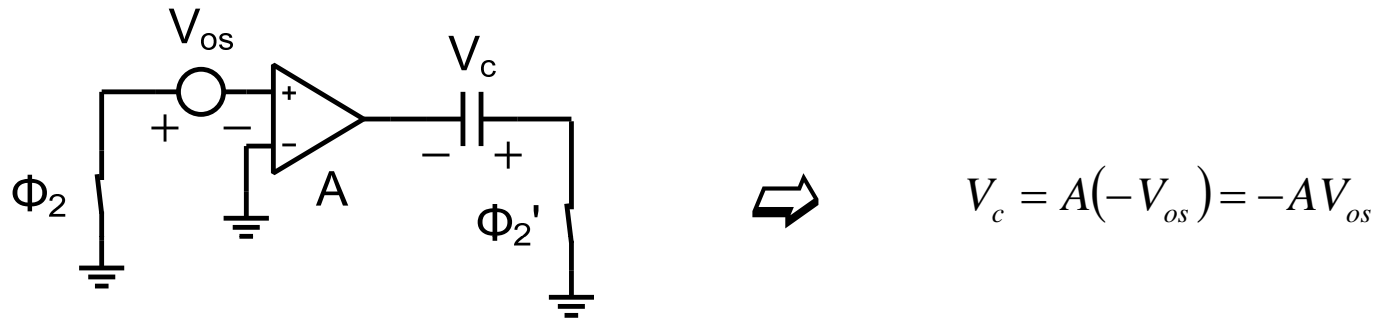- Multi-stage AC coupling

- Φ_3 switches off first
  $\rightarrow \Delta V_1$ on C_1 will be
     absorbed by C_2.

- Φ_4 switches off next, Φ_2
  last.

Output Offset Cancellation

- AC coupling at output with offset stored in C.

- A must be small and well controlled (independent of V_o).
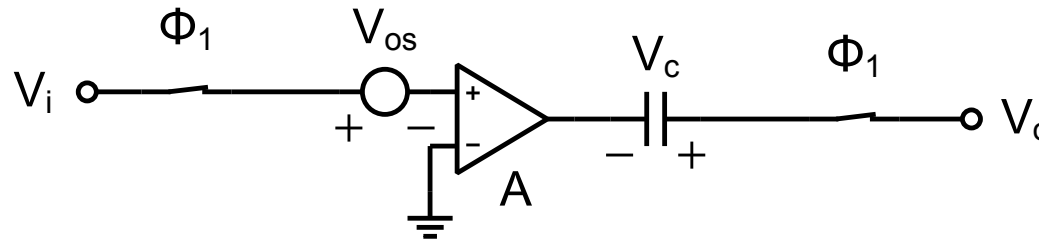
- Does not work for high-gain op-amps.

Offset Storage – Φ_2

$$V_c = A(-V_{os}) = -AV_{os}$$

- Closed-loop stability is not required.
- CF and CI of Φ_2' gets divided by A when referred to input.

Ref: R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier,"
    IEEE Journal of Solid-State Circuits, vol. 13, pp. 499-503, issue 4, 1978.

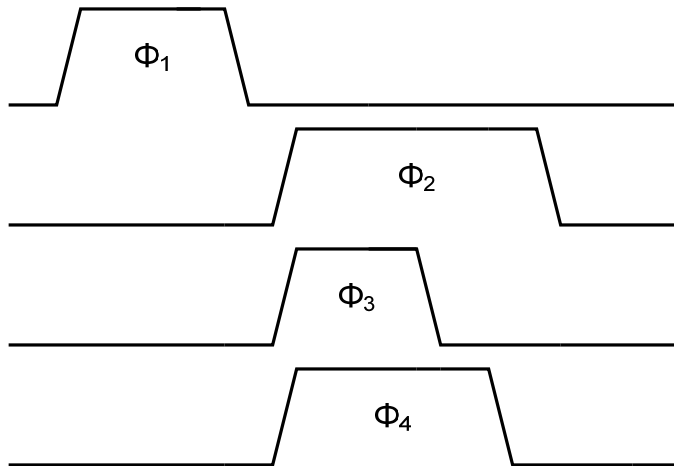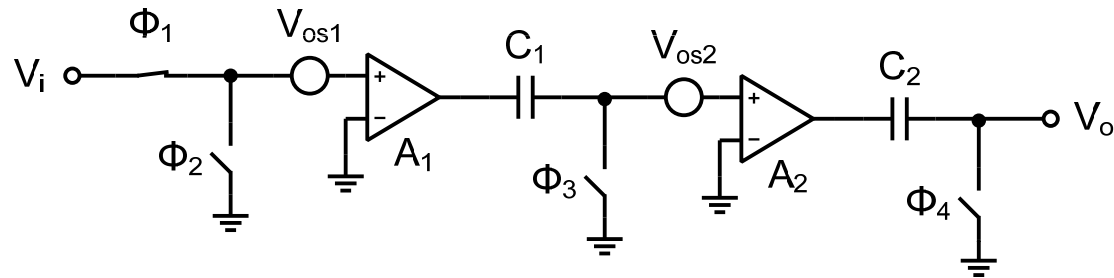# Amplifying Phase – Φ_1

$$V_o = A(V_i - V_{os}) + AV_{os}$$
$$= AV_{in}$$

$\Rightarrow$

Input $-$ referred offset $= 0$

- Cancellation is complete if A is constant (independent of V_o).
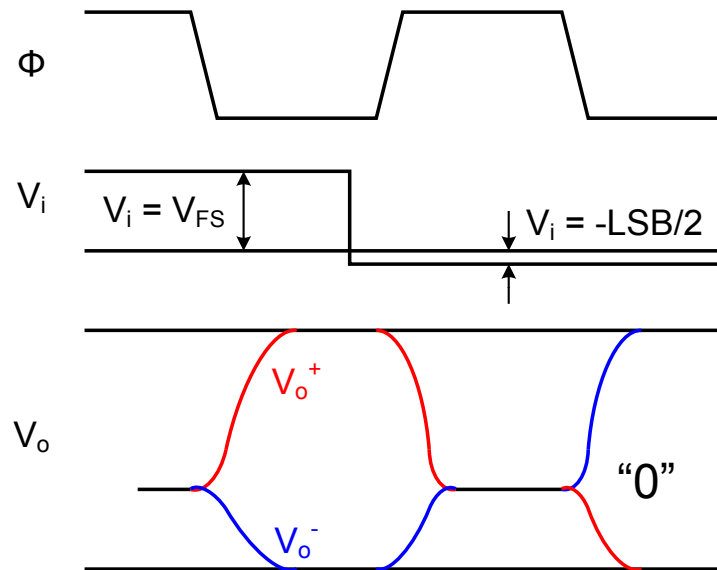
- AC coupling at output attenuates signal gain.
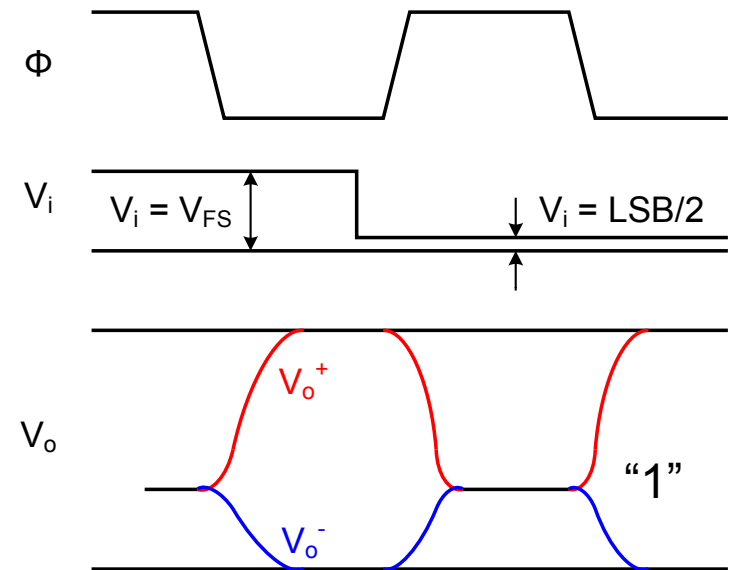
Multi-Stage Output Offset Cancellation

- Multi-stage AC coupling

- Φ_3 switches off first
  $\rightarrow \Delta V_1$ on C_1 will be
  absorbed by C_2.

- Φ_4 switches off next, Φ_2
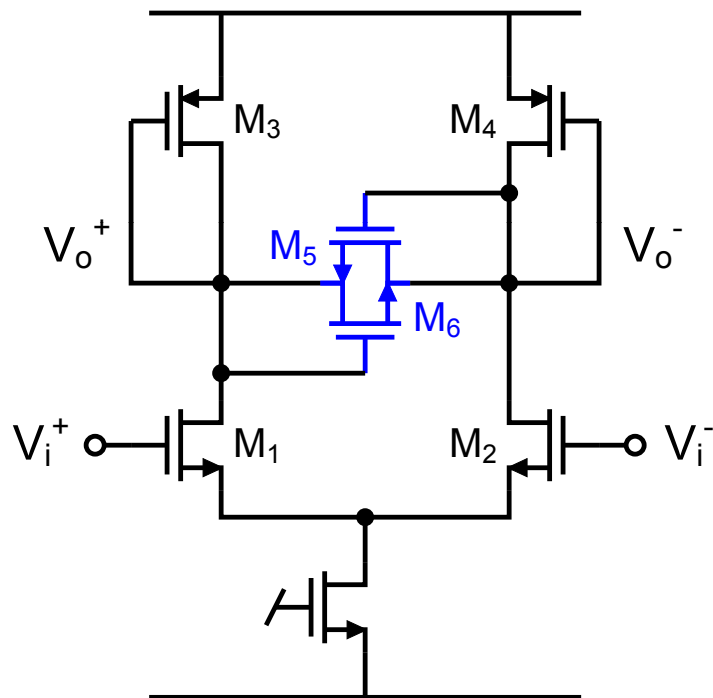 last.

# Overdrive Recovery

Overdrive Recovery Test

Case I

Case II

A small input (±0.5 LSB) is applied to the comparator input in a cycle right after a FS input (the largest possible input) was applied; the comparator should be able to resolve to the right output in either case.
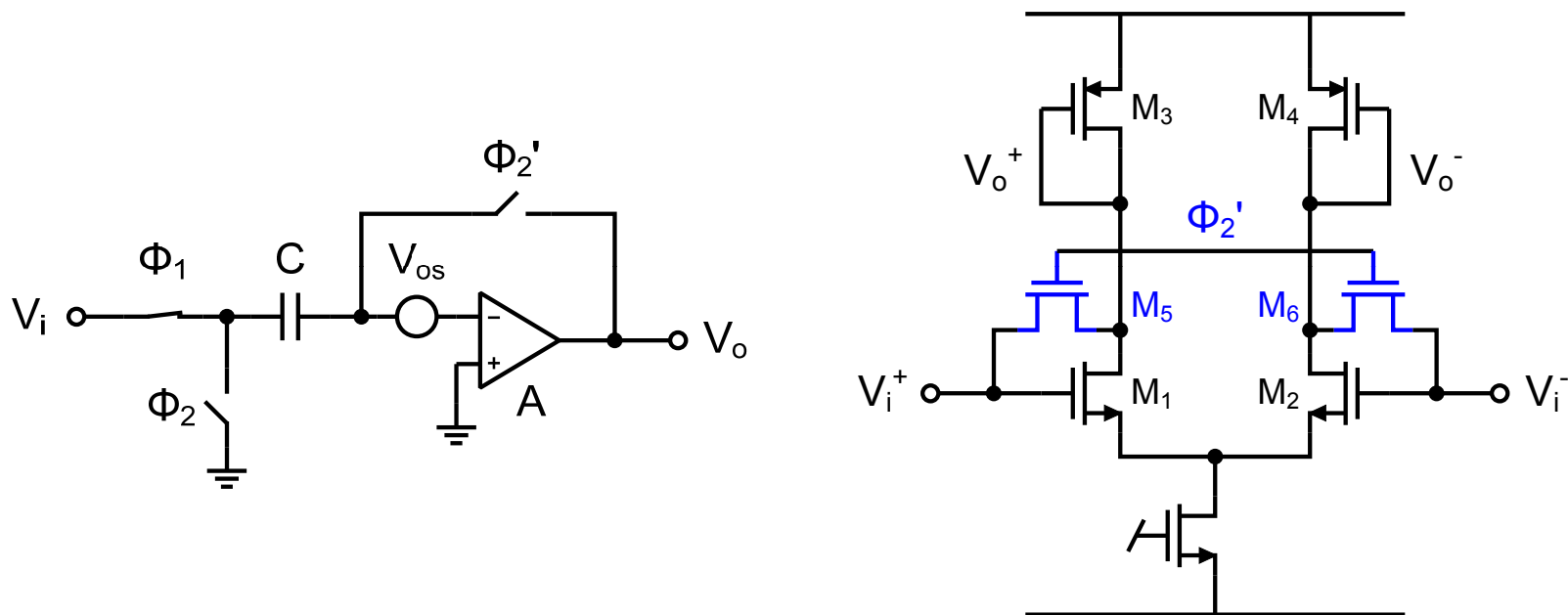
Passive Clamp

- Limit the output swing with diode clamps at output.

- Signal-dependent R_o

- Clamps add parasitics to the PA output.

Active Reset
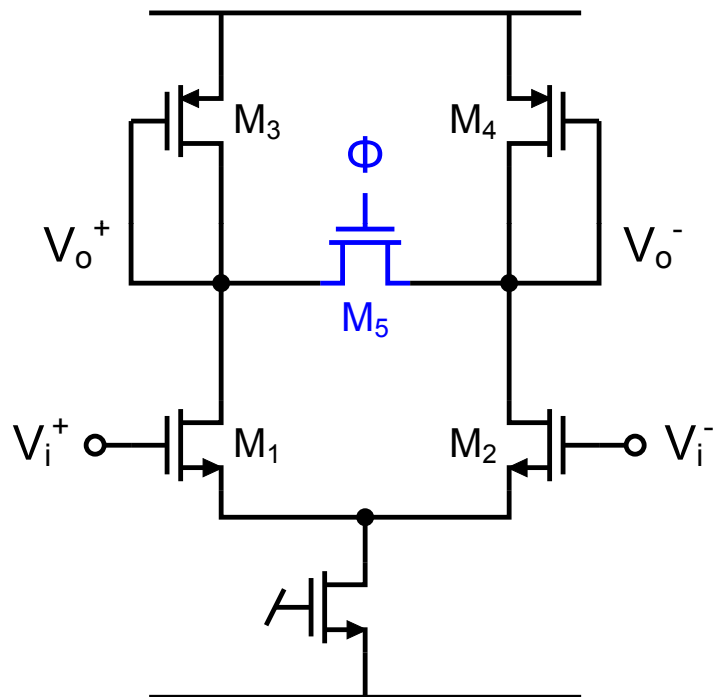
- Kill PA gain with a switch (M_5).

- Time-dependent R_o

- M_5 adds parasitics to the PA output.

PA Autozeroing

- Two-phase operation, Φ_2 phase is used for offset storage.

- Autozeroing switch Φ_2' also resets and removes the memory of PA.