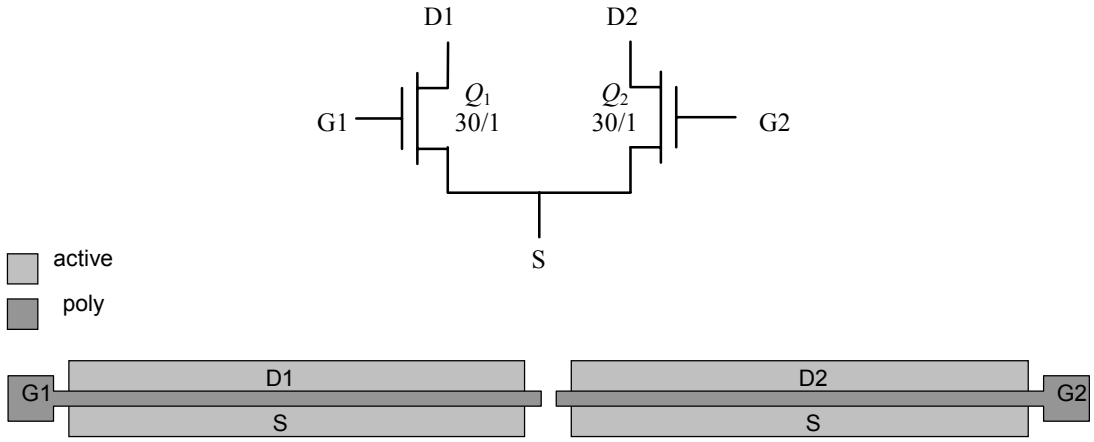
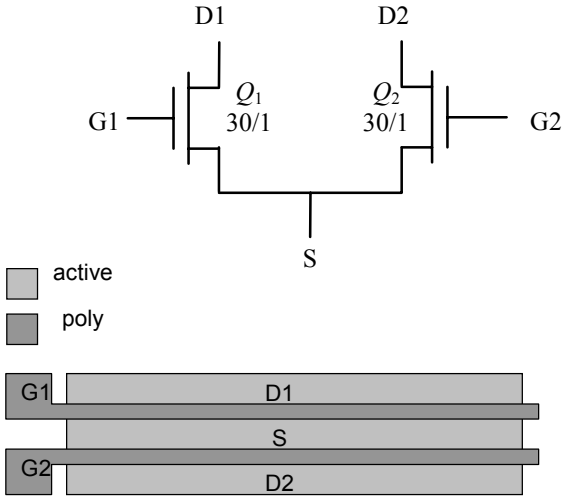
Basic Differential Pair Layout



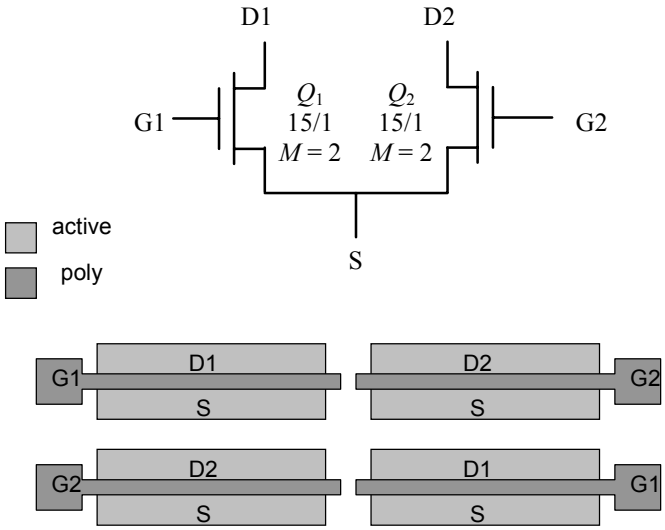
Good matching in the absence of cross-chip gradients; both drain currents flow in same direction.

Alternative Differential Pair Layout



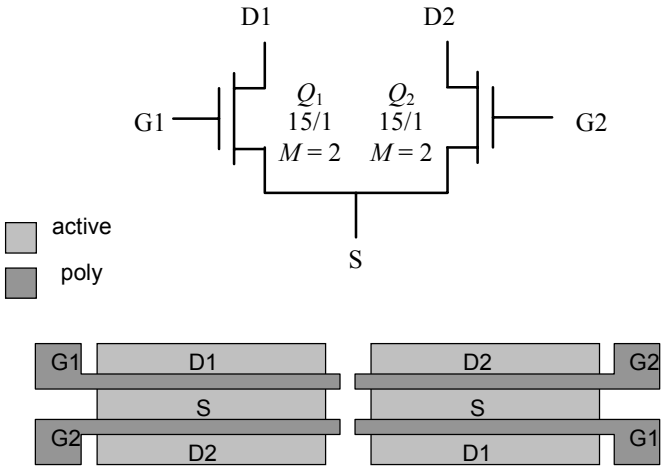
More compact, but worse matching than previous case; drain currents flow in opposite directions.

Common Centroid Layout



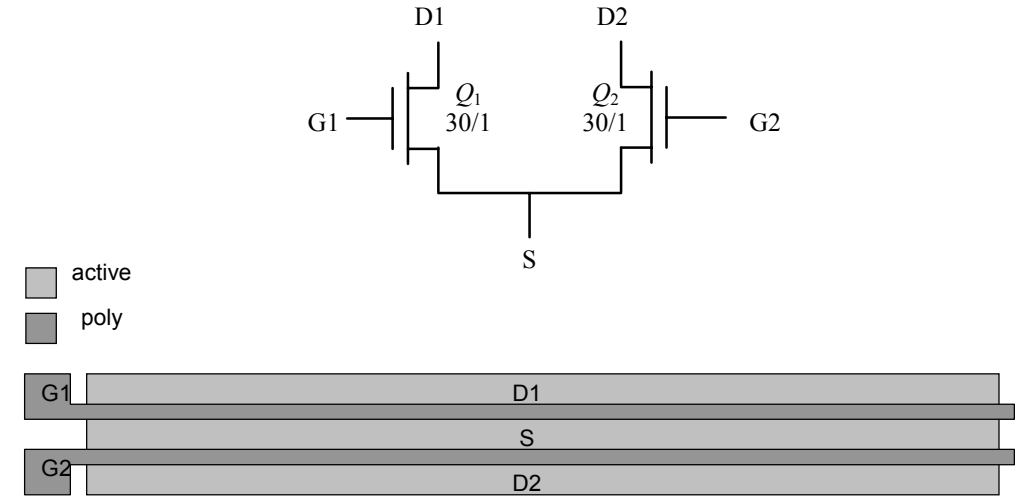
Q_1 and Q_2 have a "common centroid", which makes them immune from cross-chip gradients. Best matching performance possible.

Alternative Common-Centroid Layout



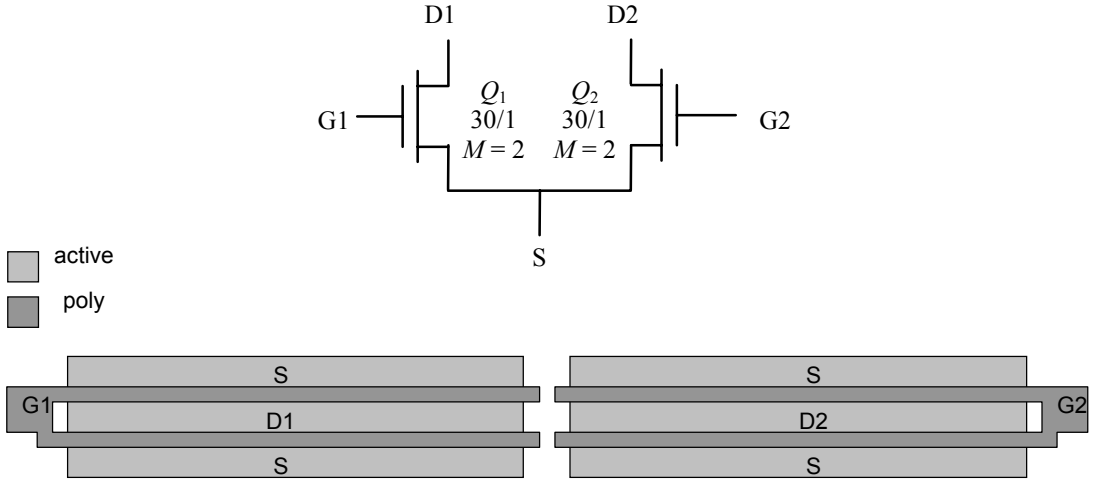
Immune from cross-chip gradients like previous case, but area is saved by sharing sources.

Differential Pair with Very Wide Transistors



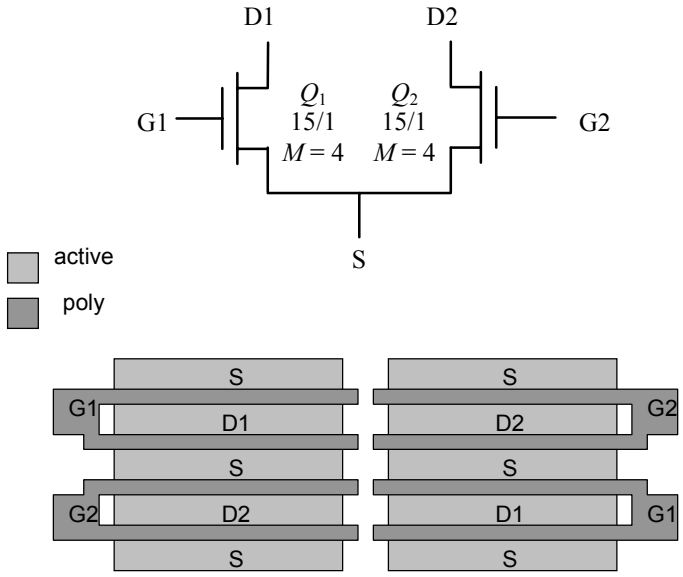
Very wide transistors can lead to awkward layout and significant series gate resistance.

Multi-Finger Transistors



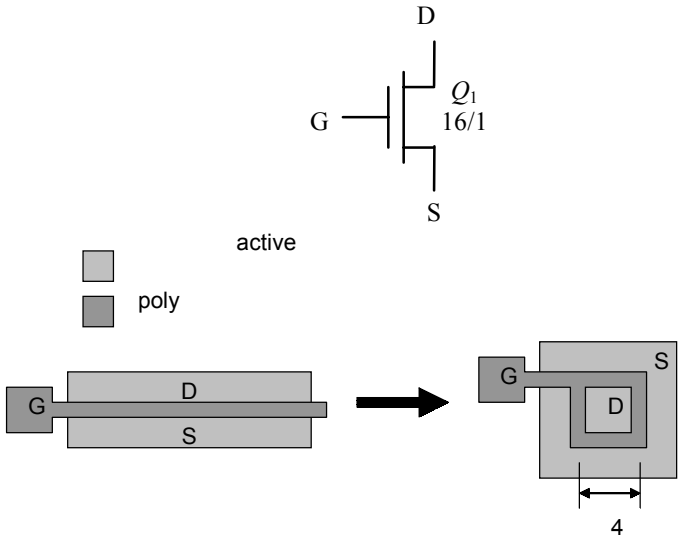
Multi-fingered gates save space and reduce series resistance in gate. Notice that drains are selected to minimize parasitic capacitance to bulk.

Common Centroid Layout with Multi-Fingered Gates



Drain-to-bulk parasitic capacitance is minimized; sources are partially shared to save area.

"Doughnut" Transistors



Gives the minimum C_{gd} (gate-to-drain overlap) and C_{db} (drain-to-bulk) parasitic capacitances for a given W/L ratio. May be used to minimize Miller effect when high speed is desired and a dominant pole is created elsewhere.