A 109 nW, 44 ppm/°C CMOS Current Reference with Low Sensitivity to Process Variations

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***Abstract*— We present the design of a circuit, implemented in a standard 0.35 µm CMOS process, that provides a bias current practically independent of temperature and process variations. Experimental results show that the proposed circuit provides a reference current with a temperature coefficient of 44 ppm/°C over a range from 0 to 80 °C. The reference current is generated by exploiting a MOS transistor as current defining element, instead of a resistor, allowing us to achieve a relative standard deviation due to process variations of 2%. The minimum supply voltage is 1.3 V and the minimum supply current is 36 nA. The line sensitivity is 569 ppm/V. The chip area is 0.035 mm^2.**

I. INTRODUCTION

Low voltage and extreme low power are essential design requirements for circuits and systems to be deployed in a pervasive electronics scenario, where battery replacement can be very costly or where other scarce energy scavenging techniques are used. This leads to a strong demand for circuit building blocks operating with low supply voltage and sub microwatt power. Among them, voltage and current reference generators are used in almost all analog and digital systems to provide very stable, temperature-independent voltage and current references. Many high precision and temperature-compensated current references have been presented in the literature [1-5]. Classical CMOS current references use a resistor as a current-defining element [1,5]. The core of a classical current reference circuit is shown in Fig. 1. All MOS transistors operate in the saturation region. By using the square law for the I-V characteristic of the MOS transistor, the reference current has the expression shown below,

$$I_{REF} = \frac{2}{\mu_p C_{ox} (W/L)_p} \frac{1}{R^2} \left(1 - \frac{1}{\sqrt{K}}\right), \qquad (1)$$

where μ_p is the hole mobility in PMOS transistors, C_{ox} is the oxide capacitance and W and L are the channel width and length. As clear from (1) they require very large resistance to produce nanoampere reference currents, which are required in ultra-low-power systems, leading to a large area occupation on the chip. Moreover, since the standard deviation of an integrated resistor can be larger than 30%, the generated current is very sensitive to process variations.

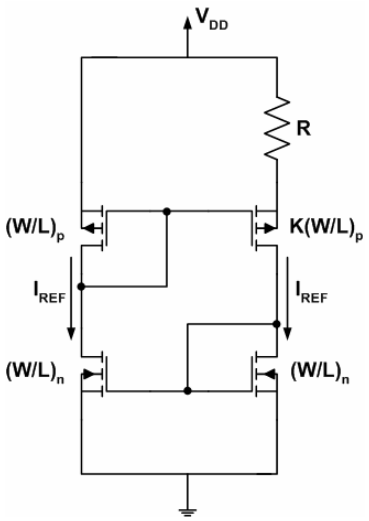

Fig. 1: Core of a classical current reference

The temperature coefficient of the reference current is given by,

$$\frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T} = -\frac{1}{\mu} \frac{\partial \mu}{\partial T} - \frac{2}{R} \frac{\partial R}{\partial T}. \qquad (2)$$

Since the two terms of (2) are process parameters, the temperature of the reference current cannot be set to zero through design. Some solutions have been proposed in the literature to overcome such inconvenient [5], even if the problems due to the area occupation and process sensitivity remain.

For such reason, resistorless current references have been proposed in the literature but they have poor temperature coefficient and sensitivity to process variations [2] or too large area occupation [3].

In this paper we present a resistorless current reference circuit with small temperature coefficient and sensitivity to process variations and, at the same time, small area occupation on the chip.

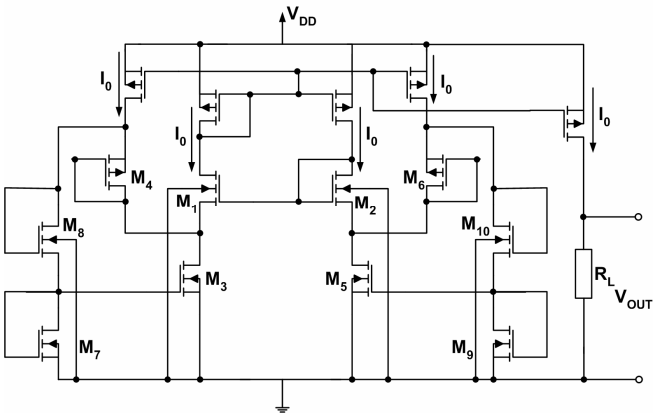

Fig. 2: Proposed current reference.

II. Circuit Description

The proposed current reference circuit is shown in Fig. 2. The two transistors M_1 and M_2 work in the subthreshold region while all the others transistors work in the saturation region. The I-V characteristics of a MOS transistor that operates in the saturation and in the subthreshold region can be approximated by (3) and (4), respectively,

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{th}\right)^2 = \frac{k}{2}\left(V_{GS}-V_{th}\right)^2, \tag{3}$$

$$I_D = \mu V_T^2 \frac{W}{L}\exp\left(\frac{V_{GS}-V_{th}}{mV_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right], \tag{4}$$

where μ is the carrier mobility in the channel, V_T is the thermal voltage, V_{th} is the threshold voltage, m is the subthreshold slope coefficient, W and L are the channel width and length, respectively. Referring to Fig. 2, we can write

$$V_{GS1} + V_{DS3} = V_{GS2} + V_{DS5}. \tag{5}$$

We can use (4) to derive the gate-source voltages of M_1 and M_2 in the case of a drain-source voltage much larger than the thermal voltage V_T. Assuming equal currents in the two branches, we can derive that,

$$V_{DS5} - V_{DS3} = mV_T \ln\left(\frac{(W/L)_2}{(W/L)_1}\right). \tag{6}$$

By using (3) to express the current flowing in both M_7 and M_8 and noticing that $V_{GS7} = V_{GS3}$ we can derive the source voltage of M_4

$$V_{S4} = V_{thn}\left(1-\sqrt{\frac{k_7}{k_8}}\right)+\left(1+\sqrt{\frac{k_7}{k_8}}\right)V_{GS3}, \tag{7}$$

where V_{thn} is the threshold voltage of an NMOS transistor.
By design, we make the current in M_7 and M_8 negligible with respect to that in M_4, so that the drain current of M_4 is practically I_0 and that of M_3 is $2I_0$. With such assumption we can derive V_{GS4} and then write the drain-source voltage of M_3, V_{DS3}, as $V_{DS3} = V_{S4} - |V_{GS4}|$. From (7), we have

$$V_{DS3} = V_{thn}\left(1-\sqrt{\frac{k_7}{k_8}}\right)+\left(1+\sqrt{\frac{k_7}{k_8}}\right)\left(V_{thn}+\sqrt{\frac{4I_0}{k_3}}\right)-|V_{thp}|-\sqrt{\frac{2I_0}{k_4}}, \tag{8}$$

where V_{thp} is the threshold voltage of a PMOS transistor.
In the same way we can derive the expression of the drain-source voltage of M_5 as,

$$V_{DS5} = V_{thn}\left(1-\sqrt{\frac{k_9}{k_{10}}}\right)+\left(1+\sqrt{\frac{k_9}{k_{10}}}\right)\left(V_{thn}+\sqrt{\frac{4I_0}{k_5}}\right)-|V_{thp}|-\sqrt{\frac{2I_0}{k_6}}. \tag{9}$$

By substituting (8) and (9) in (6) and by assuming $k_7/k_8 = k_9/k_{10}$, the expression of the reference current I_0 is given by,

$$I_0 = \frac{k_5}{2}\frac{m^2V_T^2\ln^2(n)}{\left[\sqrt{2}s\left(1-\sqrt{p}\right)+\sqrt{\mu_n/\mu_p}\left(\sqrt{l}-\sqrt{t}\right)\right]^2}, \tag{10}$$

where $n = k_2/k_1$, $p = k_5/k_3$, $s = 1+\sqrt{k_9/k_{10}}$, $t = k_5/k_6$, $l = k_5/k_4$, μ_n is the carrier mobility of an NMOS transistor. As clear from (10), the sensitivity of the reference current to process variations, if matching errors are neglected, is due to carrier mobility. Mobility has a dispersion of about 5%, which is much smaller than that the tolerance of an integrated resistor (even larger than 30%), leading to a sensitivity to process variations much smaller than that of current reference circuits that use an integrated resistor as current-defining element.

III. Temperature Coefficient

As a first approximation we can assume that the mobility has the following temperature dependence [6],

$$\mu = \mu_0\left(\frac{T}{T_0}\right)^{-\mu_T}, \tag{11}$$

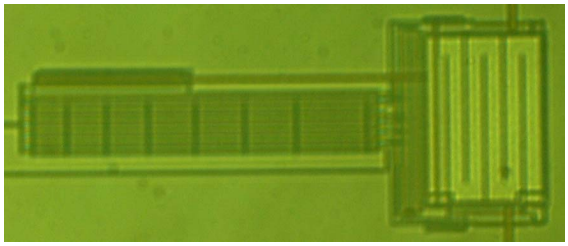

Fig. 3: Die Photograph (core).

where μ_0 is the mobility at the reference temperature T_0, μ_T is exponent mobility coefficient. By differentiating (10) and taking into account (11), we can derive the temperature coefficient of the reference current. By setting the temperature coefficient to zero, one can obtain,

$$\sqrt{l}-\sqrt{t}=\sqrt{2\frac{\mu_p}{\mu_n}\frac{2+\mu_{Tn}}{2+\mu_{Tp}}}\,s\left(\sqrt{p}-1\right), \tag{12}$$

where, μ_{Tn} and μ_{Tp} are the exponent mobility coefficient in a NMOS and PMOS transistor, respectively. As a consequence, with an appropriate choice of the coefficients l and t, we can achieve a zero temperature coefficient. Even though the temperature coefficient is not temperature-independent, it exhibits small variations around the reference temperature at which the condition of zero temperature coefficient has been enforced.

IV. Sensitivity to Process Variations

If matching errors are neglected, the coefficients n, p, s, l and t in (10) can be considered process independent, since they are W/L ratios of MOS transistors. Therefore, the sensitivity of the reference current to process variations is due to the carrier mobility μ_n of an NMOS transistor and μ_p of a PMOS transistor. From (10) we can derive the following expression for the variation dI_0 of the reference current,

$$dI_0=a\frac{d\mu_n}{\mu_n}+b\frac{d\mu_p}{\mu_p}, \tag{13}$$

where a and b are two coefficients derived by differentiating (10). The ratio a/b has the expression shown below,

$$\frac{a}{b}=\frac{\sqrt{2}s\left(1-\sqrt{p}\right)}{\mu_p\sqrt{\mu_n}\left(\sqrt{l}-\sqrt{t}\right)}. \tag{14}$$

By substituting the expression of $\sqrt{l}-\sqrt{t}$ given in (12), in (14), we can rewrite (14) as

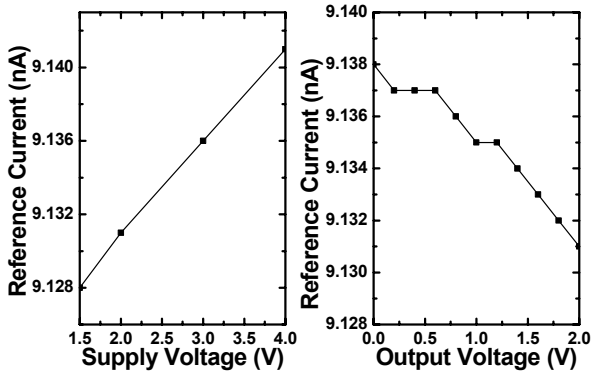

Fig. 4: a) Reference current vs. supply voltage at room temperature, b) reference current vs. output voltage for V_{DD}=3 V.

$$\frac{a}{b}=-\frac{2+\mu_{Tp}}{\mu_p\sqrt{\mu_p}\left(2+\mu_{Tn}\right)}. \tag{15}$$

In our technology the ratio a/b is about -158. Since the standard deviations of μ_n and μ_p are equal and by taking into account that $a>>b$, the relative variation of the reference current can be written as,

$$\frac{dI_0}{I_0}\cong a\frac{d\mu_n}{\mu_n}=\frac{2+\mu_{Tp}}{\mu_{Tp}-\mu_{Tn}}\frac{d\mu_n}{\mu_n}\cong -0.4\frac{d\mu_n}{\mu_n}. \tag{16}$$

Since in our process the standard deviation of the mobility is about 5%, we expect that the standard deviation of the reference current is about 2%.

V. Experimental Results

The proposed current reference circuit has been implemented in AMS 0.35 µm CMOS. The die photograph is shown in Fig. 3. Measurements show that the proposed current reference generates an average reference current of about 9.14 nA. Fig. 4a shows the reference current as function of the supply voltage at room temperature. Experimental results show that the reference current has a variation of 14 pA at room temperature when the supply voltage varies from 1.5 V to 4 V leading to a line sensitivity of 569 ppm/V. Fig. 4b shows the reference current when the output voltage varies. With a supply voltage of 3 V, the reference current has a variation of 7 pA when the output voltage varies from 0 to 2 V, leading to a load sensitivity of 274 ppm/V. The minimum supply voltage that ensures the correct operation of the current reference circuit is 1.5 V. The supply current is four times the reference current, that is 36.6 nA. Fig. 5 shows the reference current dependence on temperature for different values of the supply voltage. The measured temperature coefficient is 44 ppm/°C at V_{DD}=3 V,

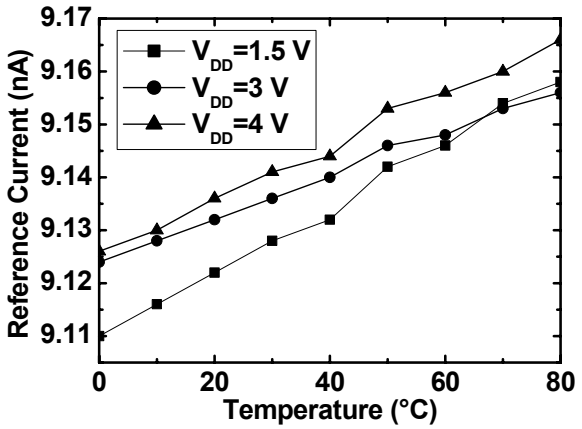

Fig. 5: Reference current vs. temperature for different values of the supply voltage.

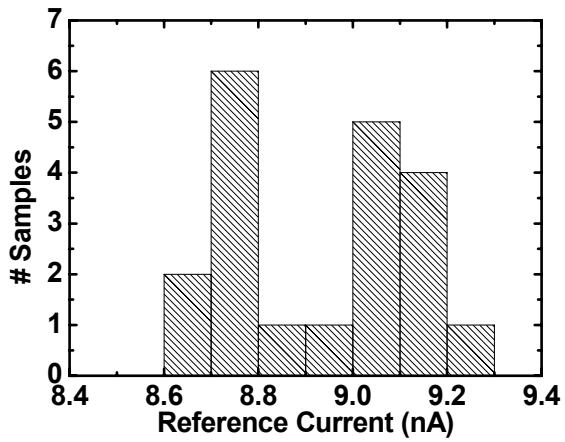

Fig. 6: Histogram of the reference current for 20 measured samples from different wafers.

55 ppm/°C at V_{DD}=4 V and increases to 66 ppm/°C at V_{DD}=1.5 V, corresponding to the minimum allowed supply voltage. In order to evaluate the sensitivity of the reference current to process variations, 20 samples from different wafers of the same batch have been tested and the results are shown in the histogram of Fig. 6. Experimental results show a standard deviation of the reference current of 2.16%, which is very close to the value expected from theoretical analysis and Monte Carlo simulation results. The area occupation on the chip is 0.035 mm^2. The performance of the proposed current reference generator is compared with those of other designs already reported in the literature and implemented in a standard CMOS process in Table I. We can note that the proposed current reference generator is able to work with the lowest supply voltage and the lowest supply current fitting the requirements of modern low-voltage low-power systems. Moreover, the proposed circuit shows very good performance in terms of temperature coefficient, line sensitivity, load sensitivity and process sensitivity. The area occupation is acceptable.

Table I: Comparison with other designs reported in the literature.

	This work	Lee [1]	Sansen [2]	Georgiou [3]	Fiori [5]
Technology	0.35 µm CMOS	2 µm CMOS	3 µm CMOS	0.8 µm CMOS	0.35 µm BiCMOS
Minimum Supply Voltage (V)	1.5	N/A	3.5	2.5	2.5
Reference Current (nA)	9.14	287	774	430	13650
Supply Current (nA)	36.56	N/A	2000	860	N/A
TC (ppm/°C)	44	226	375	600	28
Line sensitivity (ppm/V)	569	4000	130	5000	4000
Load Sensitivity (ppm/V)	274	N/A	400	1455	N/A
Process sensitivity (3σ)	6.5%	N/A	2.5%	23%	57%
Area (mm^2)	0.035	N/A	0.2	0.002	0.0042

VI. CONCLUSIONS

A current reference generator implemented in AMS 0.35 µm CMOS has been presented and its design criteria have been discussed in detail. The proposed topology is resistorless, allowing us to achieve small area occupation on the chip and low sensitivity to process variations. The proposed circuit fits the requirements of modern low-power and low-voltage systems providing, at the same time, very low sensitivity to process and temperature variations, low supply and load sensitivity.

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