

Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits

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Abstract— We report an accurate and practical method of estimating interconnect capacitances for a given circuit layout. The method allows extraction of the complete circuit level capacitances at each node in the circuit. The layout geometry is reduced into base elements that consist of different vertical profiles at each node in the layout. Accurate analytical models are developed for calculating capacitances of multilayer structures using a 2-D capacitance simulator TDTL. These models are then transformed into 3-D geometry. The resulting model capacitance values are found to be within 10% of both the measured data and 3-D simulations of structures that are prevalent in a typical VLSI chips. The models and their coefficients for different vertical profiles are stored in the capacitance extraction tool CUP, which is coupled to the layout extractor HILEX. As each base element has a unique vertical profile, the corresponding capacitance can easily be calculated for each node that is then written out to a circuit netlist. The comparisons of the models with the measured data, as well as 3-D simulations results, are also discussed.

I. INTRODUCTION

A VLSI circuit can be viewed as a dense system of metal layers in a stratified dielectric medium over a silicon substrate. The computation of capacitances between different metal layers for such a densely packed multiconductor system is a complex and difficult task. Numerical techniques such as finite difference [1]–[4], finite element [5], [6], boundary element methods [7]–[9], and recently reported multipole algorithms [10] exist to evaluate these capacitances but are too compute intensive to be applied at the VLSI chip level. On the other hand, fast empirical models have also been proposed [11]–[13], but they are not accurate enough, particularly for estimating 2-D and 3-D coupling capacitances.

In the past, procedures for estimating interconnect capacitances at the circuit level have been proposed and implemented [14]–[18], wherein interconnect lines are modeled as distributed lumped circuit elements directly from the layout by using analytical formulas. However, in all these procedures, very approximate formulations have been implemented for estimating the capacitances that limit the validity of the results. For example, the fringe capacitance is calculated using a simple analytic formulation that assumes the fringing surface to be a ground plane. Thus, it completely ignores: (1) the fringe capacitance dependence upon the fringe surface area, and (2)

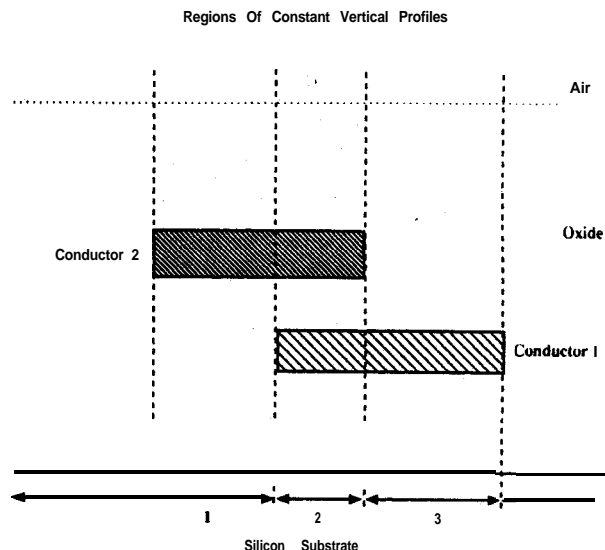


Fig. 1. Vertical profiles at four different points between conducting lines Conductor 1 and Conductor 2, illustrating the concept of vertical profiles.

the presence of other conductors above and below it. Since a VLSI circuit is inherently a 3-D structure, the “vertical profile” (see Section II) varies considerably depending upon its spatial location. This is clear from Fig. 1, which shows three vertical profiles in a typical two-layer metallization system.¹ Ignoring the presence and size of other conductors, while calculating the capacitance at a given point in the circuit, is a serious drawback of most of the published methods of estimating capacitances in a VLSI circuit.

In this paper, we report an accurate and practical method of estimating interconnect capacitances for a given layout. The layout geometry is first reduced into base elements, generally trapezoids, on a conducting layer. Next, transformations are applied to the area of the trapezoids to compute the capacitance contribution of each trapezoid. The use of transformations is necessary as capacitance models are extracted using 2-D simulations whereas layout geometry is 3-D in nature. The capacitance of the trapezoids is estimated as a sum of three components, the parallel plate capacitance (due to overlap area), the lateral capacitance (coupling between nonoverlapping conductors in the same plane), and the fringe capacitance (coupling between conductors in different planes). As a result

¹ Throughout the text the word metal and conductor are used interchangeably.

Manuscript received November 9, 1994; revised June 14, 1995. This paper was recommended by Associate Editor J. White.

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Publisher Item Identifier S 0278-0070(96)01340-1.

of these approximations, any complicated geometry can be evaluated by algebraic operations on these elements. The unit capacitance parameters for these elements themselves are derived by precharacterizing and parameterizing a 2-D/3-D model library using numerical simulations. Since the model libraries are valid only for a given technology, these libraries need to be generated for each technology. This is the price paid to achieve higher accuracy in calculating interconnect capacitances as against simple analytical models that are usually valid only for lumped structures and are of limited accuracy [13].

Our method of estimating the capacitances in a given layout has been in regular use at Digital for many years. It has been used extensively in the design of several chips, including all of Digital's Alpha microprocessors. The algorithms are fast enough to routinely compute capacitances for all nodes of multimillion transistor circuits. The method of estimating nodal capacitances also allows one to

- easily construct models for nodal capacitances as a function of process parameters,
- optimize the process in order to achieve target node capacitances.

The procedures for estimating the interconnect capacitances in a VLSI circuit are discussed in Section II. The capacitance models and their parameters (coefficients) derived from 2-D numerical simulations for different geometries are discussed in Section III. This is followed by a discussion on automatic generation of the model libraries for different structures in Section IV. Comparisons of the models with the measured data, as well as 3-D simulations results, for some geometries are discussed in Section V. The discussion on model validation at the circuit level is covered in Section VI, followed by conclusions in Section VII.

II. PROCESS FLOW FOR ESTIMATING CAPACITANCES

The VLSI layout contains information about the connectivity and dimensions of various elements such as transistors, diodes, and their interconnections. Implicit in the layout is information regarding the vertical dimensions of the circuit. The sequence of material layers (conductors and dielectrics) that are present in a vertical dimension at any point on a VLSI circuit is referred to as the "vertical profile." The layout is typically extracted using a layout extraction tool such as HILEX² which is closely integrated to the capacitance extraction program CUP. This program then allows extraction of the complete circuit level capacitances at each node of the circuit.

Fig. 2 shows the block diagram of the capacitance extraction procedure as implemented in Digital's HILEX/CUP tool suite.

- 1) The layout obtained from HILEX is first flattened. The flattened layout and geometry information is then passed to CUP.
- 2) The layout (geometry) is then divided into stripes. Each stripe is approximately 200λ wide, where λ is the

² HILEX is Digital Equipment Corporation's proprietary Hierarchy Layout Extraction tool, which is a much improved version of the one reported in reference [14].

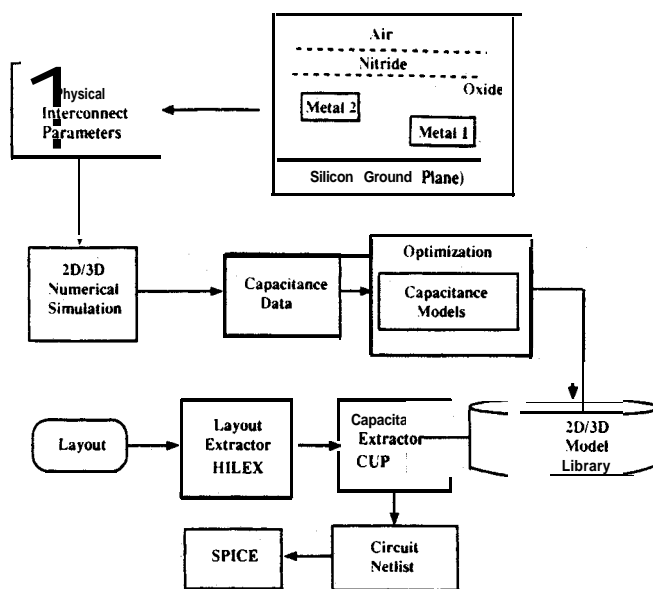


Fig. 2. Block diagram for estimating capacitances between metal lines for SPICE simulation.

"elementary distance unit" that is normally equal to half the minimum feature size for a given technology. Striping is performed across the layout, typically with a left to right sweep. The layout in each stripe can be processed independently.

- 3) Each stripe is next fractured into elemental areas that consist of rectangles and/or right or left angled triangles.
- 4) Processing for each stripe is started from the lowest level in the layer hierarchy. Calculations for the capacitance for each elemental area are then performed. These capacitance calculations are based on the models and their coefficients (see Section III) stored in the CUP model library for different vertical profiles. As each elemental area has a unique vertical profile which is now known, the corresponding capacitances are easily calculated. The elemental areas associated with a given node are then summed to give the total or "lumped" capacitance for each node that is then written out to a circuit netlist.

III. CAPACITANCE MODELS

The interconnect capacitance at each node in a circuit is calculated using the model shown in Fig. 3(a). It consists of three conducting layers over the substrate treated as a reference plane (ground potential). The three layers are: (1) bottom conductor-1, (2) middle conductor-2, the conductor of interest, and (3) top conductor-3; they are assumed to be perfect conductors (zero resistivity). The equivalent circuit model for the geometry of Fig. 3(a) is shown in Fig. 3(b). The capacitance of interest at any node, in general, consist of the following three components:

- the overlap capacitance C_a due the overlap between two conductors in *different* planes,
- the lateral capacitance C_{lt} between two conductors in the *same* plane

- the fringe capacitance C_{fr} , that represents coupling between two conductors in **different** planes.

Thus, in general, the interconnect capacitance C_t at any node is given by

$$C_t = C_a + C_{lt} + C_{fr}. \quad (1)$$

For the geometry shown in Fig. 3(a), the overlap capacitance is the sum of the capacitance due to the overlap between conductor-2 and conductor-3 (C_{23a}) and between conductor-2 and conductor-1 (C_{21a}). Similarly, the fringe capacitance C_{fr} is the sum of the capacitances C_{21f} and C_{23f} , while the lateral capacitance is the sum of C_{24} and C_{25} (see Fig. 3(a)). Note that C_{21f} and C_{23f} are the sum of the fringing capacitance from both edges of the conductor-2 to the surface of the conductors 1 and 3, respectively. Thus, $C_{21f} = C'_{21f} + C'_{21f}$. Also, note that value for the lateral (C_{24} and C_{25}) and fringe (C_{21f} and C_{23f}) capacitances are affected by the presence and/or absence of conductor-1 and conductor-3. Thus, the capacitance of the conductor-2 (self capacitance) is in fact, the sum of

$$C_{22} = C_{21a} + C_{23a} + C_{21f} + C_{23f} + C_{24} + C_{25} + C_{2ref} \quad (2)$$

where C_{2ref} is capacitance of the conductor-2 with respect to reference (ground) plane. The values for C_{ij} ($i, j = 1 \dots n$, n being the number of conductors) are calculated using the boundary element capacitance simulator **TDTL**³ similar to the one discussed in [7]. For the geometry of Fig. 3(a), the numerically simulated capacitance matrix is a 5 x 5 matrix shown below

$$C_{ij} \equiv \begin{bmatrix} C_{11} & -C_{12} & -C_{13} & -C_{14} & -C_{15} \\ -C_{21} & C_{22} & -C_{23} & -C_{24} & -C_{25} \\ -C_{31} & -C_{32} & C_{33} & -C_{34} & -C_{35} \\ -C_{41} & -C_{42} & -C_{43} & C_{44} & -C_{45} \\ -C_{51} & -C_{52} & -C_{53} & -C_{54} & C_{55} \end{bmatrix}. \quad (3)$$

From this capacitance matrix, the coefficient C_{22} is the sum of $C_{21} + C_{23} + C_{24} + C_{25} + C_{2ref}$, which in fact is equivalent to (2). For the sake of clarity, in Fig. 3(a), we have not shown the conductor-2 capacitance with respect to the reference ground. Moreover, due to the shielding effect of **conductor-1**, the capacitance of conductor-2 with respect to the ground plane is negligible and can easily be ignored. The above capacitance matrix is obtained assuming quasi-static behavior of the electric and magnetic fields and thus is applicable only at low frequencies where the skin effect in conductors can be ignored.

It should be pointed out that the modeling approach we have developed is not restricted only to the structure shown in Fig. 3 but is applicable to any arbitrary geometry. However, structures such as vias are not presently modeled by this approach. In the following sections, we show models for the three components of the total node capacitance C_t .

³TDTL is Digital Equipment Corporation's proprietary Two Dimensional Transmission Line tool, which calculates line inductance and capacitances, and is based on algorithms reported in reference [7].

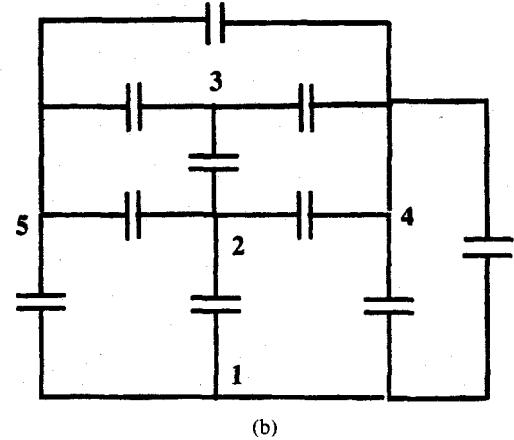
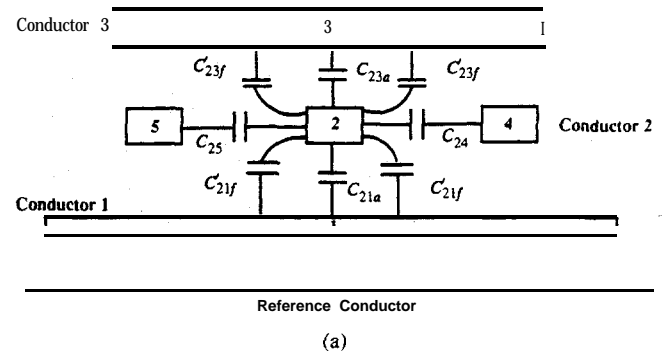


Fig. 3. (a) Five conductors structure showing different components of capacitances. (b) circuit equivalent model for structure shown in (a).

3.1. Overlap Capacitance

The overlap capacitance is formed by the surface overlap (in two dimensions) of two conductors l_1 and l_2 separated by a distance $d_{l_1 l_2}$ (see Fig. 4) apart. It is calculated using the following well known equation for parallel plate capacitance:

$$C_a = \frac{\epsilon_0 \epsilon_r}{d_{l_1 l_2}} \cdot A \quad (4)$$

where $\epsilon_0 (= 8.854 \times 10^{-14} \text{ F/cm}^2)$ is permittivity of free space, ϵ_r is the relative permittivity of the material between the two conductors l_1 and l_2 , and A is the overlap area between them (the shaded area in Fig. 4). The fabrication process is assumed to be planar so that the thickness $d_{l_1 l_2}$ between the conductors can be assumed constant for a particular layer combination. This capacitance is calculated only when the two conductors are not parts of the same electrical node. If N is the number of conducting layers in a circuit, then there will be $N(N-1)/2$ different numbers for $d_{l_1 l_2}$ that are stored in CUP.

3.2. Lateral Capacitance

The lateral capacitance is formed by two parallel edges of nonoverlapping (in two dimensions) conductors in the same plane as shown in Fig. 5. For the two parallel conductor edges, with a uniform vertical profile i in the capacitor region, the lateral capacitance is given by

$$C_{lt} = F_{l_1 l_1}^i(d) \cdot l \quad (5)$$

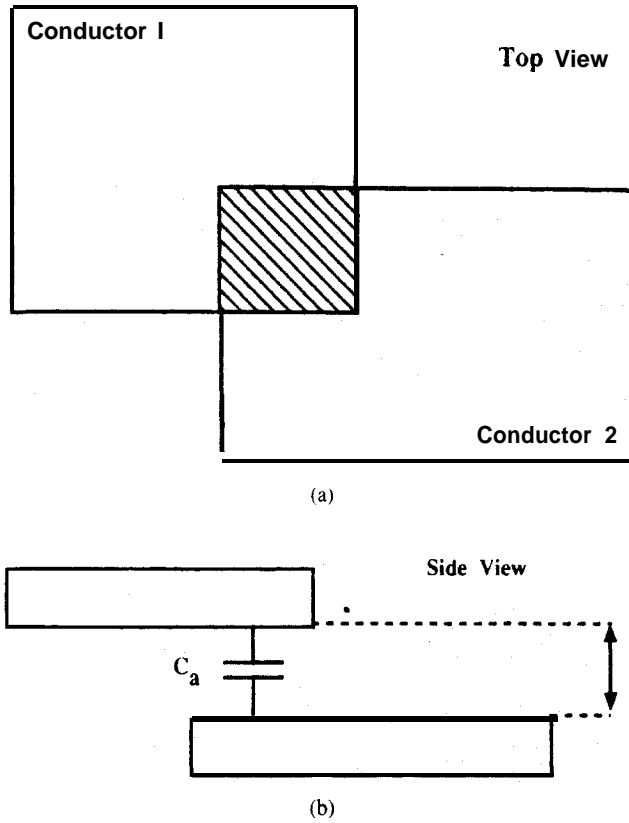


Fig. 4. Schematic showing overlap capacitance between two conductors. (a) Top view. (b) Side view. Shaded area is the area A in (4).

where l is the length of the parallel edges of the two conductors l_1 and l_2 in the same plane, $F_{l_1 l_2}^i(d)$ is the capacitance per unit edge length of two parallel edges of the conductors distance d apart, in the presence of the vertical profile i .

The function $F_{l_1 l_2}^i(d)$ is found to fit the following form:

$$F_{l_1 l_2}^i(d) = C_0 + \frac{C_1}{d} + \frac{C_2}{d^2} + \frac{C_3}{d^3} + \frac{C_4}{d^4} \quad (6)$$

where C_0, C_1, C_2, C_3 , and C_4 are constants arrived at after fitting this equation to the 2-D simulated [7] lateral capacitance data. Fig. 6 shows simulated (circles) lateral capacitance between two metal lines distance d apart and at height h from the silicon surface (treated as a ground plane). Curves A and B correspond to the capacitances between two conductors in the same plane (say, metal M1) with and without the presence of a metal M2 above M1, respectively. For both cases, the simulated data fits the modeled results (continuous lines), based on (6), to within 2%. Note that there is a separate set of these five constants, C_0, C_1 etc., for each vertical profile.

The value for C_{lt} depends upon the spacing d and the length l of the parallel edges of the conductors and the vertical profiles in the area between two parallel edges. Note that the vertical profile changes depending upon whether there are conductors above, below, and/or between the conductors whose edges form the capacitance to be calculated. As an example, Fig. 7 shows two M1 edges (conductors 1, 3) defining a capacitor (shaded area), and M2 (conductor 2) and M3 (conductor 4) edges partially shading the capacitor region,

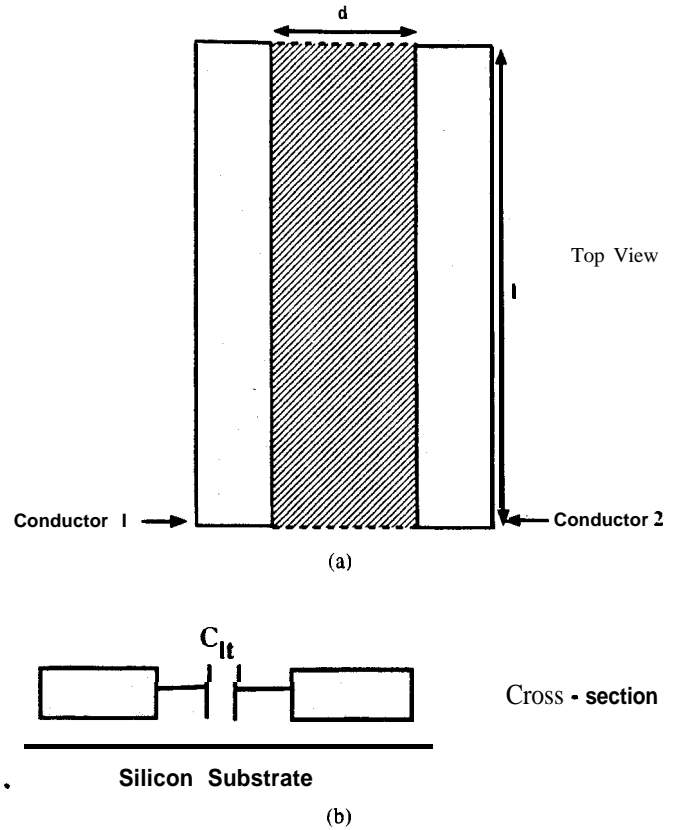


Fig. 5. Schematic showing coupling capacitance between two metal layers in the same plane. (a) Top view. (b) Side view.

clearly defining nine different regions with four distinct vertical profiles (marked A to D). In order to limit the processing time, the capacitance C_{lt} is ignored when the distance d between the conductors exceeds a certain maximum distance d_{\max} . The capacitance C_{lt} between two M1 conductors in the presence of conductors M2 and M3 above and below M1, respectively, are approximated by a linear interpolation rule. Thus, in such cases, the lateral capacitance is given by the area weighted mean of the capacitances for the separate profiles and is calculated using the following relation:

$$C_{lt} = \frac{\sum_{i=1}^n A^i \cdot F_{l_1 l_2}^k(d) \cdot l^i}{d \cdot l}, \quad k \ll i \quad (7)$$

where A^i is area of the i th ($i = 1, 2, \dots, n$) vertical profile region encountered within the capacitor region, l^i is length of the i th element such that $l = \sum_{i=1}^n l^i$. Note that in Fig. 7, there are nine regions ($i = 9$), but only five regions of constant vertical profile so that there are only four different $F_{l_1 l_2}^k$ ($k = 4$). This approach is valid because it is observed in the simulations that the lateral capacitance linearly varies with the variation in the area of a particular vertical profile. In the example shown in Fig. 6, the lateral capacitance between the M1 edges is calculated using (7), which is a weighted average of the lateral capacitances over the five different vertical profiles that occur. This linear approximation is fairly good for estimating capacitances at the circuit level and typically approximates the actual capacitance to within 10%.

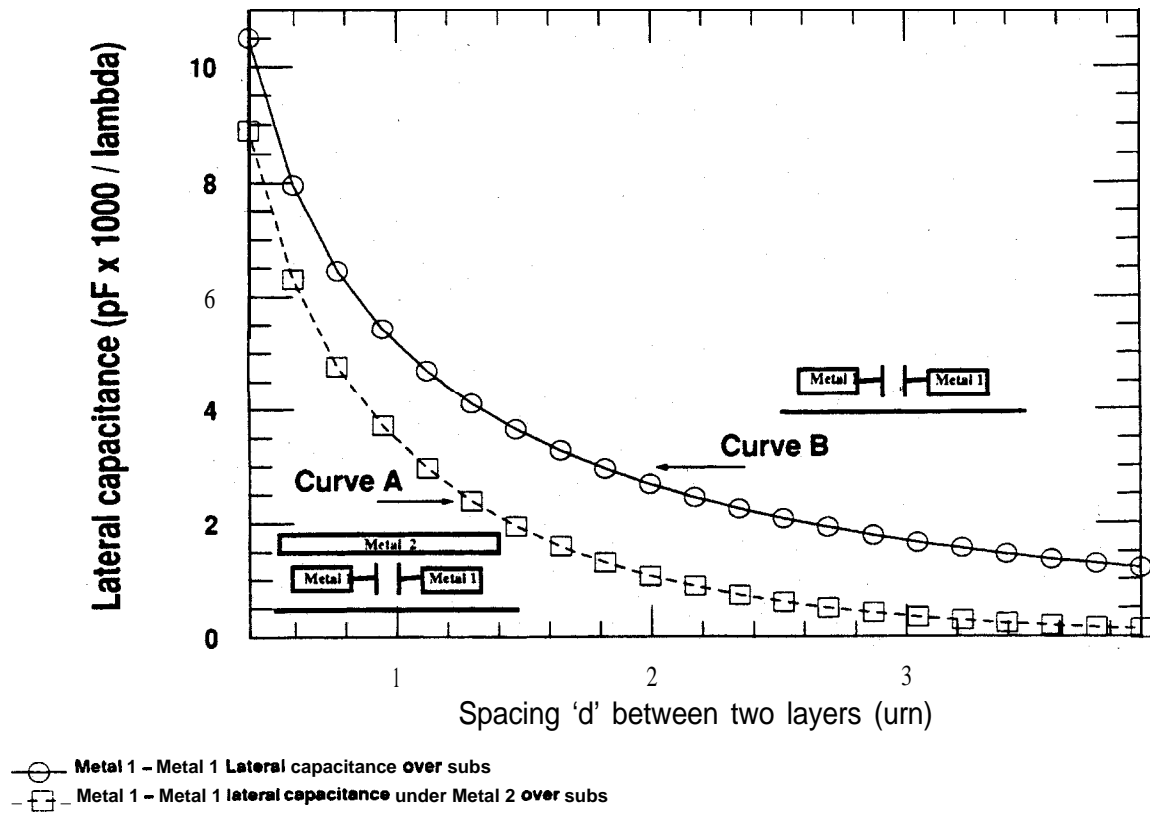


Fig. 6. Figure showing the lateral (coupling) capacitance between two layers as a function of distance between them with and without a shading layer.

3.3. Fringe Capacitance

The fringe capacitance C_{fr} is formed between the edge of one conductor and the surface of a second conductor above or below the first one. Fringe capacitance is identified only between the two conductors on different planes. Fig. 8(a) shows fringe capacitance when the two conductors overlap, while Fig. 8(b) shows the fringe capacitance when the edges do not overlap. The fringe capacitance between a given edge and a given surface depends on three factors: (1) area of the surface, (2) location of the surface with respect to the edge, and (3) geometry of the conductors involved.

From 2-D numerical solution, it is found that the fringe capacitance between conductors l_1 and l_2 can be modeled as

$$C_{fr} = C_{fro} \cdot l \cdot (e^{-x_1/x_0} - e^{-x_2/x_0}) \quad (8)$$

where x_1 and x_2 are the distances from the edge of conductor l_1 to the near and far surface edges, respectively, of conductor l_2 (see Fig. 8), C_{fro} is the maximum value of the fringe capacitance (see Fig. 9(b)), l is the length of the edge of l_1 , and x_0 is the measure of how the fringe capacitance varies for incremental length of the fringing surface (see Fig. 9(b)). If $x_1 = 0$, i.e., when the edge of conductor l_1 coincides with conductor l_2 , the above equation takes the form

$$C_{fr} = l \cdot C_{fro} \cdot (1.0 - e^{-x/x_0}) \quad (9)$$

and has the following physical interpretation. As the fringing surface is increased, the fringe capacitance increases and

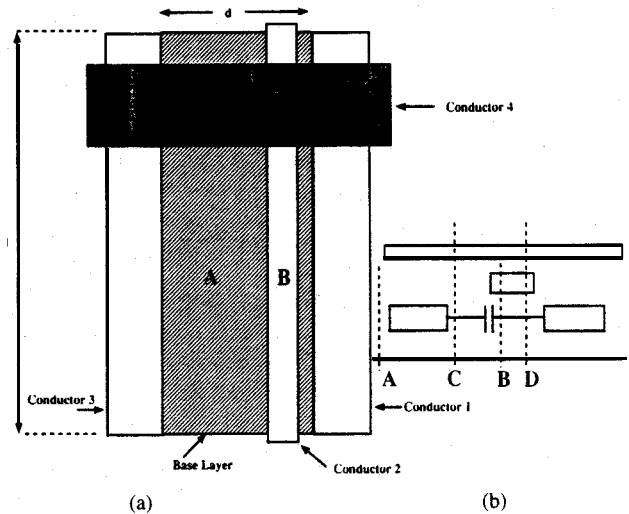


Fig. 7. Schematic showing lateral (coupling) capacitance between two metal layers (Conductors 1 and 3) in the same plane in the presence of other layers (Conductors 2 and 4) above the base layer. (a) Top view. (b) Side view. Four vertical profiles (dashed lines) are evident in (b).

in the limit when $x \rightarrow \infty$, C_{fr} asymptotically approaches C_{fro} . The simulated value of C_{fr} for three different values of x_0 , but a fixed value of C_{fro} are shown in Fig. 9(b). Note that although curves "b" and "c" do not approach to a constant C_{fro} , however, for large enough value of x , C_{fr} will approach C_{fro} . To determine C_{fro} and x_0 , simulations are performed using the geometry of Fig. 9(a), and parameters

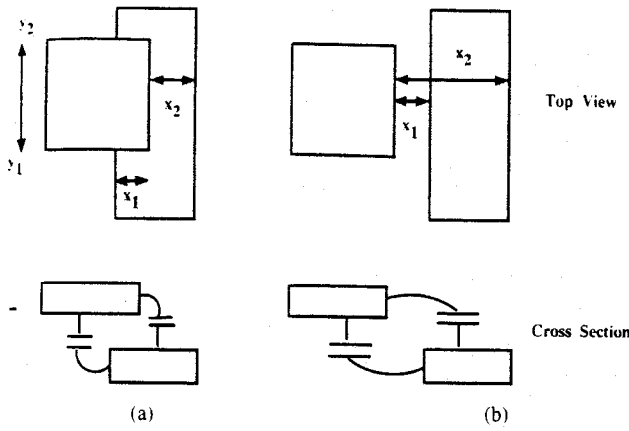


Fig. 8. Schematic showing the fringe capacitance between two layers in the case (a) with overlap between conductors and (b) without overlap between conductors.

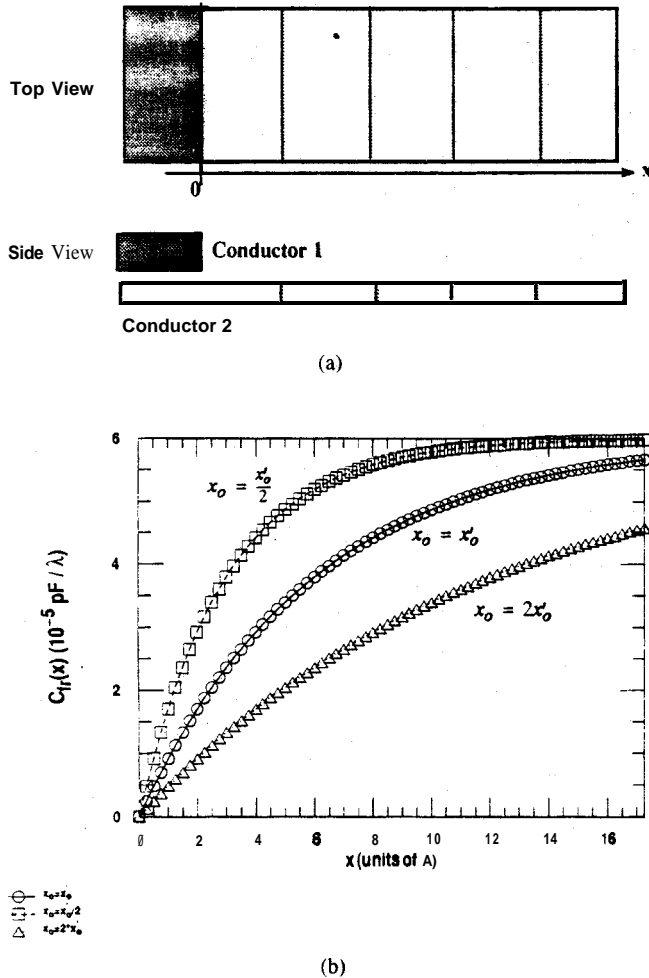


Fig. 9. Schematic indicating the geometry used to extract the fringing model coefficients and illustrating the behavior of the fringing capacitance.

C_{fro} and x_0 are determined by performing a least squares fit of the above equation to simulated data. A separate fringe capacitance is calculated for each vertical profile of interest, and these constants C_{fro} and x_0 are different for different vertical profiles.

For calculating the fringe capacitance between conductors l_1 and l_2 , the capacitor region of significance must be determined. This is found by forming a rectangle from the edge of interest extending to a distance d that is determined by a requirement for accuracy and speed of capacitance calculations. A large d implies a large rectangular region that has to be fractured into trapezoids and hence requires greater computational effort than a smaller region. However, a smaller d also results in ignoring fringe capacitance contributions beyond the particular d chosen. Therefore, d is chosen to be a value that is a suitable compromise between speed and accuracy. The fringe capacitance between an edge of a conductor l_1 and surface of another conductor l_2 , in the presence of vertical profile i is given by

$$C_{fr} = F_{l_1 l_2}^i a_e^i \quad (10)$$

where $F_{l_1 l_2}^i$ is a measure of fringe capacitance (per unit length) from edge of conductor l_1 to surface of the conductor l_2 , in the presence of vertical profile i , and a_e^i is the effective area in the transformed space as discussed below.

Fig. 10 illustrates the geometry for calculating fringe capacitance from a conductor edge to a surface at a distance x . The scaled area a_e^i is found by performing an integration over the edge of the conductor surface in the transformed domain using the following transformation:

$$\begin{aligned} x' &= x \\ y' &= y e^{-x/x_0} \end{aligned} \quad (11)$$

Since layout geometry is complex, it is fractured into polygons that are one of three types: rectangles, left-, or right-angled triangles. The fringe capacitance contribution for each of these elemental areas for a given vertical profile, in the capacitor region is then calculated using (10). The effective area for the rectangle is given by (see Fig. 10)

$$a_e^i = l \cdot x_0 \cdot (e^{-x_1/x_0} - e^{-x_2/x_0}) \quad (12)$$

where l is length y of the fringing conductor l_1 from conductor l_2 . The corresponding effective area for a right-angled triangle is given by

$$a_e^i = \frac{l}{(x_2 - x_1)} [x_0^2 e^{-x_1/x_0} + (x_1 x_0 - x_2 x_0 - x_0^2) e^{-x_2/x_0}] \quad (13)$$

Here (x_1, y_1) and (x_2, y_2) are coordinates of the trapezoid and are known from the layout. The expressions for the fringe capacitance can therefore be seen to consist of a coefficient that is derived from the product of $F_{l_1 l_2}^i$ and an effective area a_e^i .

IV. AUTOMATED GENERATION OF CAPACITANCE PARAMETERS

The complexity of the process for generating the model library for all the vertical profiles requires that the process be automated. Towards this end, the program AUTOCUP (automated generation of capacitance parameters) has been developed. It generates all the interconnect capacitances and

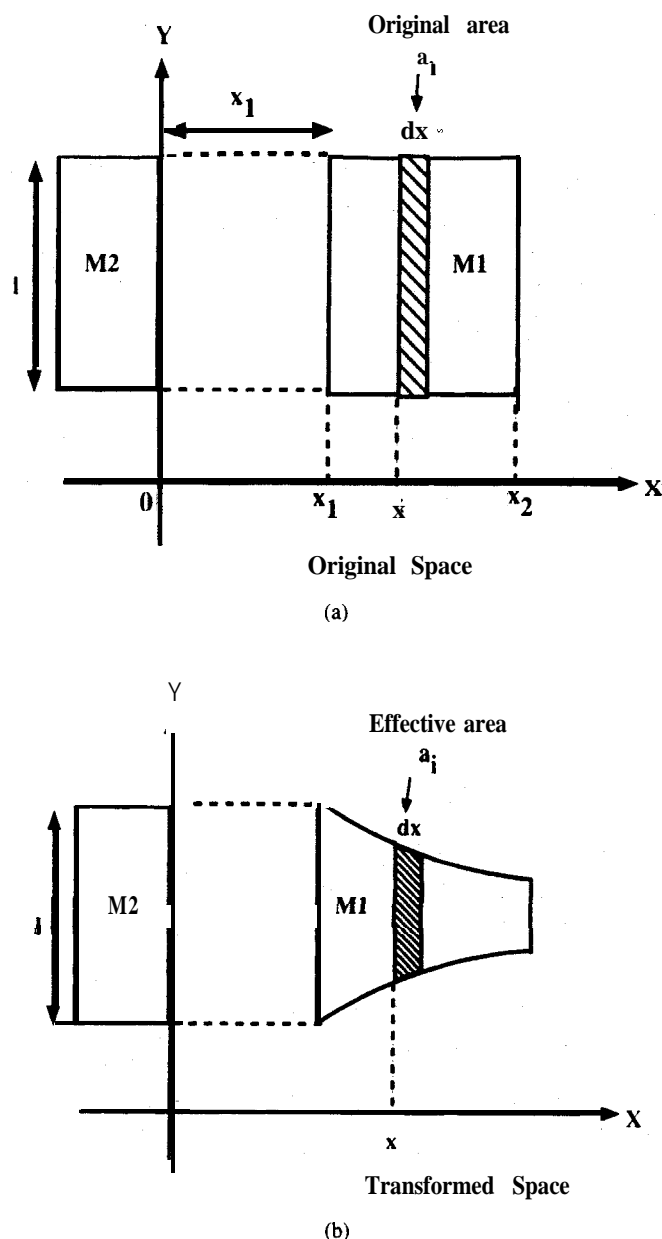


Fig. 10. Schematic illustrating the calculation of the fringing capacitance for two nonoverlapping conductors.

their coefficients required for CUP using the following three steps.

Step Z—As a first step, the information for simulating specific geometries is read from a process file. This file contains relevant process information such as conducting layers widths and thicknesses and spacings between the conducting layers and dielectric constants of the insulating layers. Based on this information, the simulation geometry is created for all vertical profiles of interest. For the lateral capacitance models, the simulation geometries are made functions of the spacing between conductors. For fringe capacitance models, the length of the fringing surface is varied.

Step II—The process file from step I is used to generate capacitances of the conductors using 2-D numerical simulation tool TDTL that is based on algorithms discussed in [7]. The

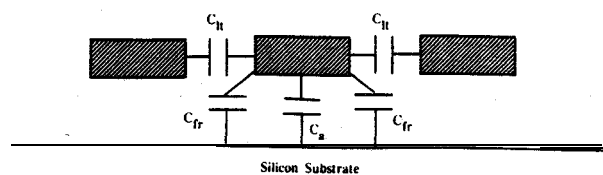


Fig. 11. Schematic showing the equivalent lumped capacitance model for two adjacent conductors.

output of TDTL is a matrix of capacitance coefficients such as the one shown in (3). For an N conductor system (plus ground plane), the size of this matrix is $N \times N$. The elements C_{jj} of the capacitance matrix is the self capacitance of the conductor j , i.e., the capacitance between the conductor and the reference plane

$$C_{jj} = C_{jref} + \sum_{k=1}^N C_{jk} \quad k \neq j; j = 1, 2, \dots, N \quad (14)$$

and the off-diagonal elements C_{jk} that exist between the conductors j, k is the so-called coupling capacitances between them.

The self-capacitance of a conductor represents the total capacitance of that conductor with all other conductors grounded. This form of input is typically required for timing and circuit simulation tools. These capacitance elements C_{jk} are then separated into their component parts (area, lateral, and fringe) as required. The separation into components indeed depends upon the full geometry of the conductors under consideration. For the example shown in Fig. 11, we have three conductors in the same plane. For this geometry, the TDTL capacitance matrix will have nine elements (C_{jk}, j and $k = 1, 2, 3$). The fringe capacitance C_{fr} for the central conductor to substrate is calculated as

$$C_{fr} = \frac{C_t - 2C_{lt} - wC_a}{2} \quad (15)$$

where w is the width of the central conductor.

Step III—Once the capacitance components are obtained for each geometry as a function of spacing, the capacitance data is fitted to the respective models, discussed in the previous section, using the nonlinear least squares optimization program OPTIMA [19]. This program allows redundancy in parameters to be easily determined with a confidence region evaluation technique.

The output of AUTOCUP is a file containing all the model coefficients and layer specifications required to completely characterize the multilevel VLSI circuit. The procedure allows rapid calculations of capacitance model parameters, once the necessary geometry is set up. For a case of $N = 7$ conducting layers, a total of approximately 600 TDTL simulations are required to generate these coefficients.

V. MODEL ACCURACY

An important feature of the capacitance extraction methodology in CUP is the use of geometric transformations that are applied to analytical models derived for a wide variety

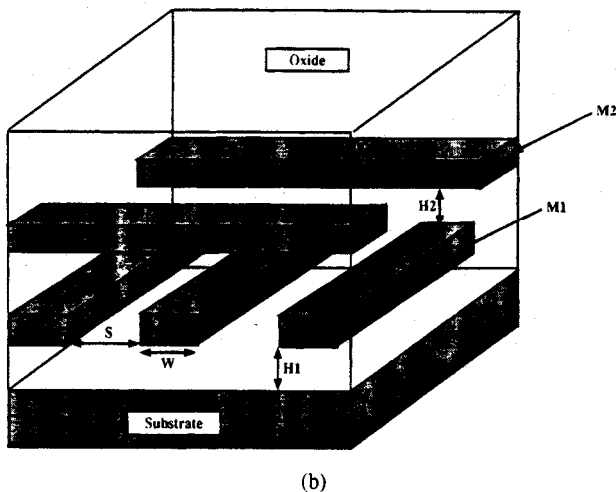
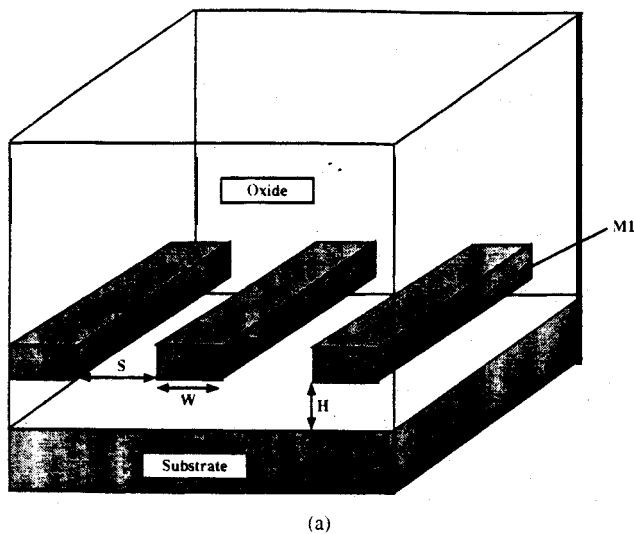


Fig. 12. 3-D structure used to compare CUP extraction with accurate numerical simulation. (a) Comb structure. (b) Crossover structure.

of geometries. These transformations effectively allow the computation of 3-D capacitances from 2-D analytical models. To verify the accuracy of the models, a comparison of CUP extracted capacitances with 3-D simulated capacitances is performed. The 3-D simulations were based on a boundary value simulator similar to those reported in [9]. This comparison was carried out for two geometries shown in Fig. 12. The first geometry (Fig. 12(a)) is a conductor comb over substrate (Case A), while the second geometry (case B) shown in Fig. 12(b) is the classical crossover structure widely used as a benchmark for capacitance comparison. The results in Table I are for the central conductor in the array for Case A and for the central conductor in the lower conductor array for Case B.

The simulated results are within 10% of the CUP extracted numbers. The CUP extractions have also been compared with measured results. Measurements were made on test structures that consist of combs of conductors over silicon substrate with different spacing between conductors. After careful subtraction of the parasitics due to pads and lead capacitances, the coupling capacitances for a wide variety of these test structures

TABLE I
COMPARISON BETWEEN 3-D SIMULATION AND CUP
EXTRACTION FOR LINE CAPACITANCES SHOWN IN FIG. 12

	Self Capacitance C_{11} (pF)		Lateral Capacitance C_{12} (pF)	
	3-D Simulation	CUP	3-D Simulation	CUP
CASE A	2.57×10^{-5}	2.43×10^{-5}	8.53×10^{-4}	9.0×10^{-4}
CASE B	3.20×10^{-5}	2.70×10^{-5}	1.82×10^{-4}	1.34×10^{-4}

TABLE II
COMPARISON BETWEEN MEASUREMENT AND CUP
EXTRACTION FOR THE LATERAL CAPACITANCE—Case A

Spacing μm	CUP extracted	Measured value
0.75	$5.45 \times 10^{-5} \text{ pF}$	$5.5 - 5.78 \times 10^{-5} \text{ pF}$
1.5	$3.45 \times 10^{-5} \text{ pF}$	$3.49 - 3.73 \times 10^{-5} \text{ pF}$

were found to be within 10% of the CUP extracted numbers. Measurements were performed using an HP4275 at 1 MHz. The results of the comparison for two such cases, comb structures with spacings of 0.75 and 1.5 μm is indicated in Table II.

The CUP extracted results agree with the measured values to within 10–15%.

VI. VALIDATION AND MODEL BUILDING

The model libraries for a multilevel circuit contain hundreds of capacitance coefficients. Verification of the results of capacitance extraction is therefore essential. This has to be performed on actual layout to obtain a realistic picture of the extracted capacitances on circuit performance. Moreover, validation serves two other essential purposes, those of ensuring error free and robust model libraries to the design community as well as serving as an indicator for tracking changes in layout capacitances due to changes in process parameters.

To satisfy the above requirements, our validation strategy is two-fold. In order to avoid difficulties in interpreting results that can arise with complex layout, a highly structured layout is used for one part of the validation. This layout is in the form of a series of conductors with varying geometry (space, width) and vertical profiles (for a multilevel layout, this can be a large but manageable number). This form of layout allows a rapid estimation of the impact of process changes on capacitance behavior and highlights model related problems and/or unphysical coefficients in the model library. It also serves as a design guide allowing comparison of trends in nodal capacitance across technologies. The validation procedure involves extraction of capacitance using a given model library on the test layout and retrieval and storage of the various components and total nodal capacitances in a database. The second layout contains sections of actual circuit designs. The use of these layouts gives a more realistic picture of how process changes impact the circuit nodal capacitance.

The ease of use of our methodology and its tight integration with existing CAD tools gives considerable flexibility to circuit designers and process engineers, who can customize

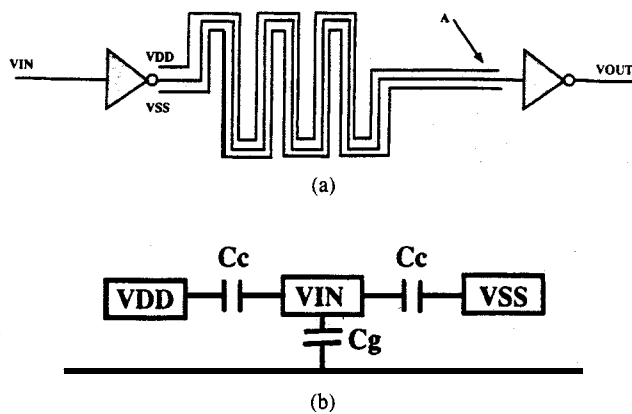


Fig. 13. Circuit schematic of a buffer circuit driving interconnect dominated load with adjacent VDD and VSS lines.

process files. As an example, it is possible to construct polynomial models of nodal capacitances as a function of process parameters of the form

$$C_j = \sum_{i=0}^N b_i p^i \quad (16)$$

where p^i are the process parameters, and b_i are coefficients to be determined. This enables the optimization of process parameters to obtain target capacitances that are closely optimized for speed, power, crosstalk, and other performance criteria. An example of the application of our methodology is applied to a buffer circuit driving a load dominated by interconnect capacitance, with adjacent V_{dd} and V_{ss} lines (see Fig. 13)).

A simple linear model of the ratio of the total lateral capacitance to the ground capacitance at node A (indicated in Fig. 13) was constructed as a function of the conductor thickness. This ratio is a good measure of how the signal carrying conductor can couple to adjacent lines during transients in a circuit. To ensure that the ratio of lateral capacitance to total capacitance $C_{lt}/C_{tot} \leq 20\%$, the linear model suggests the use of a target thickness of $t = 0.56 \mu\text{m}$, given a range of $0.45 \leq t \leq 0.75 \mu\text{m}$ in the conductor thickness.

Although the above example is a rather simple illustration, the procedure can be generalized to handle multiple objectives. As a first step, polynomial models of multiple objectives are constructed using well-known statistical design techniques. This is followed by optimization to obtain desired target responses, subject to constraints imposed on the process parameters such as conductor dimensions. This is compactly expressed as the following optimization problem:

$$\min \sum_{j=1}^N w_j [C_j - C_{p,j}] \quad (17)$$

subject to $x_l \leq x \leq x_u$ and C_p are different objective functions.

VII. CONCLUSION

In conclusion, we have reported an accurate and practical method of estimating interconnect capacitances for a given

circuit layout. The method allows extraction of the complete chip level capacitances at each node in the circuit. Accurate analytical models are developed for calculating capacitances between two conductors in the presence of other conductors using a 2-D capacitance simulator TDTL. These models and their coefficients for different vertical profiles are stored in the capacitance extraction tool CUP, which is coupled to the layout extractor HILEX. The comparisons of the models with the measured data, as well as 3-D simulations results, are also discussed.

ACKNOWLEDGMENT

The authors are thankful to H. Kumar, C. Richardson, A. Cave, and R. Cvijetic for their help in implementing the capacitance models in CUP and validation of the models at the circuit level.

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