Cancel PWM DAC ripple with analog subtraction

Stephen Woodward -November 28, 2017

19 Comments

Every PWM DAC design needs analog filtering to separate the desired PWM duty-cycle-proportional DC component from unwanted AC ripple. The simplest of these is the basic RC low-pass filter, which gives a peak-to-peak ripple amplitude (for the worst case of 50% PWM duty cycle, where T_{PWM} = PWM cycle time, and assuming RC > T_{PWM}) of:

$$V_{ripple} / V_{fullscale} = T_{PWM} / 4 \cdot RC$$

The obvious design tradeoff is that while any desired degree of ripple attenuation can be achieved by choosing a large enough RC product, settling time will correspondingly suffer. For example, if we (fairly logically) choose a definition for the settling band as equal to ripple amplitude, then…

$$T_{settle} = RC \cdot ln(V_{fullscale} / V_{ripple})$$

$$= T_{PWM} \cdot V_{fullscale} \cdot ln(V_{fullscale} / V_{ripple}) / (4 \cdot V_{ripple})$$

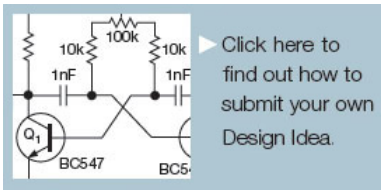
The consequences of this relationship can be illustrated by the 8-bit case:

$$Given: V_{ripple} / V_{fullscale} = 1/256; RC = 64 \cdot T_{PWM}$$

$$T_{settle} = 64 \cdot ln(256) \cdot T_{PWM} = 355 \cdot T_{PWM}$$

which, even for a fairly speedy 32 kHz (31µs T_{PWM}), predicts a positively *glacial* 11ms settling time.

Clearly, if settling time is a critical design parameter, we'll need to do better and find a less simplistic filtering scheme. The extreme possibilities that lie in this direction are illustrated by my previous DI, **Fast-settling synchronous-PWM-DAC filter has almost no ripple**.



But not every application that can't tolerate molasses-in-January $355 \cdot T_{PWM}$ settling times need or can justify such a complex filtering solution. The **Design Idea** presented here addresses these middle-of-the-road applications. As shown in **Figure 1**, it augments the basic R1/C1 low-pass with an inverter, R2, and C2, which combine to negate and subtract (most of) the undesired AC component from the wanted DC signal, leaving a relatively clean analog output with settling time much less than a simple RC filter.

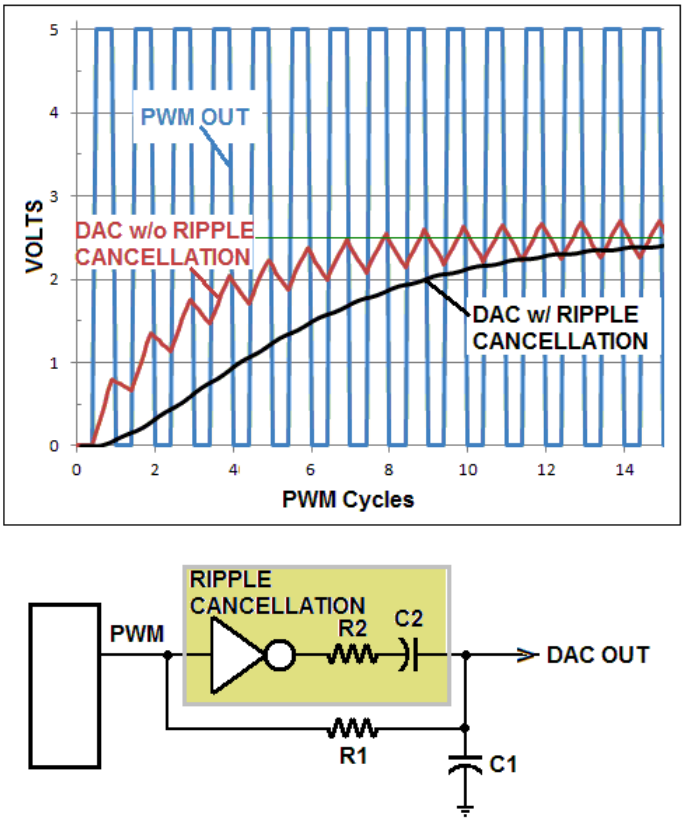


Figure 1 Waveforms & schematic of PWM DAC ripple canceller

But how pure is "relatively clean", and how fast is "much less"? Setting R2=R1 and C2=C1, the ripple and settling time figures for the new circuit are:

$$V_{ripple} / V_{fullscale} = (T_{PWM} / 4 \cdot RC)^2$$

$$T_{settle} = T_{PWM} \cdot ln(V_{fullscale} / V_{ripple}) \cdot (V_{fullscale} / 16 \cdot V_{ripple})^{1/2}$$

Referring again to the 8-bit case (illustrated graphically in Figure 1):

Given: $RC = 4 \cdot T_{PWM}$

$$T_{settle} = 22 \cdot T_{PWM} = 0.69 \text{ ms}$$

with a 32 kHz cycle, it's 16 times faster, with a squared ripple-amplitude ratio!

For many applications, this represents a very worthwhile tradeoff between a modest increase in circuit complexity and a significant increase in PWM DAC performance.

*—**W. Stephen Woodward** is one of EDN's most prolific and innovative Design Ideas authors, with dozens of contributions to his credit.*

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19 Comments

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ReAlAl

Very interesting, especially for microcontroller with complementary outputs on PWM.
Thanks!

Dec 8, 2017 5:53 AM EST

0 | 0 Reply

Al Grasso

I think the circuit proposed, within the boundary conditions stated in the narrative by the author, is perfect. I would like to add a small suggestion and that is to replace the single term negative integrator with a two-terms op-amp that adds a degree of differentiation to speed-up the time response. In that way it may be possible to match the original rise-time of the ripple and reduce even more the residual.
I am retired now and have no access to a lab else I would love to test it out.

Dec 7, 2017 4:13 PM EST

0 | 0 Reply

rydel0

But well, its a simple solution without opamp's, that's why it will be interesting. But I'm maybe wrong ? We have to Spice it.

Dec 5, 2017 6:33 PM EST

0 | 0 Reply

rydel0

A double T or a Wien bridge will do the same think I guess, eliminating the fondamental...

Dec 5, 2017 6:10 PM EST

0 | 0 Reply

WStephenWoodward

Wien bridge? With or without the traditional lightbulb?

Sorry. Couldn't resist.

Dec 5, 2017 6:37 PM EST

0 | 0 Reply

WStephenWoodward

I agree with both Brian and Dave that there's more than one way to defrock this particular feline. Thanks for your contributions.

However, please note that both your suggestions are not only compatible with each other, but can also be combined with my analog subtraction DI to get the ripple-reducing benefits of any two or all three.

Dec 5, 2017 4:38 PM EST

0 | 0 Reply

Brian park

There is a simpler way! (following explanation is for 8-bit PWM). The secret is to manipulate the order of the (PWM period x 2^8) so the power output of the "PWM" is pushed higher in frequency. You do this by writing the PWM generator in software (routine in assembly requires 9-10 instructions per iteration and 256 byte table). This requires a 256 byte bit-reverse table. In software, you have 8-bit counter running at PWM frequency x 2^8). This value is put in index to read from table. This result is bitwise ANDed with 8-bit amplitude. If result is zero, you write zero to port, else write 1. This goes to conventional RC filter, but highest power is at PWM period x 128. (Each bit lower has frequency half, but also power 1/4th the previous).
In comment below, some do this in FPGA. Why not put the "rate multiplier" circuit in FPGA?

Dec 5, 2017 3:29 PM EST

0 | 0 Reply

undertalk

But what are the contents of the indexed table? Do you have additional information on this technique? Thanks

Dec 7, 2017 6:27 AM EST

0 | 0 Reply

ReAlAl

Just bit-reversing (one assembly instruction for cortex-M3, no tables).
See "Synchronous 6-Bit Binary Rate Multiplier" internals
http://www.ti.com/lit/ds/symlink/sn7497.pdf

Dec 8, 2017 5:48 AM EST

0 | 0 Reply

DaveR1234

You can get the same or better response with a two or three stage RC filter.

Dec 5, 2017 2:13 PM EST

0 | 0 Reply

Mohan.Gurunathan

Hi, you state that the settling time is much less with the ripple cancellation circuit; however in the figure the black curve appears to take longer to settle to the final value, as compared to the curve with the higher ripple. Can you explain? Thanks.

Dec 5, 2017 12:05 PM EST

0 | 0 Reply

WStephenWoodward

The 355Tpwm settling time of the case of a single-pole RC filter with 1lsb of ripple isn't graphed. It wouldn't fit!

Dec 5, 2017 12:31 PM EST

0 | 0 Reply

Guillermo Jaquenod

Good solution, even better if PWM is generated by an FPGA, because the inverter can be synthezised into the FPGA and the cost/benefit is increased (only one R and one C to add). Thanks!

Dec 5, 2017 10:02 AM EST

0 | 0 Reply

StuMichaels

So, where's Figure 1? Tried with both Firefox and IE; just a caption. By the comments, there used to be a Figure 1 so where did it go?

Dec 4, 2017 3:50 PM EST

0 | 0 Reply

WStephenWoodward

Good question, Stu! Looks like the EDN web elves decided you could just rely on my oh-so "picturesque" text and your imagination.

Meanwhile, see if this works:
http://i68.tinypic.com/2gt9s82.jpg

Dec 4, 2017 5:00 PM EST

0 | 0 Reply

WStephenWoodward

Trying again: **https://imgur.com/a/YWvwb**

Dec 4, 2017 6:07 PM EST

0 | 0 Reply

fast3931

This is one of those, I wish I would have thought of that years ago circuits. I think the more you appreciate this circuit the more years you have spent hours mining for simple elegant solutions to problems you have faced with over your own career, trying to find simple elegant solutions such as this one.

Dec 3, 2017 2:57 AM EST

0 | 0 Reply

Pesky Varmint

I'm very fond of simple, clever methods like this. Especially since I've had to use analog PWM so often.

Nov 30, 2017 12:59 PM EST

0 | 0 Reply

relaxe

Thanks! That's a good one.

Nov 28, 2017 3:00 PM EST

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