A Short Introduction to

# CADENCE Virtuoso Front to Back Design Environment

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# 1 Introduction to the Introduction...

As it is intended to be just a short "getting started" guide, this document is quite incomplete (compared to the official documentation) and due to the little time I had to write it... well, it surely isn't free from errors.

This document refers to the `5.10.41`-release of the CADENCE Virtuoso Front to Back Design Environment (which will be referred to as CADENCE throughout the document). In some cases problems might occur when following the instructions in here using an older version.

# 2 The CIW

The CIW is CADENCEs main window (see Fig. 1). From this window all the tools that have been integrated into your design environment can be started – these can be found in the menu bar under `Tools`. From the menu bar entry `File` file operation commands can be executed – as usual. These commands will be explained later on.

Furthermore, the CIW shows some useful information such as the name and path of the session log file (on the window-top), the name of the used design kit (in the lower left corner), and – very improtant – the log file information itself is displayed.

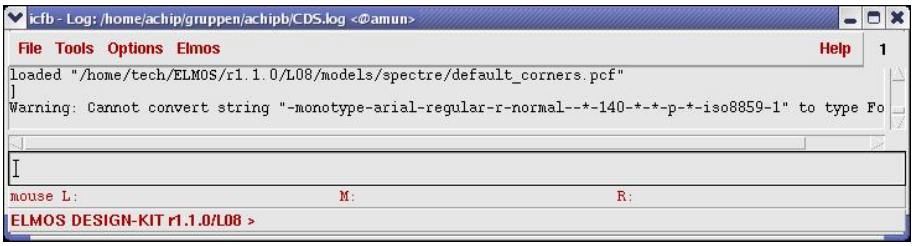


Figure 1: The CIW

# 3 Libraries in CADENCE – the Library Manager

The design data in CADENCE is organized in libraries, which contain so-called cells. Each cell has at least one, but most likely a multitude of cell views. The tool used to create and organize this data structure is the library manager (to start the library manager click `Tools` → `Library Manager...` in the CIW).

The library manager window (Fig. 2) shows the corresponding sections `Library`, `Cell` and `View`. The additional section `Category` can be activated via the checkbox on the top. These categories are another, further means for organizing the design / project data. The checkbox `Show Files` switches the representation of the sections `Cell` and `View`.

**Task: Create a new library**.
Click `File` → `New` → `Library`. In the following dialog (Fig. 3) enter the name

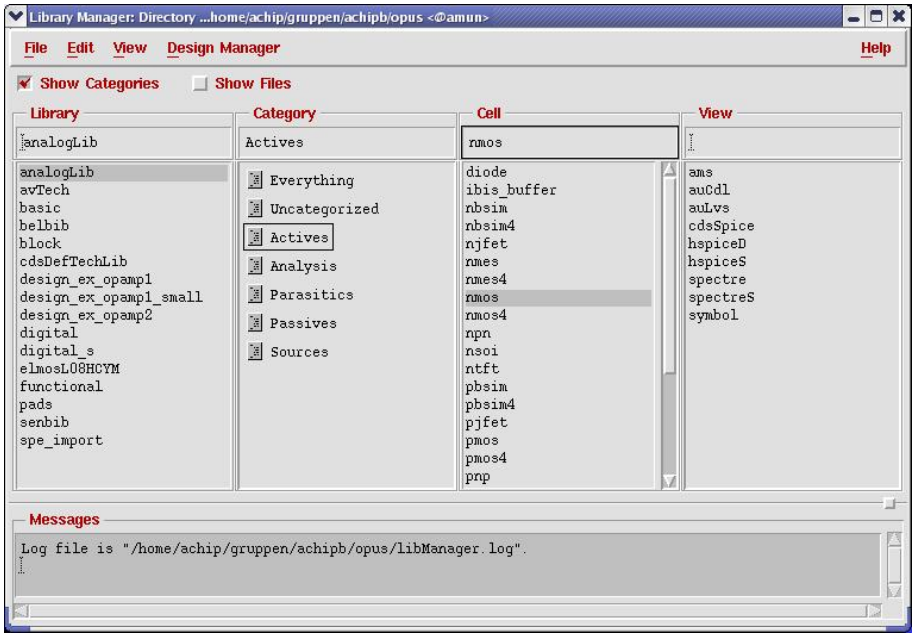


Figure 2: The Library Manager

of the new library in the field `Name`. The path, where the new library is saved can also be changed (field: `Directory`). Press `OK`.


Figure 3: Creating a new library – step 1: Naming the library

The new library should be attached to a technology file (Fig. 4). Choose `Attach to an existing tech file` (you might not want to do this in other cases, but

regarding the following tasks, you should do in this...).


Figure 4: Creating a new library – step 2: Attaching to a tech file

Now the tech file has to be specified. Choose `SGB25_dev` from the pull down menu "Technology Library".


Figure 5: Creating a new library – step 3: Choosing a tech file

Press `OK`. Finished.

# 4 Creating and Editing Schematics

The next step is to generate a schematic representation of the circuit you want to simulation, layout, manufacture. The tool to do this is the schematic composer (Fig. 6). On the left side of the schematic composer windows, there is an icon bar with the most important commands. These commands (and lots of others, too) can also be found in the menu bar.

Here is a short list of short cuts. Although they are the same on most CADENCE installations (I think these are the standard settings in some kind of "bindkey" setup file...), there is no guarantee that they will work always and everywhere.

- w – place wire
- s – snap wire
- i – place instance
- c – copy

- m – move
- r – rotate
- q – open the "Edit Object Properties" dialog (click on an instance and press "q")
- F3 – toggles a settings menu for the current action (like copy etc.)

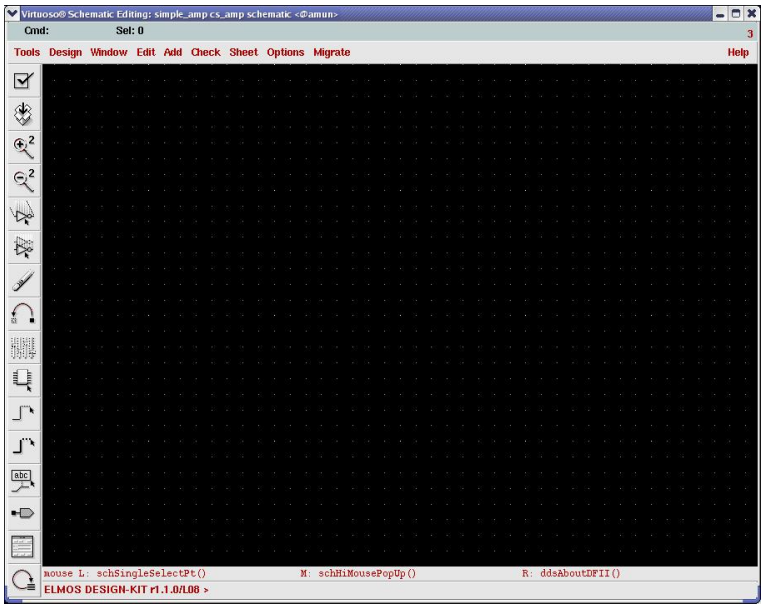


Figure 6: Schematic Editor

**Task: Create a new cell with schematic cell view.**
Click `File` → `New` → `Cell View...` in the library manager. The "Create New File" dialog (Fig. 7) opens. Choose the library you want to create the cell in and give it a name. Choose "Composer-Schematic" as tool. Press `OK`. The schematic composer window opens.

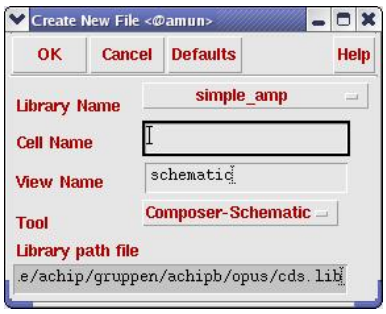


Figure 7: Creating a new schematic – The "Create New File" dialog

Now place a MOSFET and a resistor to form a common source stage. Press `i` (for instance), click `Browse...` in the next dialog ("Add Instance" dialog, see Fig. 8) and select the `nmos` cell, cellview: symbol from the `SGB25_dev` library. Set the instance parameters (in the case of a MOSFET these are at least the width and the length of the device). The order of magnitude of values in CADENCE is specified by a postfix notation; if the device width shall be $W = 10\mu m$, enter `10u M` in the corresponding field.

- G – giga – $\times 10^{9}$
- M – mega – $\times 10^{6}$
- k – kilo – $\times 10^{3}$
- m – milli – $\times 10^{-3}$
- u – micro – $\times 10^{-6}$
- n – nano – $\times 10^{-9}$
- p – pico – $\times 10^{-12}$
- f – femto – $\times 10^{-15}$

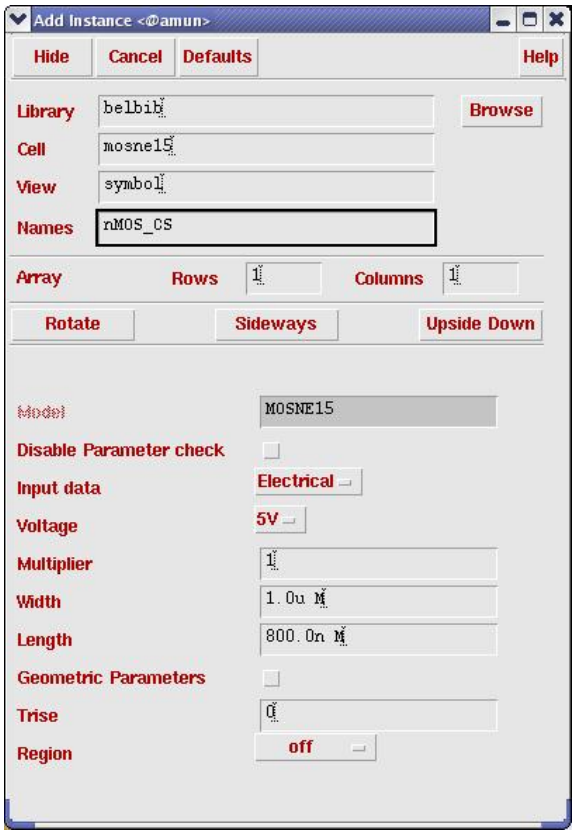


Figure 8: Add a new instance...

Variable device parameters can also be used. Place a resistor (from `SGB25_dev` / `rhigh`) and enter "R_Load" as resistance value.

Now, pins have to be placed. Pins allow to use a circuit as a subcircuit in a larger system. They are the interface for connecting the circuit in a higher level of a hierarchical design. Press `p` (to create pin). All the names for the pins needed can be entered in the field "Pin Names" in a line separated by a space. Each click in the schematic window places a pin; the name is the always the next one from the line entered in the "Pin Names" field.

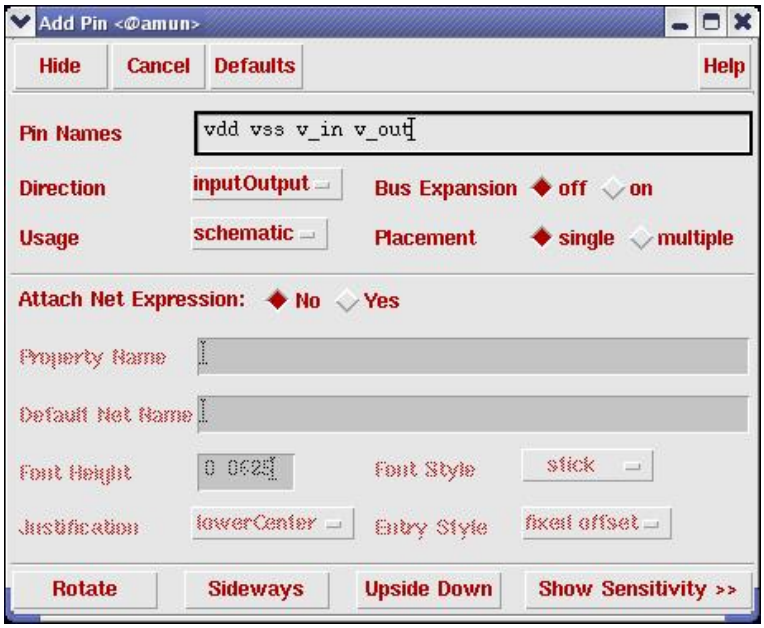


Figure 9: Create pin dialog

Now add the wires to the circuit. When finished the schematic diagram should look similar to the one shown in Fig. 10.

# 5 Creating and Editing Symbols

Now a symbol view for the circuit must be created. For symbol creation/editing also the composer tool is used. A symbol view can be instantiated in another schematic view. Connections to the subcircuit schematic use the pins created at the end of the last section.

A symbol can be created by just invoking the symbol composer (see "Create a new cell..." task in last section) and doing all the work all alone, or by generating the symbol from the schematic cell view.

**Task: Create a symbol view from the schematic cell view**. Click `Design` → `Create Cellview` → `From Cellview...` in the schematic composer menu bar. The "Cellview from Cellview" dialog opens, just press "OK", the settings should be correct. In the following "Symbol Generation Options"

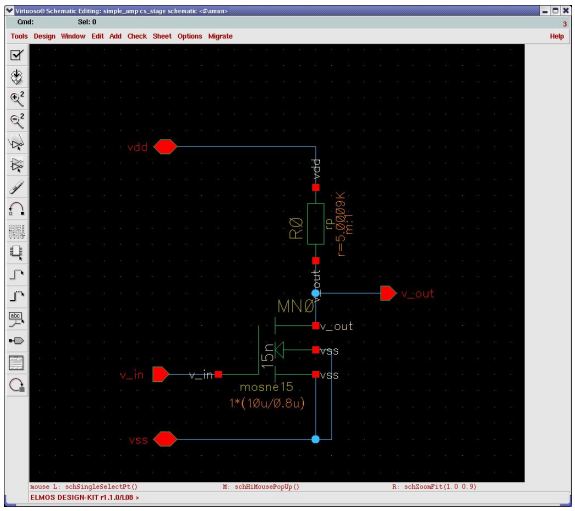


Figure 10: The finished CS amplifier

dialog, the placing of the pins and some pin properties can be edited. Again, just press "OK".

Now the symbol composer window opens, containing a preliminary symbol. Edit the symbol! After finishing your symbol, save it (press the Save button – it is the first one in the icon bar).

– A more detailed description migth follow... —

# 6 Performing Simulations – the Analog Environment

The circuit simulator in CADENCE is SPECTRE (simulators from other companies might also be integrated in your design environment, but SPECTRE is the standard simulator). The communication with SPECTRE is performed via the analog environment tool. In this tool, all settings for a successful simulation are made (like assignment of values to your design variables, simulation type setup, selection of signals – voltages and currents – to be observed, ...). The analog environment generates an ocean script which starts SPECTRE.

Two other tools are very necessary for the circuit analysis: the waveform viewer `Waveform` and the calculator. `Waveform` is for used for displaying the selected signals. The calculator offers a lot of functions like FFT, derivation of waveforms etc. These will be explained in the subsequent sections whe they are used.

The circuit schematic from the last section is quite useless to SPECTRE. Input signals as well as supply voltages, a defined ground and a load. Consequently, some kind of testbench has to be created. The separation of a simulation setup into a "circuit under test" and a testbench, that instanciates this circuit is a good methodology insofar, as idealized sources / elements supplied by a

simulation environment should not be used in a circuit that shall be realized in silicon.

**Task:** **Create a testbench**. Create a new schematic in your library for the testbench. Instanciate your "circuit under test" (the common source amplifier). The elements for the testbench can be found in the library `analogLib`. This library is supplied with CADENCE. Use the following elements:

| | element name | values / settings |
|---|---|---|
| power supply | `vdc` | DC voltage = vdd |
| input signal | `vdc` | DC voltage = vin |
| ground | `gnd` | – |
| load capacitor | `cap` | Capacitance = CLoad |

Table 1: Testbench elements from library `analogLib`

When you are finished, press the Check And Save button. The testbench should look like the one in Fig. 11:

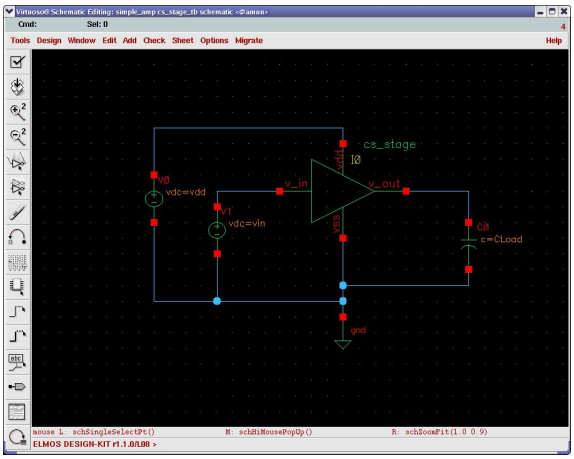


Figure 11: DC Testbench

## 6.1 DC Simulation

The DC Simulation calculates the DC steady state of a circuit. The DC steady state can be calculated for a sweep over temperature, a component parameter, a design variable. It is the first simulation to perform when analyzing a circuit with CADENCE. Using this simulation, one check whether the chosen operating point of the circuit is correct or not.

**Task:** **Set up the DC simulation**.

Start the analog environment (Fig. 12) from the schematic window (of the testbench schmatic; `Tools` → `Analog Environment`).

To set up the DC simulation

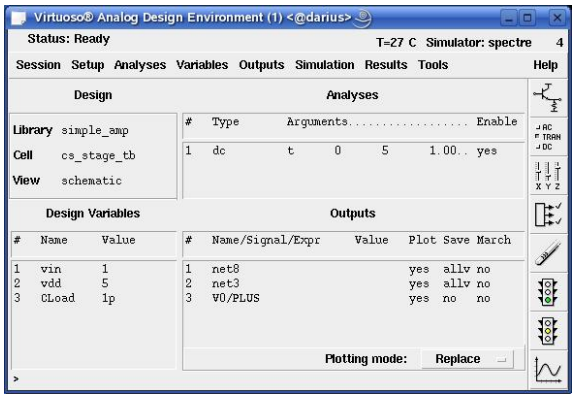


Figure 12: The analog environment window

- load the variables: `Variables` → `Copy From Cellview`,
- initialize the variables: press the "Edit Variables..." button on the right side and assign the values,
- choose an analysis: press the "Choose Analysis..." button; in the following dialog (see Fig. 13)
  - choose "dc",
  - activate "Save DC Operating Point",
  - as sweep variable select "Design Variable"; press "Select Design Variable" → vin
  - as sweep range: Start = 0, Stop = <enter the value of vdd>
  - sweep type: linear, step size: well, just enough, but not to many
  - press "OK"
- select the voltages/currents to be plotted: `Outputs` → `To Be Plotted` → `Select On Schematic`; clicking on a wire in the schematic adds the corresponding voltage to the output to be plotted, clicking on an instance pin adds the current into the pin.

Now the simulation is set up. To start it press the green traffic light button on the icon bar: Netlist And Run!

Since you already selected signals to display, right after the simulator finished the `Waveform` will pop up (Fig. 14). Now it is useful to determine an operating point for the AC Simulation of the amplifier. Press the key "A" or "B" (still in the `Waveform` window...) and a cross marker appears. Shift the marker to the point, where the output voltage is $\frac{vdd}{2}$ for example. Memorize the input voltage value.

**A short note on simulation results.** There are some other ways to access the simulation results. In general, one can always use the direct plot form (`Results` → `Direct Plot` → `Main Form...` from the analog environment window). Another possibility is using the calculator. The commands to

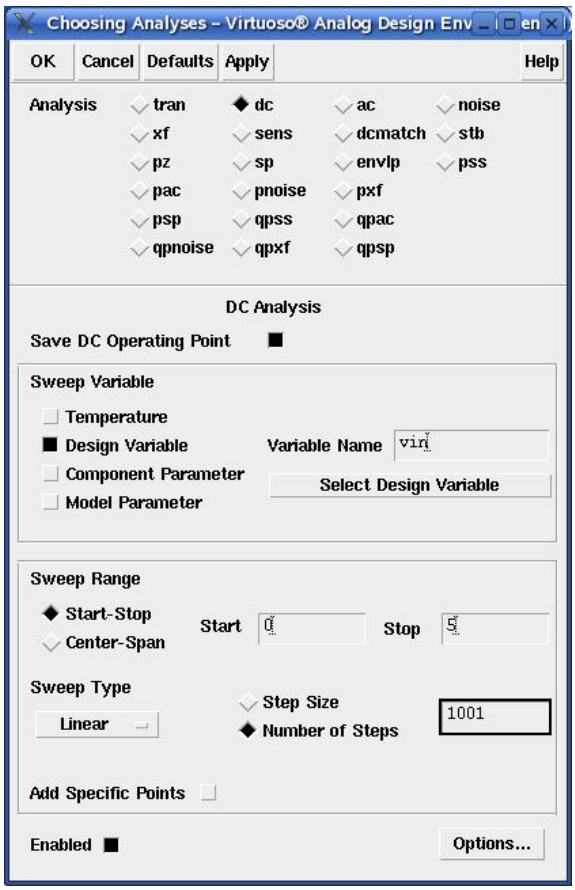


Figure 13: Setting up the DC simulation

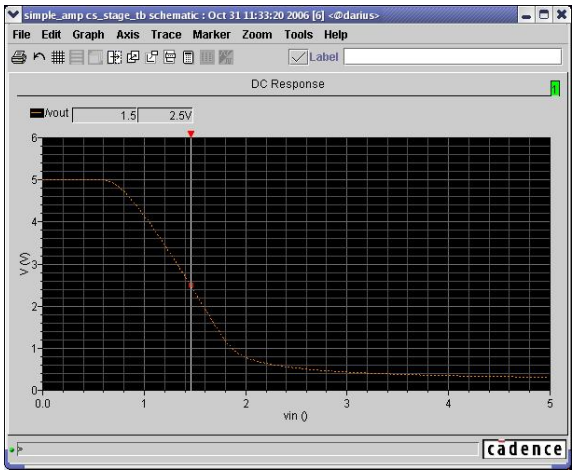


Figure 14: Result of the DC simulation

plot a signal can directly be entered here as text (you must of course know the correct syntax) or via the appropriate buttons.

**Task: Display results using the calculator; Save result equations to your simulation setup.**

Start the calculator: `Tools` → `Calculator...`. In the calculator window (Fig. 15) select the `swept_dc` tab (you just did a dc sweep) and click the `vs` radiobutton. Now a net has to be selected from the schematic. Pick the output net of the amplifier. The following text appears in the calculator's command line: `VS("/<name of the net>")`. By clicking the small plot button, you can display this nets voltage.

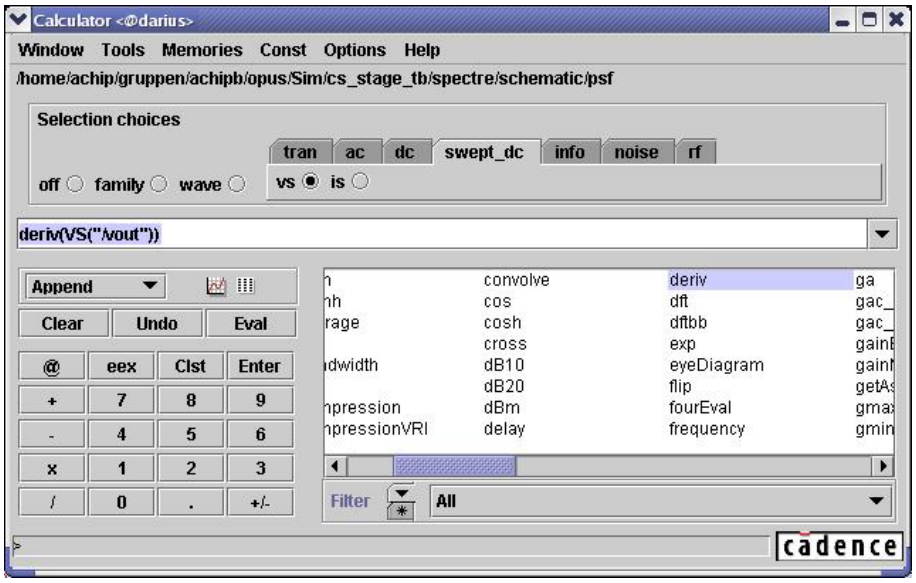


Figure 15: The calculator

To add this expression to the simulation setup in the analog environment, switch to the latter, press `Setup Outputs...` → `Get Expression`. Add a name – "output voltage" for example – and press the "add" button.

The next step is to calculate and plot the DC gain of the amplifier. In the calculator window press "Clear" and then again `swept_dc` → `vs` and select the output net. Now choose the derivation function `deriv` from the big list. The command line should display: `deriv(VS("/<name of the net>"))`. Add the function to the analog environment.

To save the simulation setup for later sessions; use `Session` → `Save State...`. Start the simulation again. The Waveformwindow now shows the results for this two expressions:

## 6.2 Parametric Sweeps

The parametric sweep allows to start multiple runs of the activated simulations sweeping a design parameter. This is useful for example, if you want to simulate the DC output characteristic $I_D = f(V_{DS})$ of a FET.

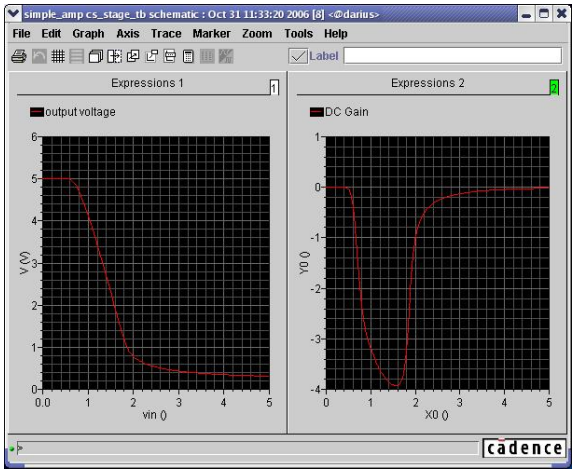


Figure 16: Results for the added exprssions

**Task: Perform a parametric sweep.**

The parameter is "R_Load". Start the parametric sweep tool: `Tools` → `Parametric Analysis...` (Fig. 17). Take the following settings:

- `Variable Name`: R_Load
- `From`: 5k
- `From`: 100k
- `Step Control`: Linear Steps
- `Step Size`: 5k

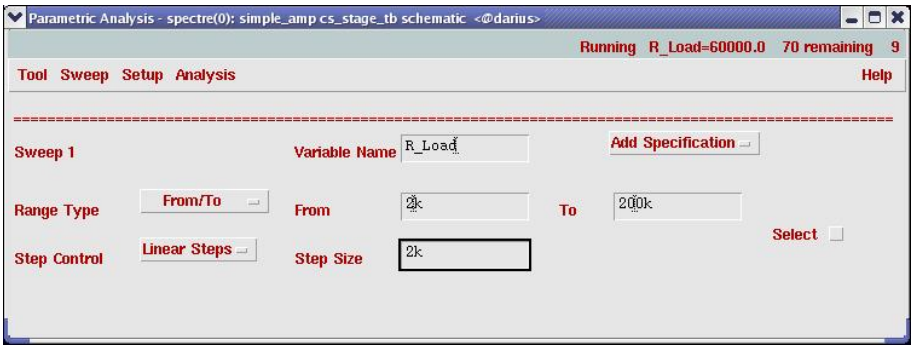


Figure 17: The parametric analysis tool

Start the simulation with: `Analysis` → `Start`. The result is a parametric plot of the two expressions you entered before. Close the Waveformwindow. Open the "Setup Outputs..." dialog (analog environment) and add an expression to calculate the maximum gain: `ymin(deriv(VS("/`*<name of the net>*`")))`. It's "ymin()" because the DC gain is negative. Replot the simulation results (use the "Plot Outputs" button...). See the results in Fig. 18

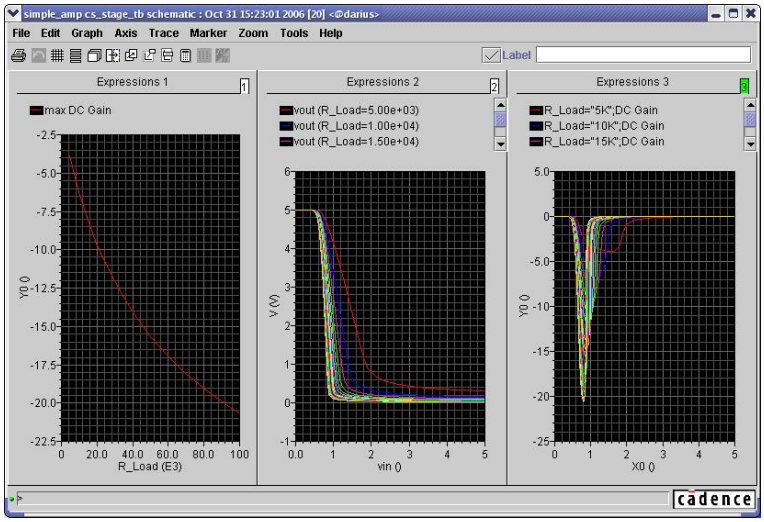


Figure 18: Result of the parametric sweep

## 6.3 AC Simulation

The AC simulation is used to calculate the frequency behavior of a circuit. The circuit is linearized in the operating point and treated as a linear network. This linearization excludes the amplitude dependency of the nonlinear devices. This results in an amplifier gain, which is the same for an input amplitude of $1mV$ and let's say $1000V$ for example. This fact should be kept in mind when using the AC simulation.

**Task: Perform an AC simulation of the CS amplifier.**

First, a value for the small signal input voltage must be entered: select the input voltage source in your test bench, press "q" and enter a reasonable value into the field "AC Magnitude". Save the schematic (→ "Check and Save"). Set up the AC simulation:

- assign the correct input dc value for your operating point,
- choose an analysis: press the "Choose Analysis..." button; in the following dialog
  - choose "ac",
  - as sweep variable select "Frequency"
  - as sweep range: Start = 1, Stop = 10G
  - sweep type: Logarithmic, Points Per Decade = 100
  - press "OK"

Start the simulation. After the simulation is finished, click `Results` → `Direct Plot` → `AC Gain & Phase`. Now, first select the output node and then the input node of the amplifier from your test bench schematic. The Waveformwindow displays Gain magnitude (dB) and phase.

## 6.4 Small Signal Noise Analysis

Based on a preceding AC simulation this analysis simulates the noise behavior of a circuit.

**Task: Perform an AC simulation of the CS amplifier.**
Set up the Small Signal Noise simulation:

- choose an analysis: press the "Choose Analysis..." button; in the following dialog
- choose "noise",
- as sweep variable select "Frequency"
- as sweep range: Start = 1, Stop = 10G
- sweep type: Logarithmic, Points Per Decade = 100
- Output Noise: Voltage
  - Positive Output Node: `Select` the output net of the amplifier
  - Negative Output Node: `Select` the ground net
- Input Noise: Voltage; `Select` the input voltage source in the test bench
- press "OK"

Start the simulation. After the simulation is finished, click `Results` → `Direct Plot` → `Squared Output noise`. The Waveformwindow displays Gain magnitude (dB) and phase. The results of the AC and the noise simulation are shown in Fig. 19

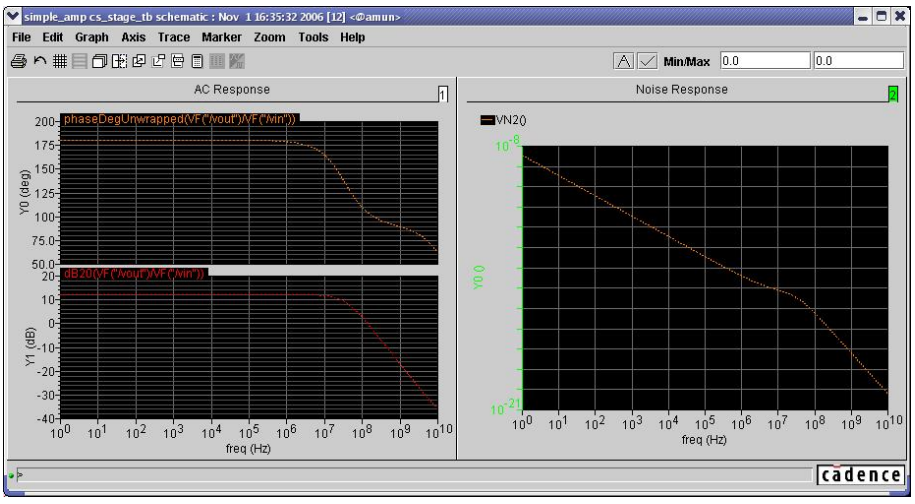


Figure 19: Results of the AC and the noise simulation

## 6.5 S-Parameter Simulation

t.b.d.

## 6.6 Transient Simulation

The transient simulation is a time domain simulation. In contrast to the AC simulation it does not linearize the circuit around an operating point. Nonlinearities – depending on the model exactness – are fully taken into account. The transient simulation is suitable to simulate the transient behavior (that's were the name come from) of a circuit going into a steady state after power up, for example.

**Task: Prepare & and perform an transient simulation of the CS amplifier.** First, the testbench has to be modified. A suitable signal source has to be chosen. Exchange the `vdc` source with a `vsin` source (also from the library `analogLib`). The settings for this source are:

- AC magnitude = 1
- DC voltage = `vin_dc`
- Amplitude = `v_amplitude`
- Frequency = `f_in`

Save the schematic and start the analog environment. Initialize the design variables:

- `vdd` = 5V
- `vin_dc` = 1.5V (in the case I chose – select the value you got from the preceding simulations)
- `v_amplitude` = 0.1V
- `f_in` = 1M
- `RLoad` = 5k

Set up the transient simulation: → `Choose Analysis...`:

- Analysis: tran
- Stop Time: 10u
- Accuracy Defaults: conservative

After pressing "OK", select the output node to be plotted. Start the simulation.

**Task: For homework :-)**

**1)** Do a parametric sweep of the transient simulation you just did over the input amplitude: `v_amplitude = 0.1 ... 1V` in 4 steps. You will see the nonlinear effects.

**2)** To quantify the nonlinearity, perform a FFT on the resulting waveforms. What do you observe?

## 6.7 Periodic Steady State (PSS) Simulation

t.b.d.

## 6.8 Nonlinear Noise Analysis

t.b.d.

## 6.9 Corner Simulation

Integrated circuits have to work over a wide range of process parameter deviations and operating conditions. Not only that they must not take any damage within that range, they also have to show a minimum performance. A powerful means to assure this is the corner simulation. Table 6.9 shows a set of common process/operating point corners. These are the "extreme" cases – other combinations of $V_{DD}$, $T$ and models are possible. and of interest.

| Corner Name | Temperature | Model | Supply |
|---|---|---|---|
| Worst Power (wp) | low ($0^o$... $-40^o$C, winter...siberian condition) | model.bcs | $V_{DD} + 10\%$ |
| Worst Speed (ws) | high ($100^o$...$120^o$C, desert condition) | model.wcs | $V_{DD} - 10\%$ |
| Typical Mean (tm) | normal ($27^o$C, room temperature) | model.typ | $V_{DD}$ |

Table 2: Process (model) and operating condition corners

The process corners are given indirectly via different transistor models. The models differ in parameter values which reflect the deviation in device processing.

To perform a corner simulation, the values given in table 6.9 have to be entered into the simulator. The corner simulation will be demonstrated using a two-stage operational amplifier. Figure 20 shows the testbench used to characterize the OPAMP. The interesting performance parameters are: gain, 3-dB frequency, unity gain frequency and phase margin. To get these values, AC simulations will be performed.

Start the analog environment. After setting up the AC simulation and perhaps adding signals and formulas, the parameters defining the process corners have to be set. The supply voltage is set in the according voltage source in the testbench. Click `Setup` → `Temperature` to change the simulation temperature. To change the models, click `Setup` → `Model Libraries...`. In the following dialog (Figure 21) the model files are listed. Select the MOSFET model file and adjust the model section tag in the model section field according to the names in table 6.9.

Figure 22 shows the OPAMP schematic. The results of the corner simulation have been added using the note text function.

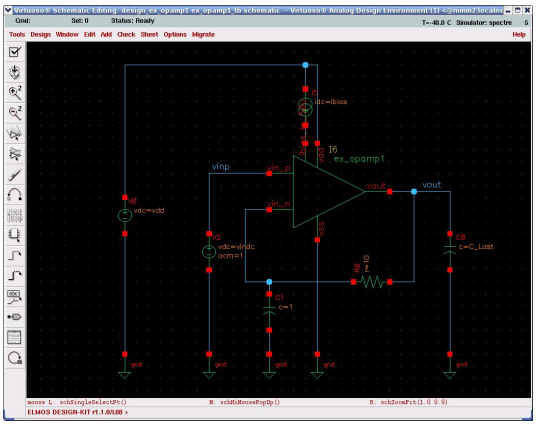


Figure 20: Testbench for OPAMP characterisation

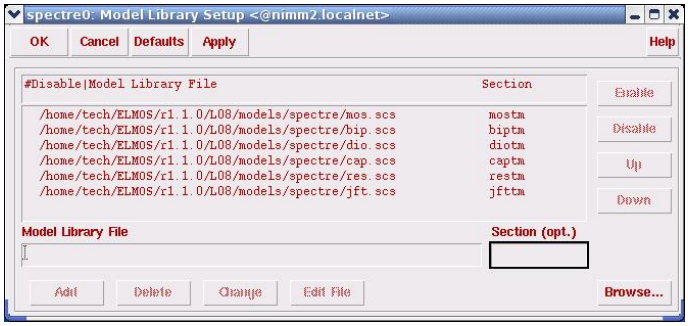


Figure 21: Model Library Setup

**Task: Prepare & and perform a corner simulation of the CS amplifier.** Take care: the DC operating point has to be adjusted for each corner! Summarize the important performance parameters and add them to the schematic using the note function.

# 7 Creating and Checking Layouts

## 7.1 Generating the Layout

Layouts are created using the Virtuoso Layout Editor. There are two ways creating a layout:

1. create a layout cellview and do all the layout work by yourself
2. use the `LayoutXL` tool

Using the second of these two options makes life a lot easier, as all instances in the layout view are created from the schematic view. Another advantage is the possibility to show the incomplete nets, i.e. the nets drawn in the schematic, that are not yet finished in the layout.

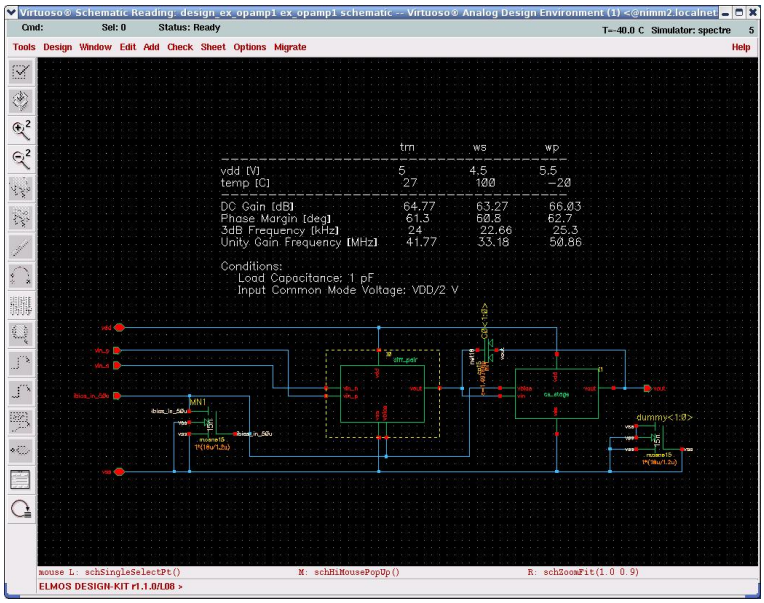


Figure 22: Schematic of the OPAMP including the results from the corner analysis

**Task: Draw the layout of the CS amplifier using `LayoutXL`.**

Open the schematic view of the amplifier. Select `Tools` → `Design Synthesis` → `Layout XL` and in the following dialog "Create New". Press "OK". In the "Create New File" dialog that follows, the correct values should already be set; check and press "OK" again. Now, the Virtuoso XL Layout Editing window opens. Select `Design` → `Gen Form Source...` – the dialog shown in Fig. 23 opens. The following settings should be made:

- Layout Generation: (these are the standard settings and should normally be like this)
  - I/O Pins: on
  - Instances: on
  - Boundary: on
- In the I/O Pins box the properties of the pins can be set/changed. Especially the pin layer should adapted. In the upper part of this box, click on the pull down menu below "Layer/Master" and change the value to one of the metal pinning layers: `MTL1 pn`, `MTL2 pn` or `MTL3 pn`. This will change the properties of all pins. Depending on the chosen pin layer, the signal and supply lines in the design have to end and will be connected via the correspnding metal layer.

  Choose `MTL1 pn` for the two supply lines (vdd and vss) and `MTL2 pn` for the input and output signal. Do this by selecting the corresponding line in the middle section and changing the "Layer/Master" property at the bottom of the I/O Pins box – using the bottom pull down menu changes

only the value of the selected pin. Press the "Update" button after each modification.

- Press the "Pin Label Options..." button and select "Layer Name: TXT" in the following dialog. You can also adapt the character heigth and the font, if you like. Press "OK".

When finished, press "OK" in the "Layout Generation Options" dialog.


Figure 23: The layout generation dialog

Now, the devices and pins placed in the schematic. Save the layout.

**Note:** To start Layout XL again after having closed the CADENCE session, open the layout view (one, that was created with Layout XL...) and select `Tools`

→ `Layout XL`. The schematic view opens and you are in Layout XL mode.

One might now want to change the appearance of the devices. For example, if the `rhigh` resistor consists of only one straight poly line, it is possible to add bends to get a more compact layout. Select the poly resistor and press "q". Switch to "Parameter" and select `Input Data` → `Layout`. Now enter a number greater than 1 in the "Segments" field and press "Apply". See, how the shape of the resistor changed.

Here are shortcuts of some important commands for layout editing/creation:

- p – create path: Creates a path in the selected layer. Specify the points of the path by left-clicking into the layout view. The path is finished with a double left-click.
- i – place instance
- c – copy: Creates a copy of the selected object. Rigth-clicking during copy rotates the object.
- m – move: Moves the selected object. Rigth-clicking during move rotates the object.
- s – stretch: Stretches an object. Behaves like the move command when one (or multiple) complete object(s) is/are selected. To stretch a path for instance, deselect all objects, press "s", click on the end of a path and modify its length by moving the mouse. Left-click to finish.
- d – delete: ...
- CTRL + d – deselect all
- q – open the "Edit Object Properties" dialog (click on an instance and press "q")
- o – create contact: Creates a contact between two wiring layers.
- k – place ruler
- SHIFT + f – display all layers
- F3 – toggles a settings menu for the current action (like copy etc.)

Place the devices to form a compact layout. To show the nets you still have to route, select `Connectivity` → `Show Incomplete Nets...` from the main menu of the layout window. Press "Select all" and then "OK".

Finish the Layout: Place two wires, each $5\mu m$ wide in `MTL1`, one on top of the layout, the other one at the bottom. These are the power supply lines. Place the resistor so that its one poly-`MTL1` contact is directly under the upper (`vdd`) supply line. This possible only if the number of segments of the resistor is odd. The bottom (`vss`) supply line should be placed on the source contact MOSFET. Place the `vdd`/`vss` pin on the supply lines and adjust the size – the pins should not overlap the metal. Connect the drain of the MOSFET to the resistor using `MTL1`; also place a contact `CON_MM` on this line. Adjust the size of the output pin an place it on the contact. The last step is to finish the input connection: press "p" (for path) and click on the left end of the MOSFET's gate.

Draw a piece of poly path, then press "F3". In the "Create Path" dialog select `Change To Layer` → `MTL1`. The next click in the layout creates a poly-`MTL1` contact and continues the path in the `MTL1` layer. Draw a little line and then change to `MTL2` using the same method. Place and adjust the input pin.

Save the layout. It should now look similar to the one shown in Fig. 24.

## 7.2 DRC – the design rule check

The design rule check (DRC) examines the placement of the objects in the layout. The DRC checks whether geometrical rules like minimum/maximum distances and widths of polygons are maintained in order to guarantee a "fault-free" manufactoring of the IC.

### DRC using DIVA

Start the DIVA DRC from your layout window via `Verify` → `DRC...` and make the following settings (see Fig. 25):

- Checking Method: flat
- Checking Limit: full
- Rules File: divaDRC.rul
- Rules Library: XXXX(push the button...)
- Machine: local

Start the DRC (press "OK"). Watch the the CIW – when the DRC is finished the error messages are displayed here.

Fix the errors! Error markers will be shown in the layout view right after the DRC finished. Important tools can be found in the menu `Verify` → `Markers`.

## 7.3 LVS – layout versus schematic

The LVS checks if the layout corresponds to the schematic and so the IC will work like intended.

### LVS using DIVA

Before starting the LVS an extracted view has to be generated from the layout view. Open the "Extractor" window (`Verify` → `Extract...`) and set up the extract:

- Extract Method: flat
- Join Nets With Same Name: no (this is used when there are multiple metal strips that have the same name and are intended to be connected to the same net one level up the hierarchy)
- View Names: Extracted: extracted
- Rules File: divaEXT.rul
- Rules Library: XXXX(push the button...)

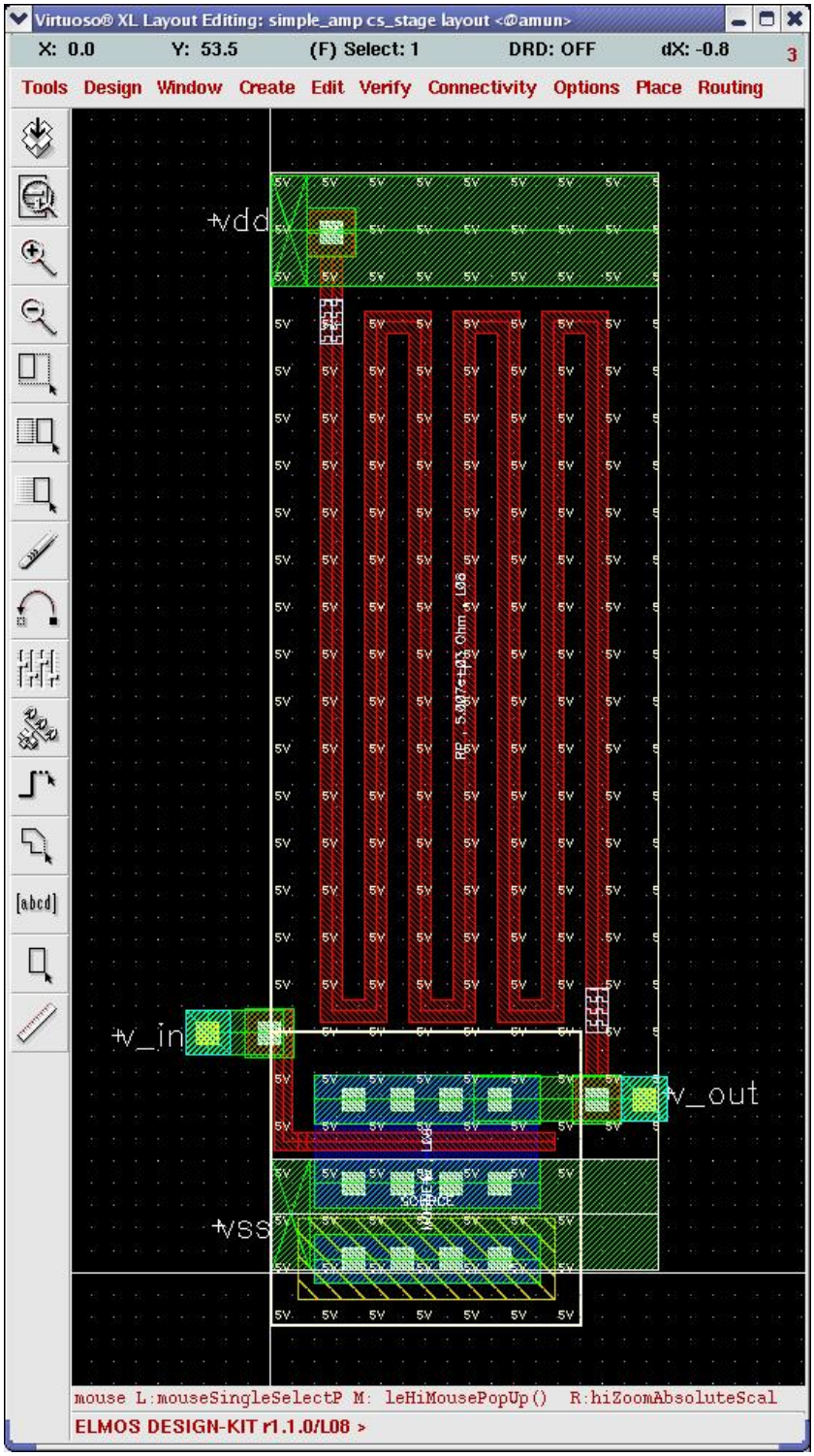


Figure 24: Layout of the CS amplifier

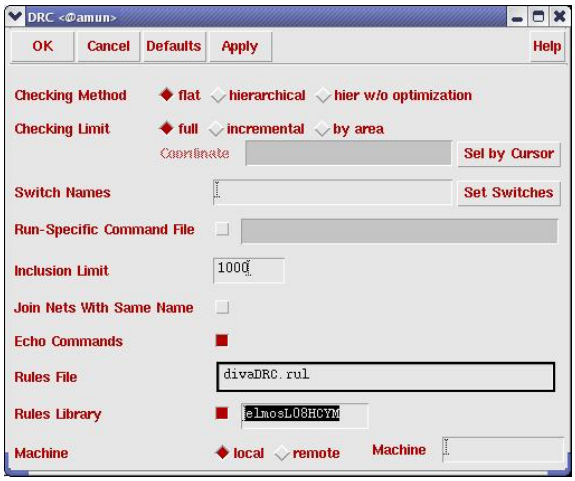


Figure 25: The DRC window...

- Machine: local

Press "OK".

After the extractor finished start the DIVA LVS from your layout window via `Verify` → `LVS...` and make the settings shown in Fig. 26. Start the LVS by clicking "Run". After the job has finished, press "Output" to see the results. The output file shows information about the errors. If everything is all right, you will find the line: "The net-lists match". Find and fix the errors!

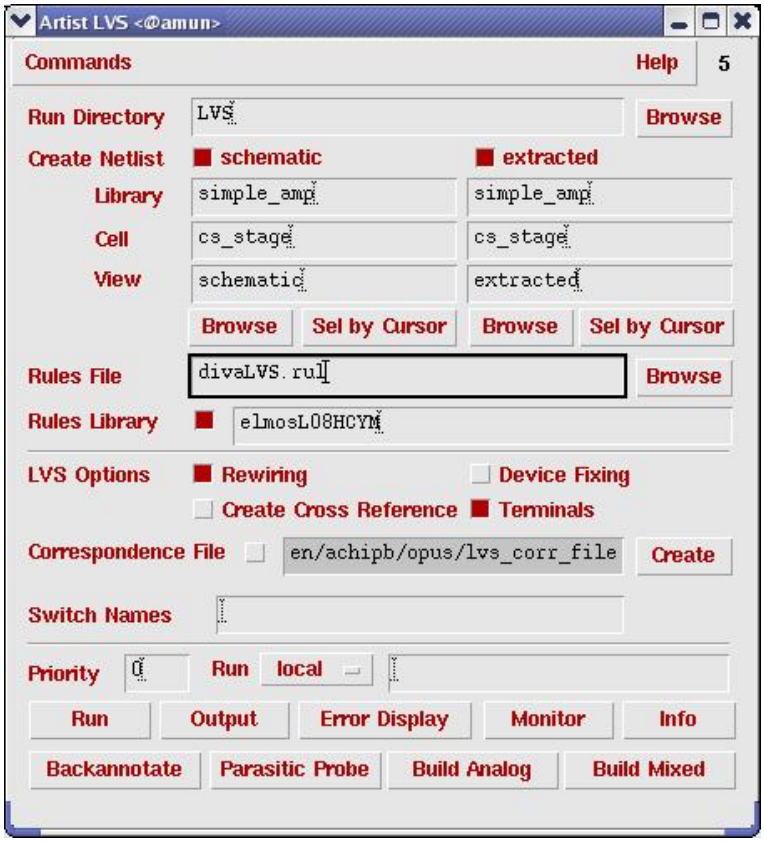


Figure 26: DIVA LVS Setup