Cadence Flow (Virtuoso) for a CMOS Inverter Design

User name: student password: student

Once you will login successfully, open a terminal (right click -> Open Terminal) and then type the following to start the cadence :

[student@DOE37 ~]$ tcsh
[student@DOE37 ~]$ ihph1m4

Virtuoso Schematic Design:

[Technology : BiCMOS - 0.25 micron, Single poly, 4 Metal]

Once the cadence starts successfully, the cadence environment will open as shown in Fig 1.

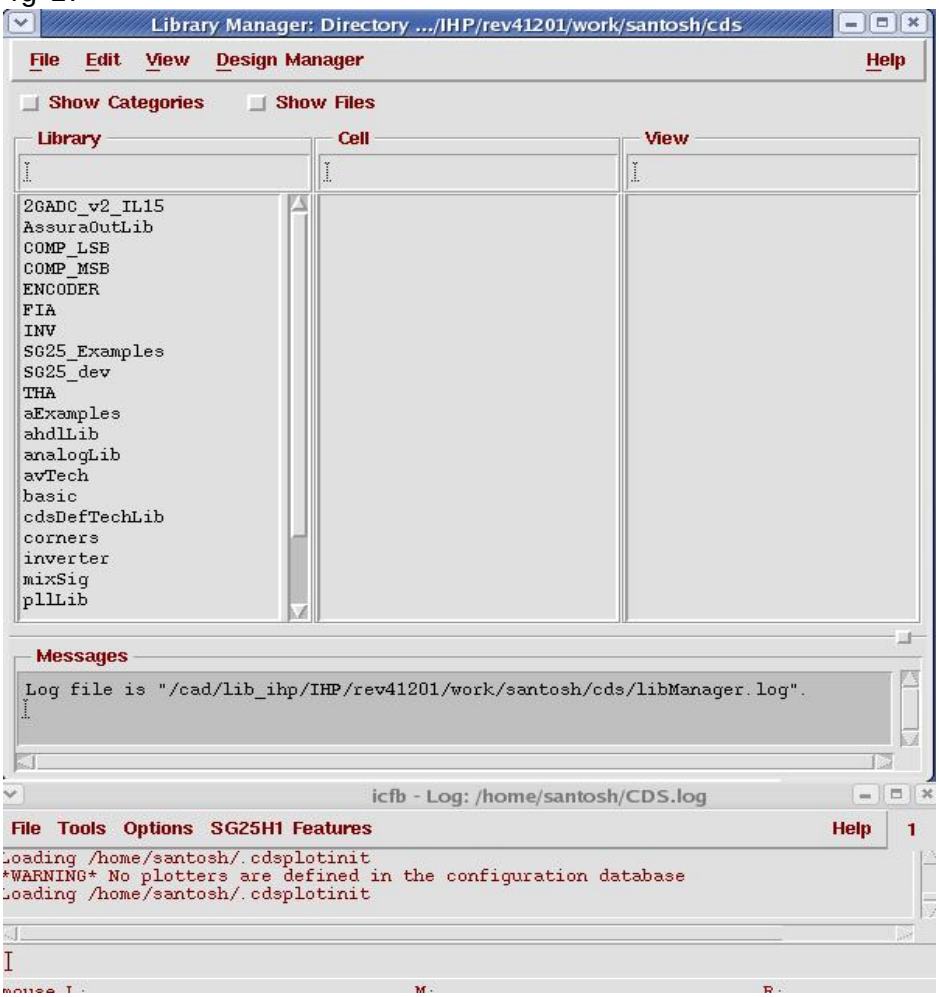

Fig 1.

Go to Library manager, file->New->Library. A new library window will open as shown in Fig 2.

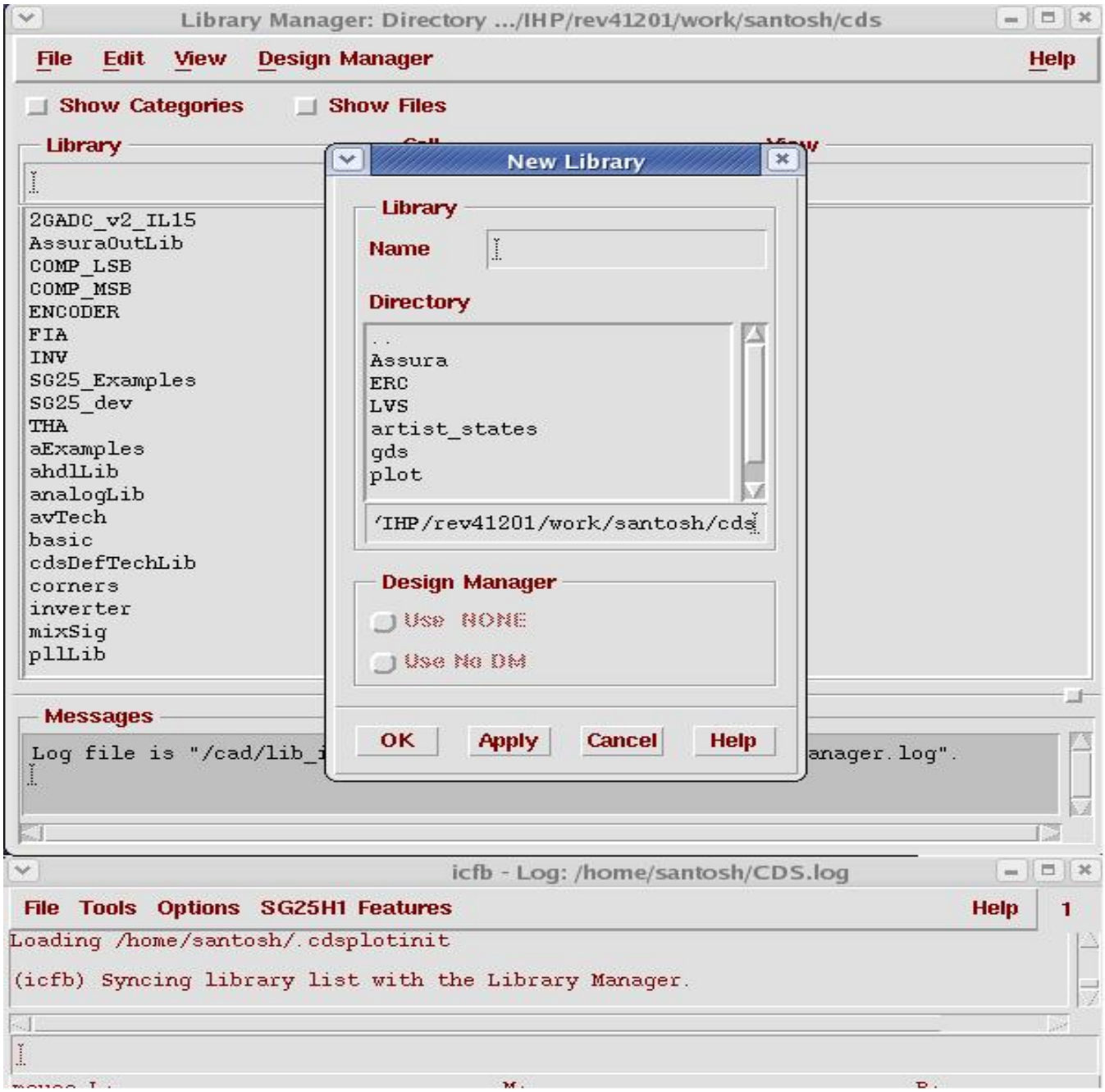

Fig 2

Give the name as INV_S and press ok. Once you will press ok, you will find a window as shown in Fig 3:

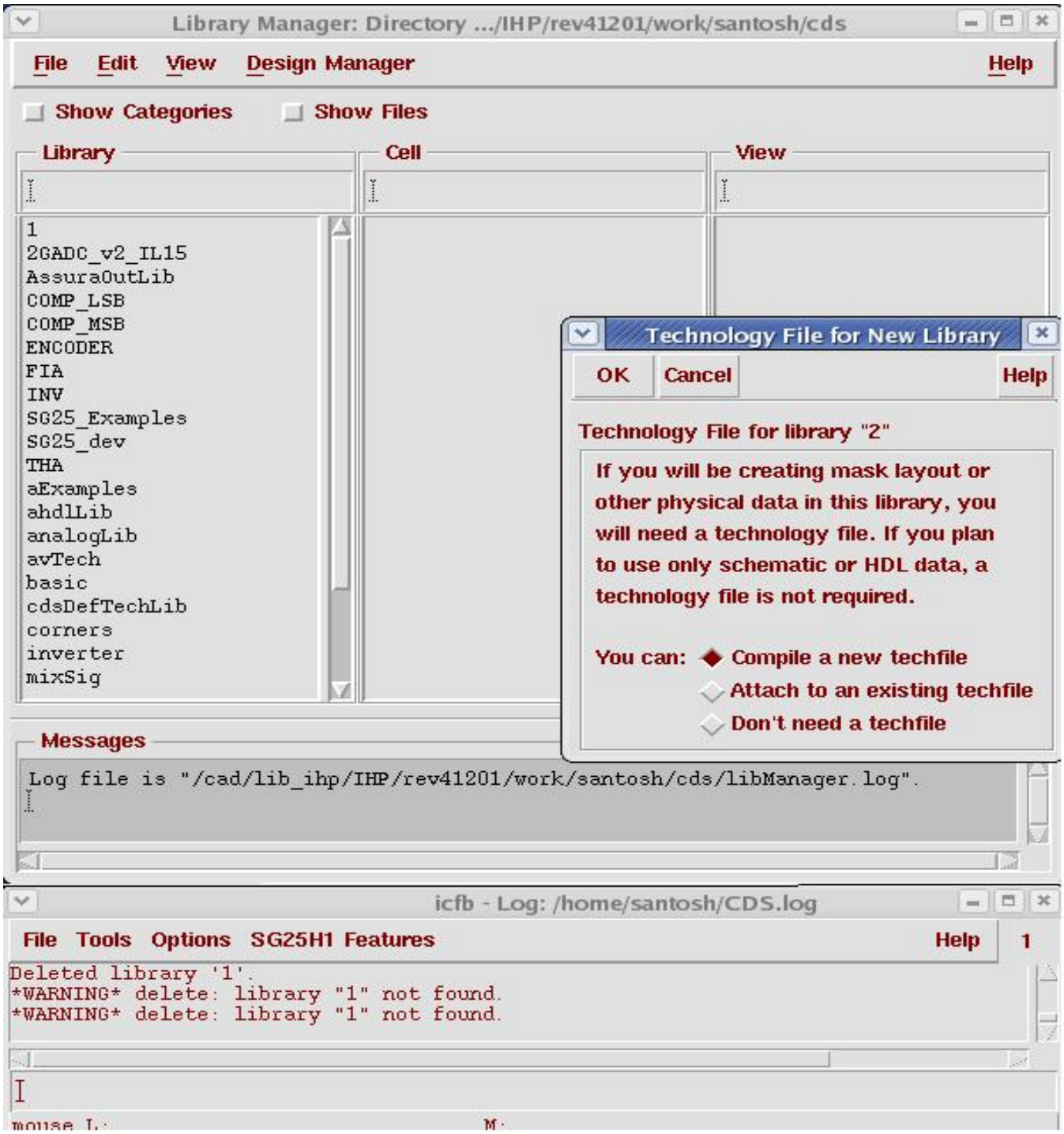

Fig 3

Select the option: “Attaché to the existing tech file”, then press ok. Now you will see a window as shown in Fig 4:

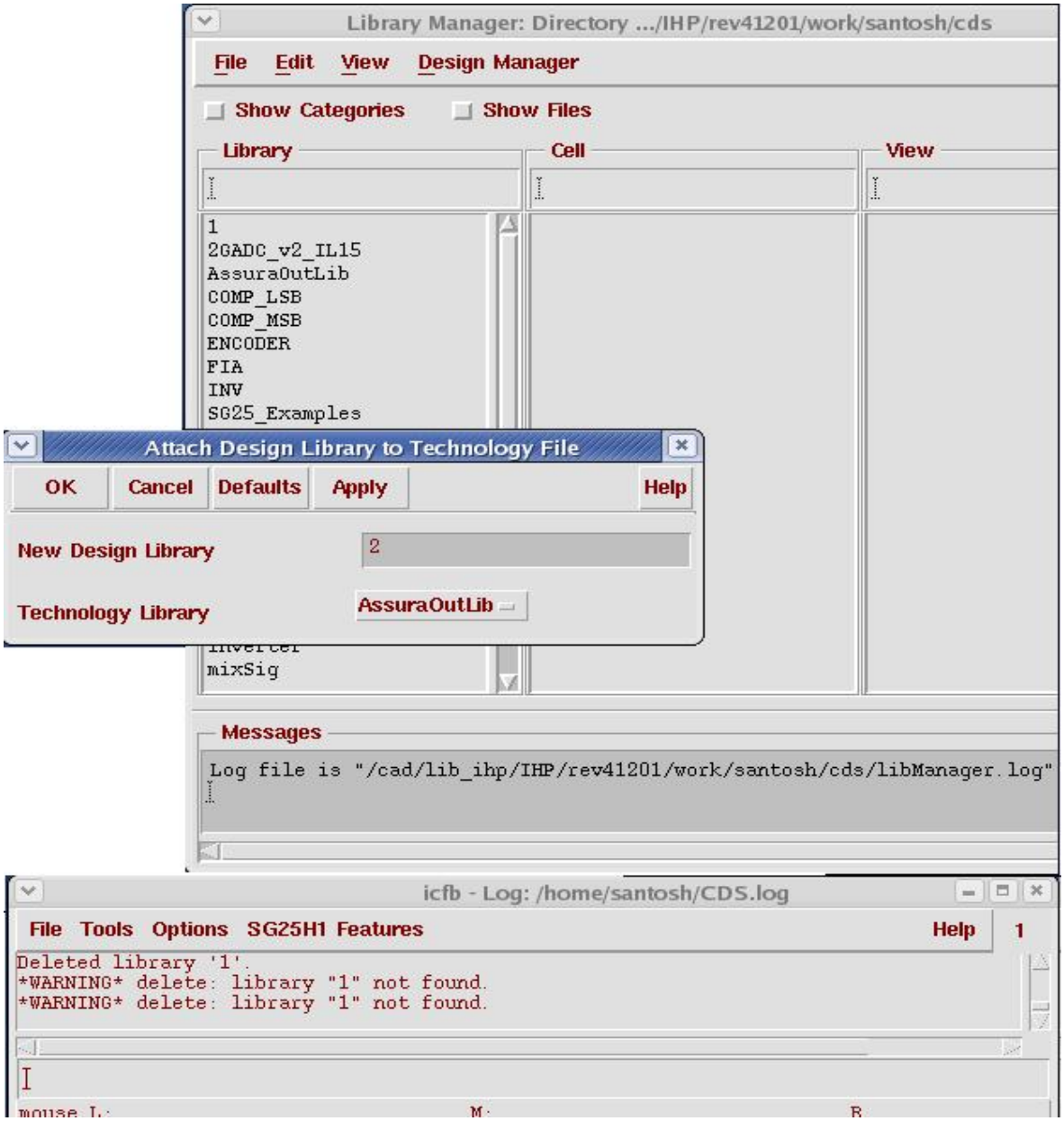

Fig 4

Change the Technology Library to SG25_dev as shown in Fig 5:

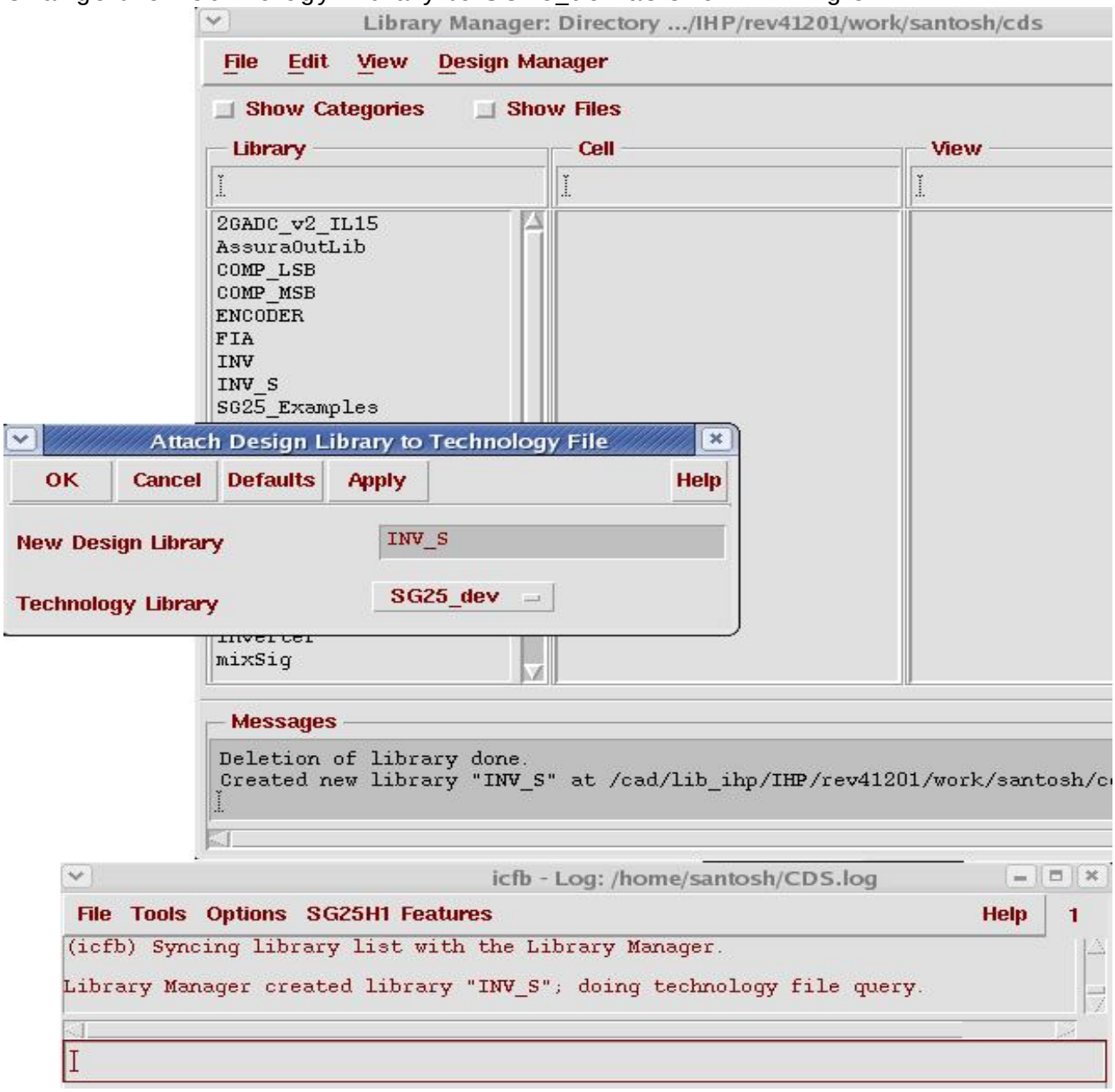

Fig 5.

Then press ok.

This will create a library INV_S as shown in Fig 6:

Fig 6.

Now, go to Library manager->file->New->cell view. One window will open as shown in Fig 7:

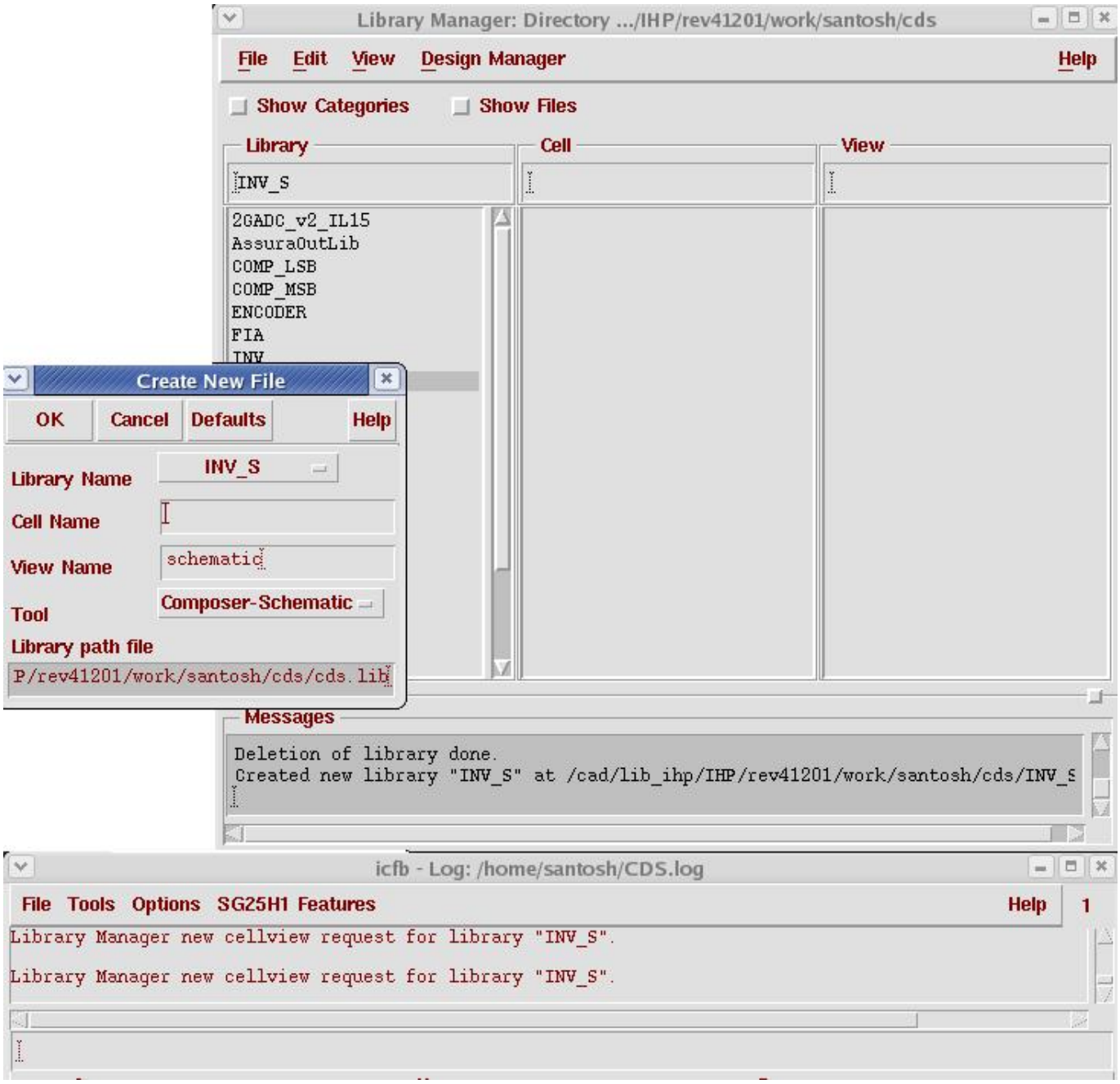

Fig 7

Give the cell name as “inv”. Set the Tool to "Composer-Schematic", then press ok. Now the Virtuoso schematic editor will open as shown in Fig 8:

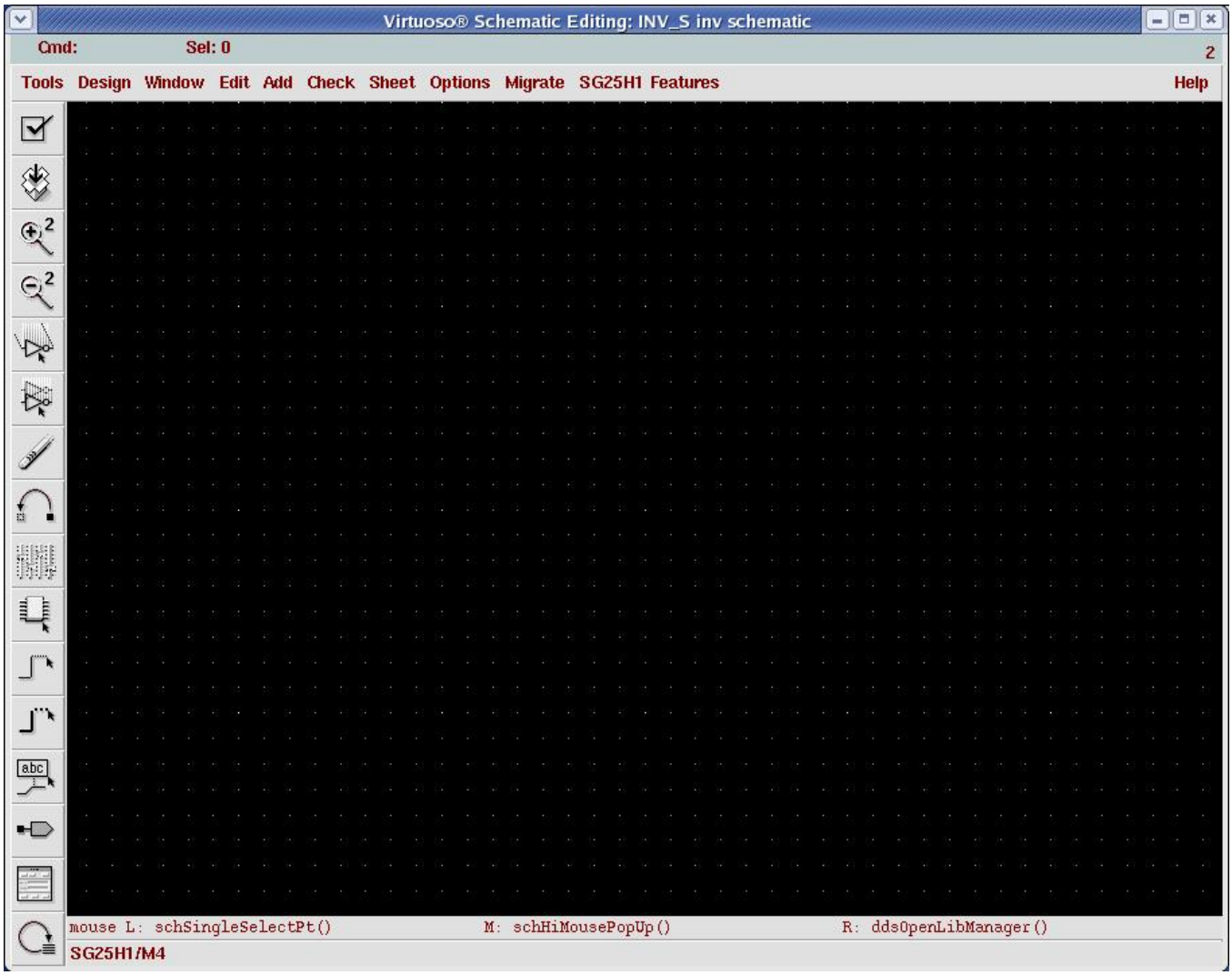

Fig 8

Now go to Add->instance. This will open a window as shown in Fig 9:

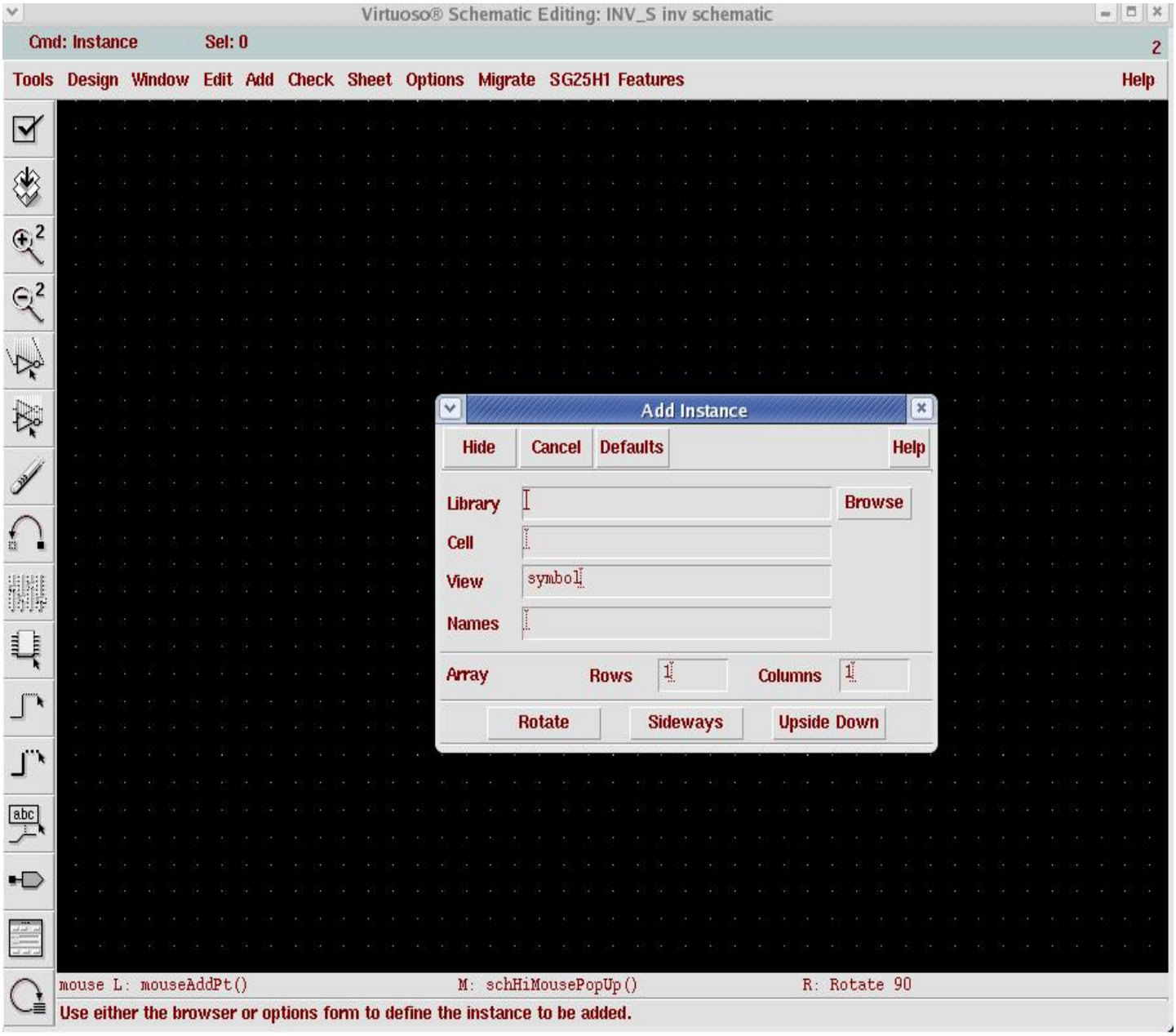

Fig 9

Now press the browse button, this will take you to Library browse window as shown in Fig 10:

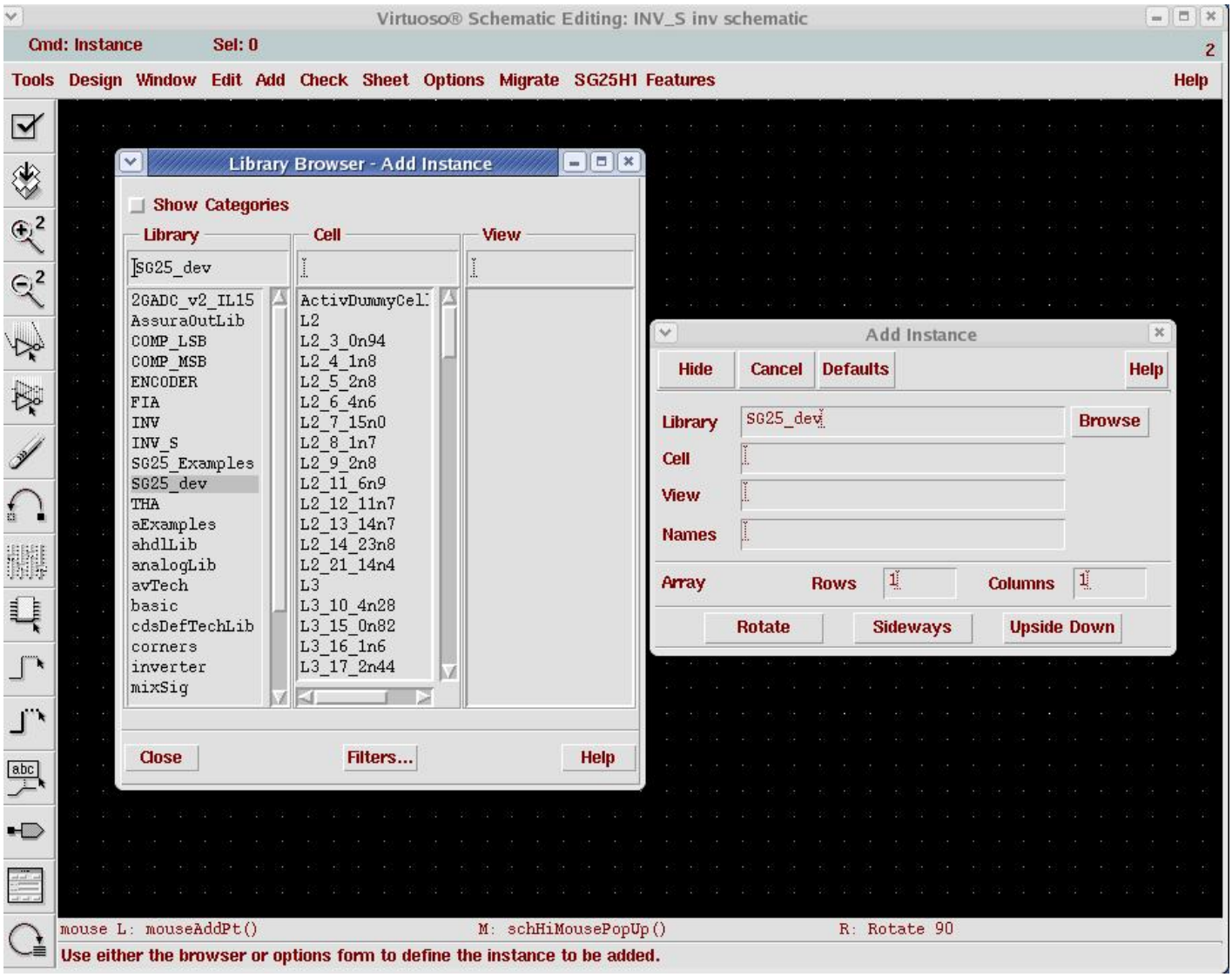

Fig 10

Select the SG25_dev library, the search for pmos as shown in Fig 11:

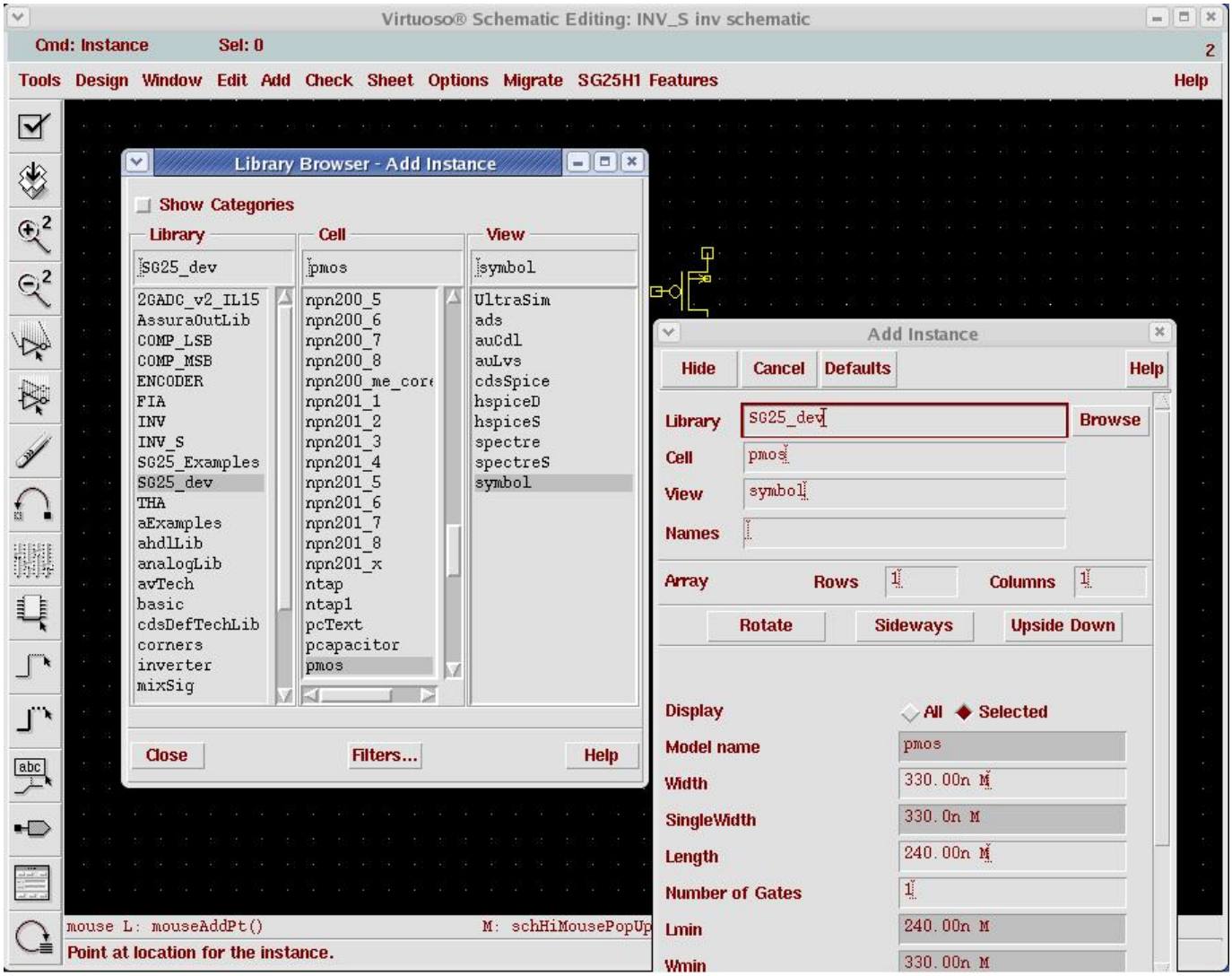

Fig 11

Now close the Library browser window, hide the Add instance window, and place the pmos on the schematic editor as shown in Fig 12:

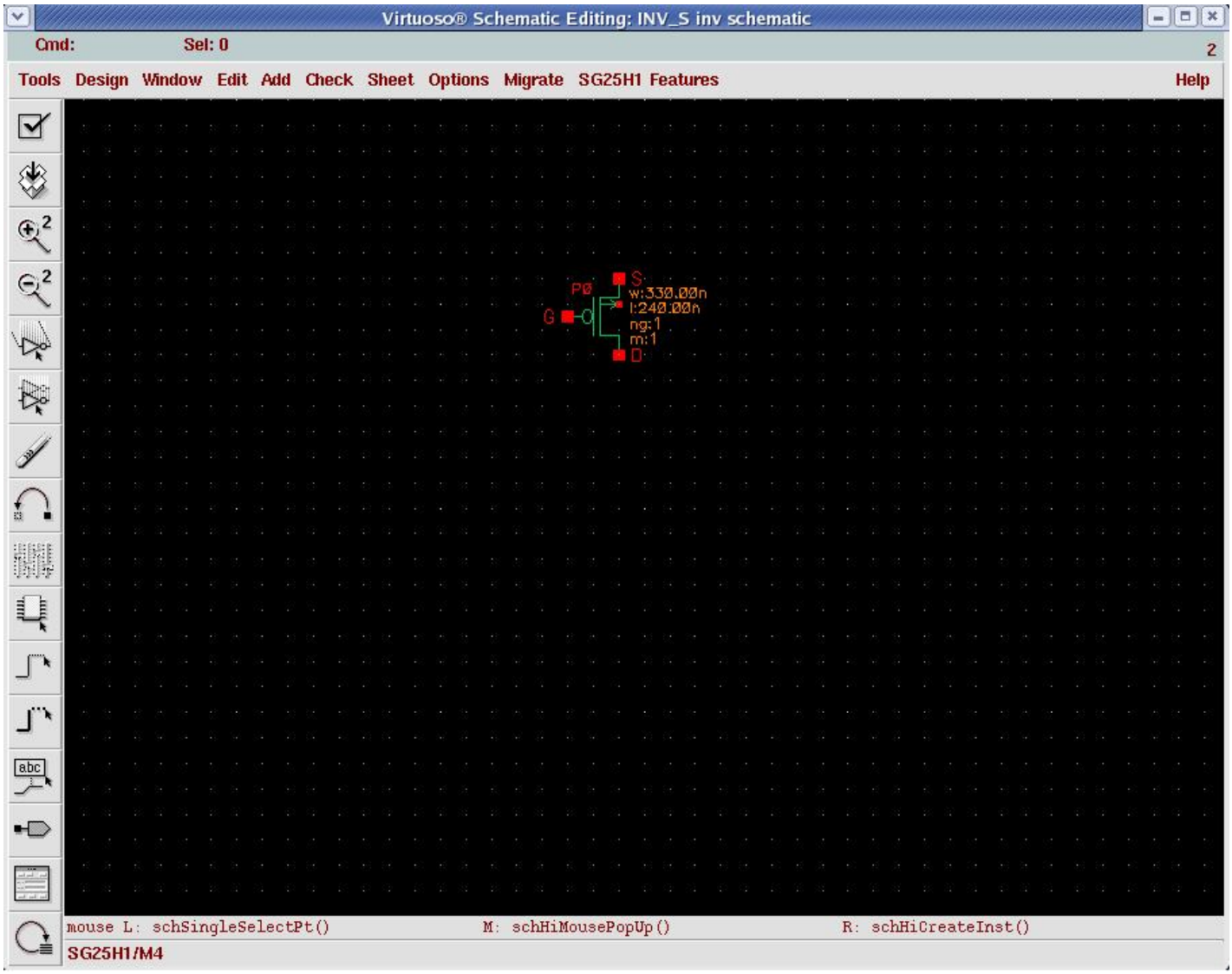

Fig 12

Then press “Esc” button.

The same way, you can go for nmos transistor. Now press “w” for wire and do the connection as shown in Fig 13:

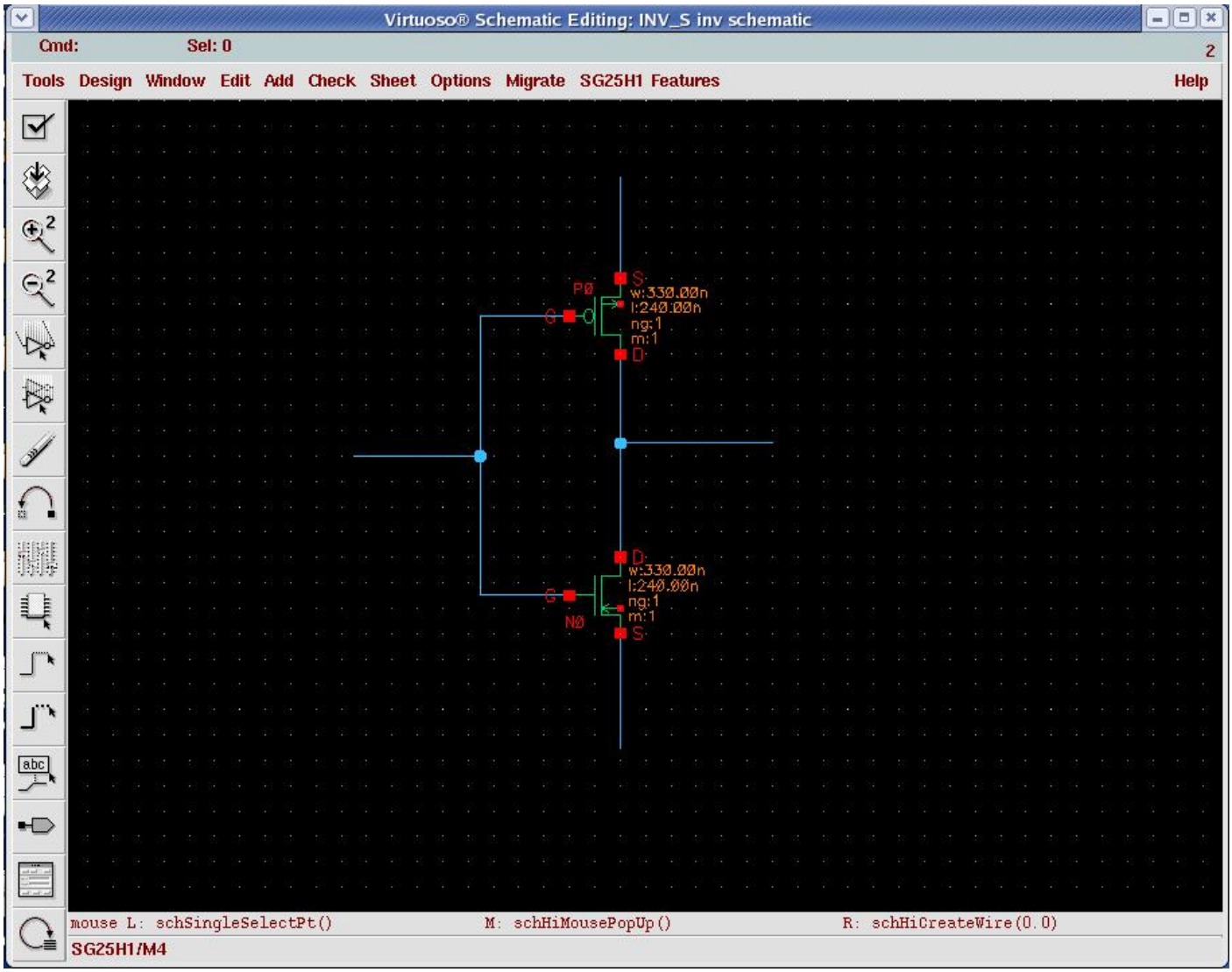

Fig 13

Now, you have to go for vdd, vdc, gnd, and vpulse. These things are available in analogLib. Then, place these components as shown Fig 14:

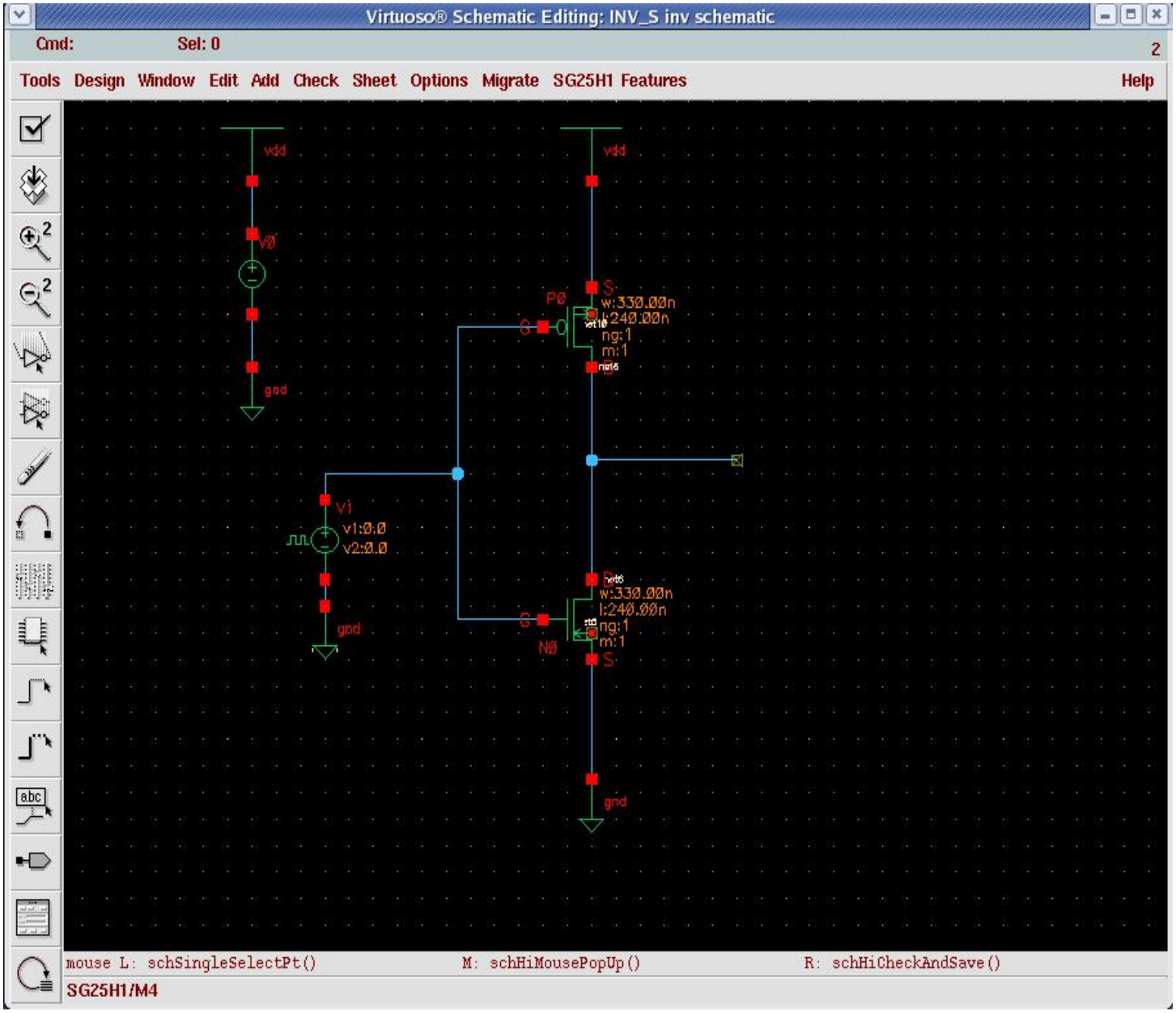

Fig 14

Connect the substrate and nwell to "sub", ptap1, ntap1 (SG25_dev). Also connect the output to a pin. This is as shown Fig 15:

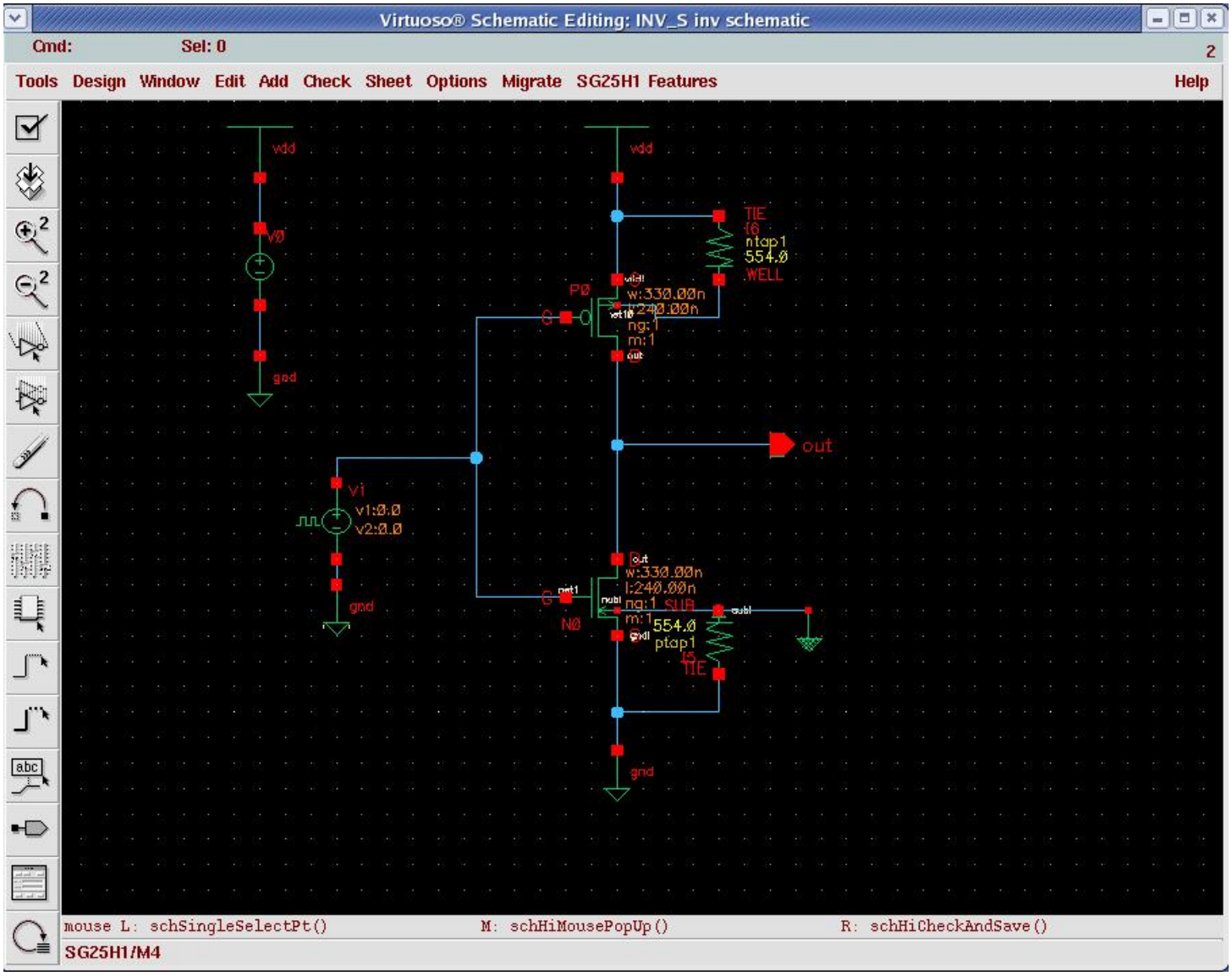

Fig 15

Now to set the pulse value, select the instances, then go to edit->property->object. This will open the following window:
Set the values as shown in Fig 16.

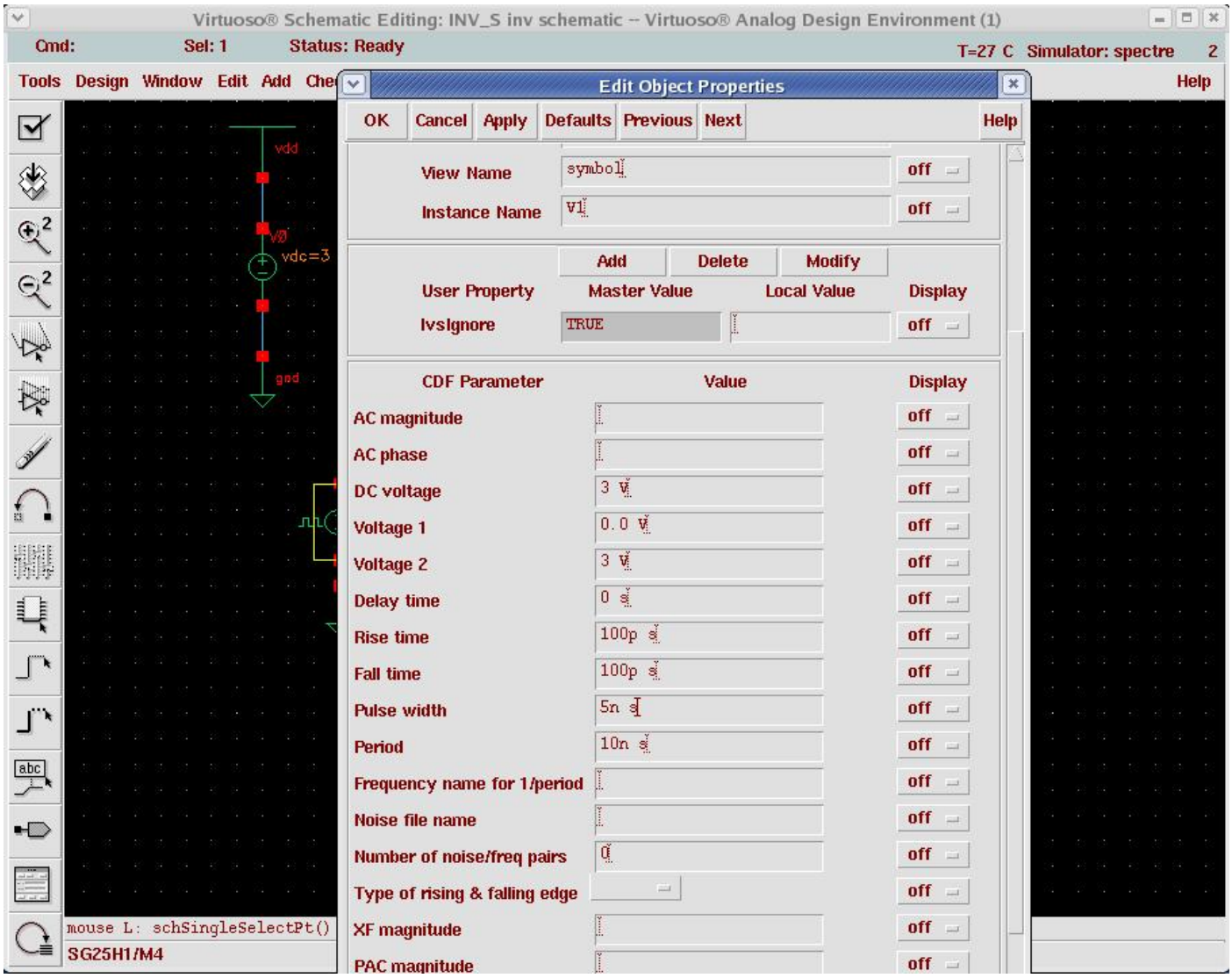

Fig 16

Same way you can set the dc value and width of pmos and nmos as shown in Fig 17, Fig 18, and Fig 19:

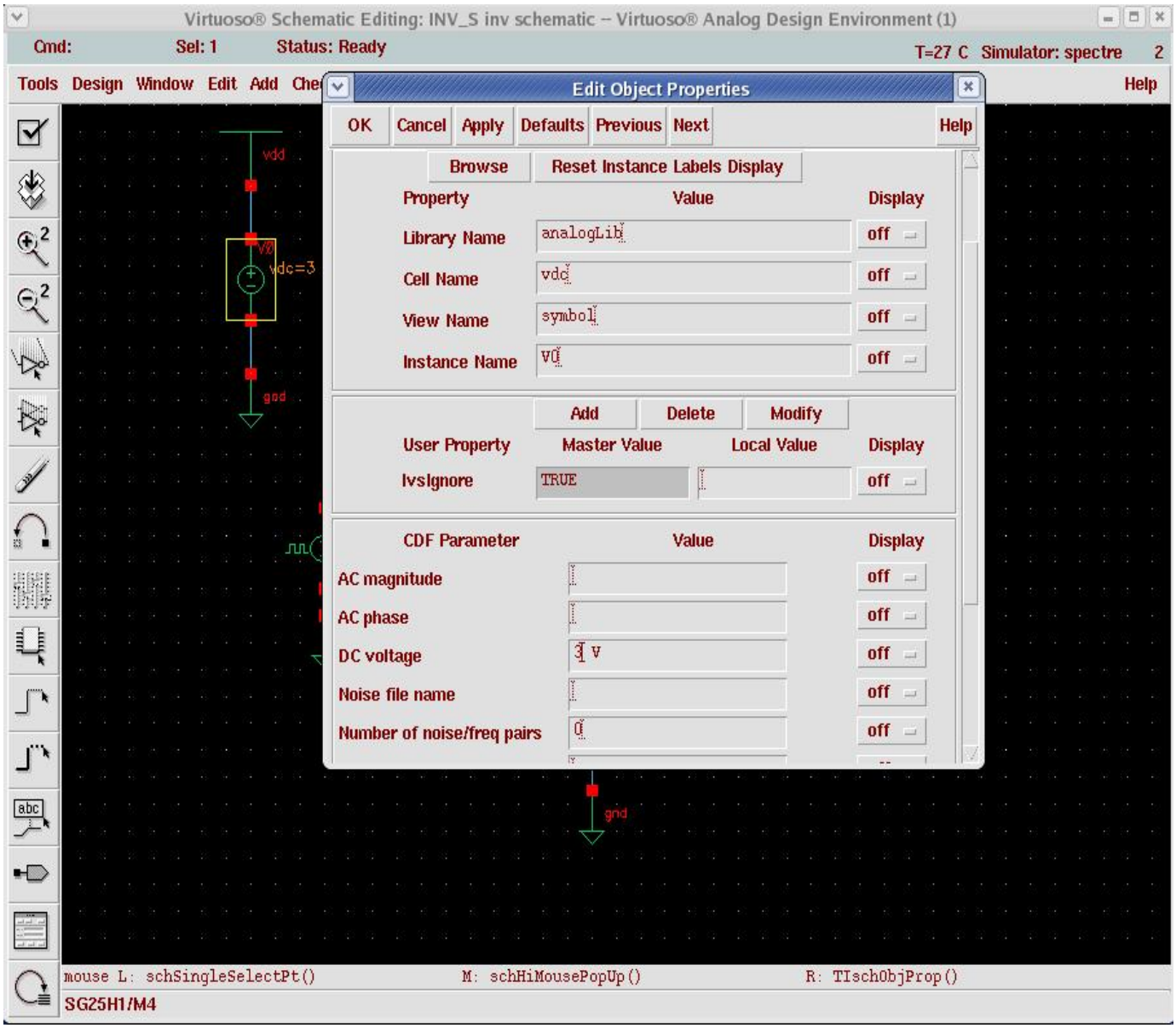

Fig 17

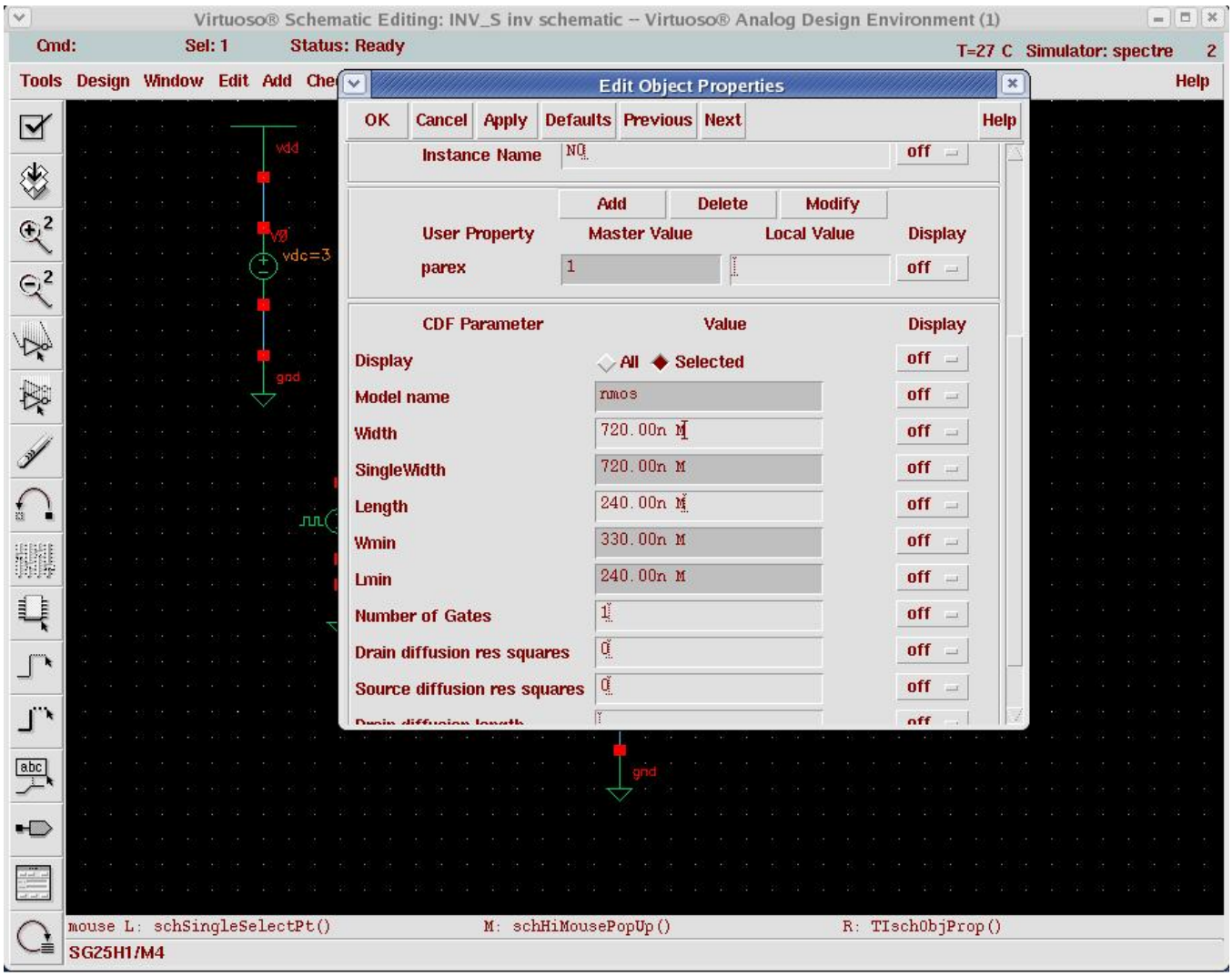
Virtuoso® Schematic Editing: INV_S inv schematic -- Virtuoso® Analog Design Environment (1)
Cmd:
Sel: 1
Status: Ready
T=27 C
Simulator: spectre
Tools
Design
Window
Edit
Add
Help
Edit Object Properties
OK
Cancel
Apply
Defaults
Previous
Next
Help
Instance Name
M0
off
Add
Delete
Modify
User Property
Master Value
Local Value
Display
parex
1
off
CDF Parameter
Value
Display
Display
All
Selected
Model name
nmos
Width
720.00n M
SingleWidth
720.00n M
Length
240.00n M
Wmin
330.00n M
Lmin
240.00n M
Number of Gates
1
Drain diffusion res squares
0
Source diffusion res squares
0
vdd
vdc=3
gnd
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: TIschObjProp()
SG25H1/M4

Fig 18

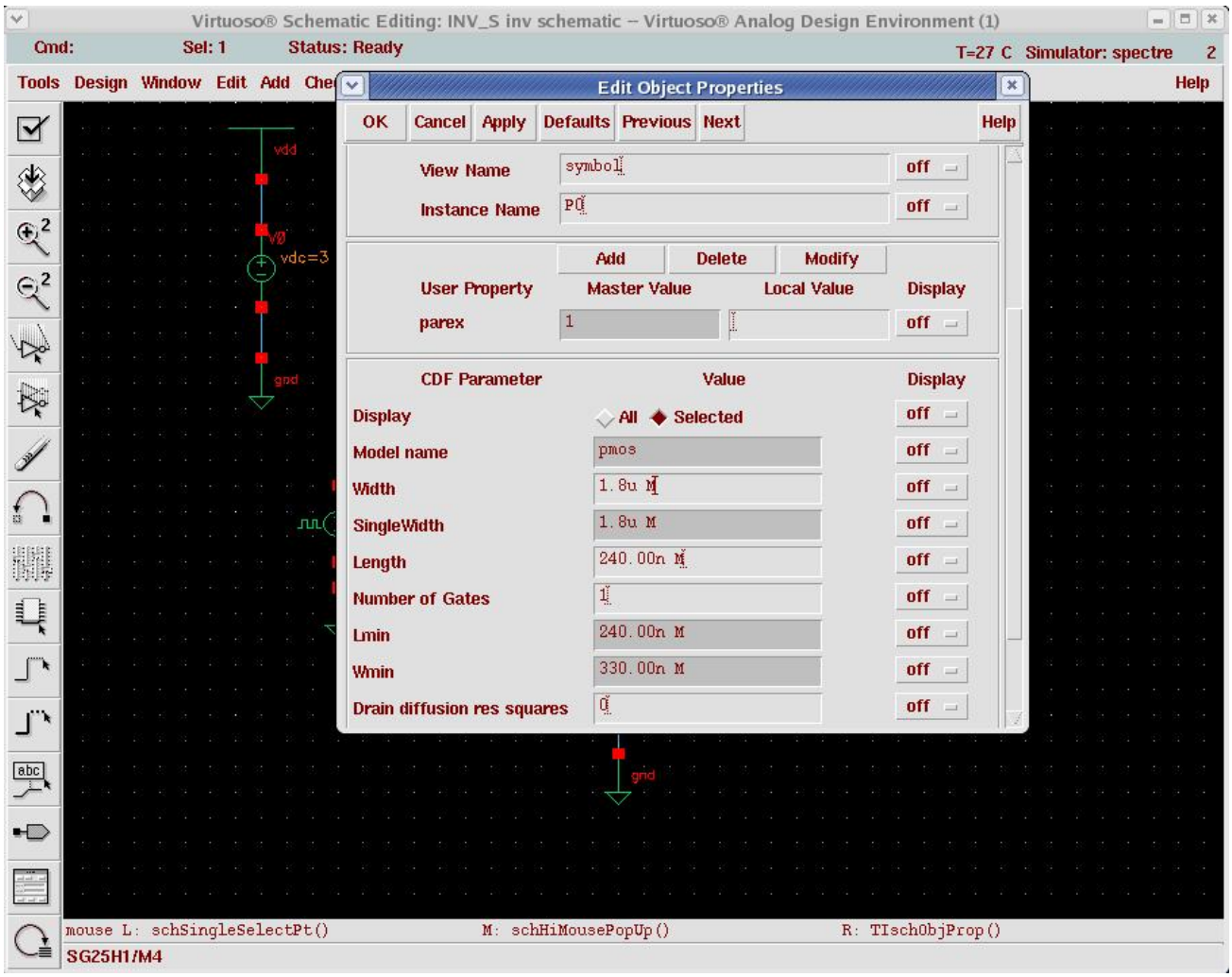

Fig 19

Then go to Design->Check and Save.

This completes your schematic.

Simulation:

Once your schematic is checked and saved without any warning and error, you can go for simulation.
For simulation, go to Tools->Analog Environment. This will open a window as shown in Fig 20:

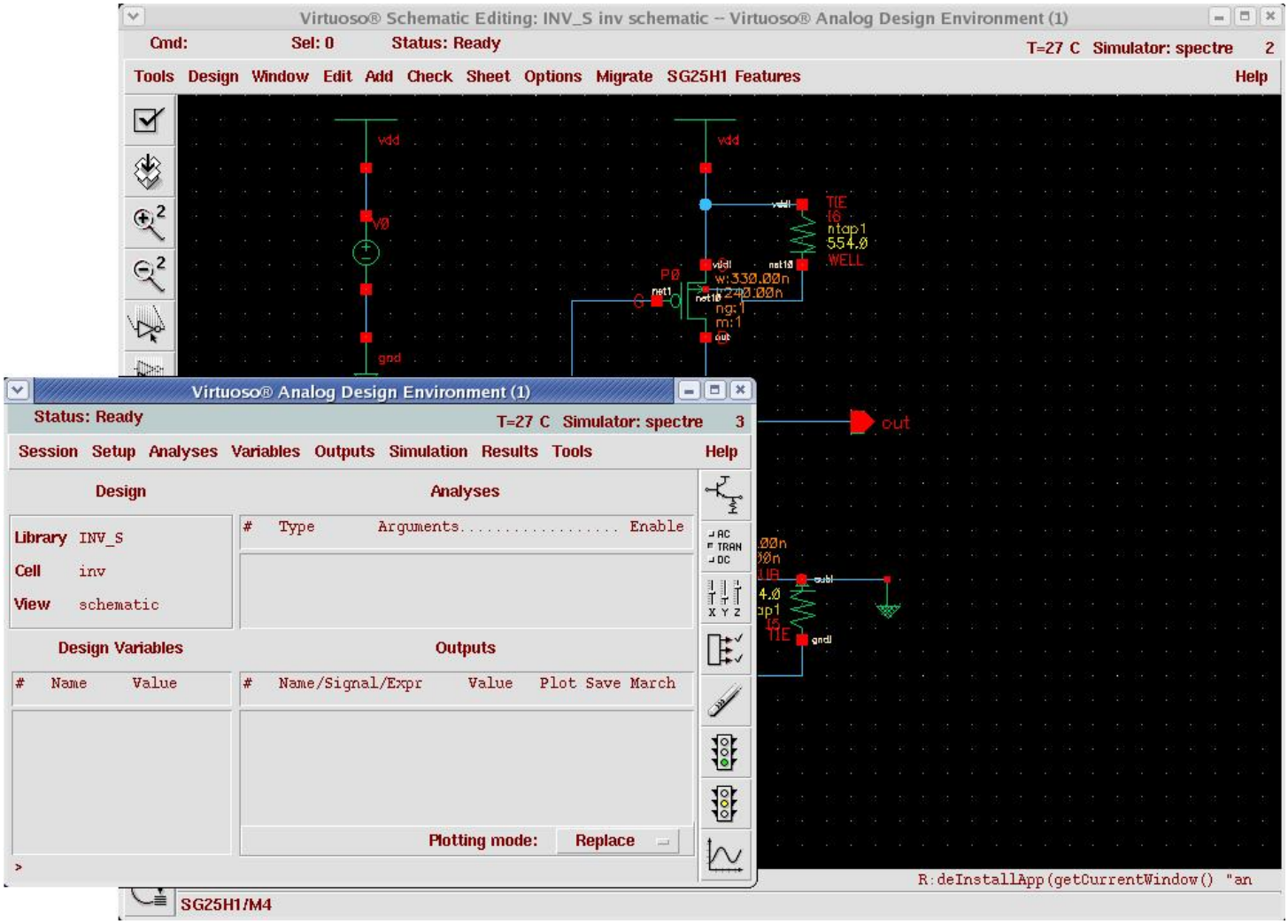

Fig 20

Now go to Analysis->Choose. You will see a window as shown in Fig 21:

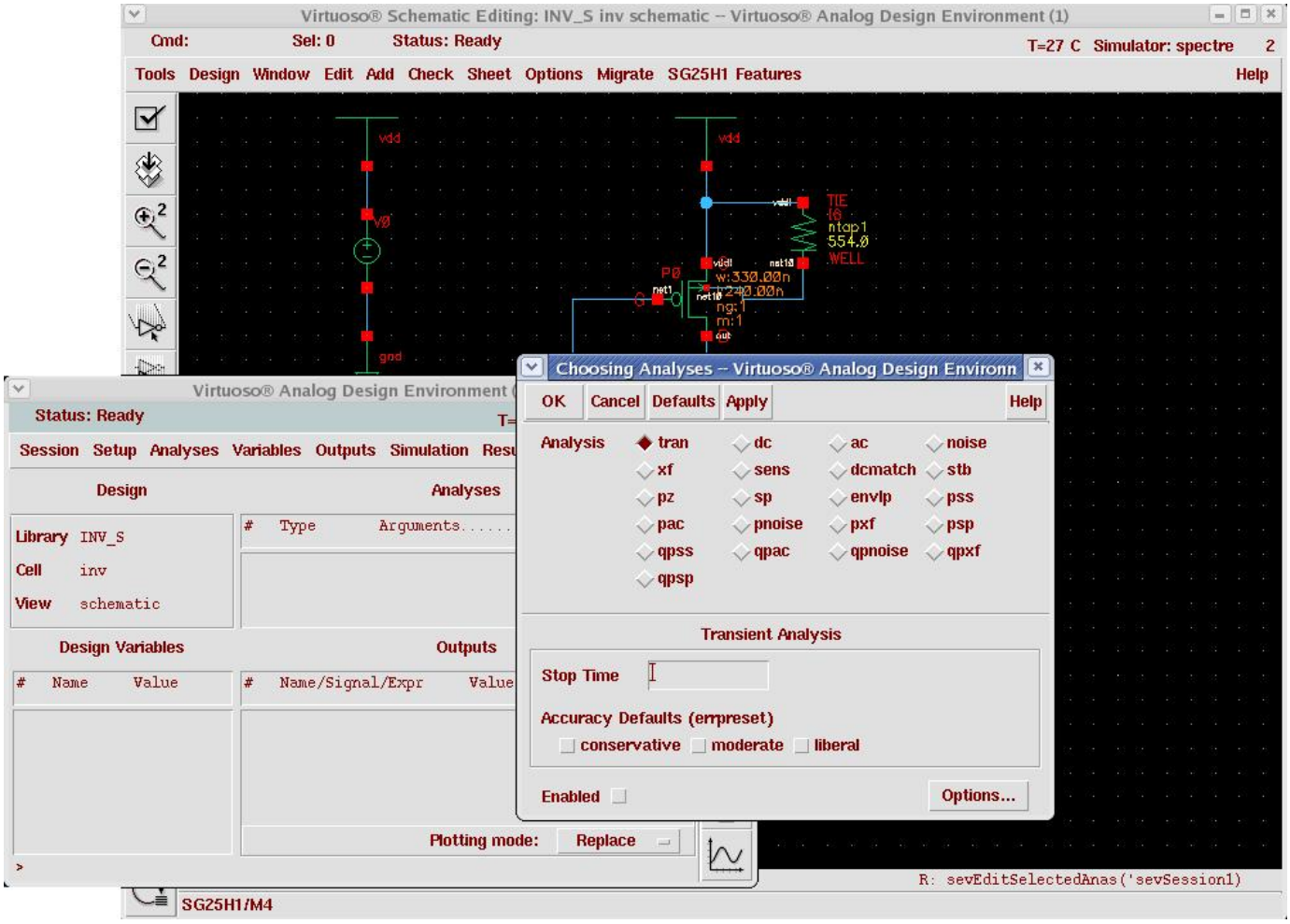

Fig 21

Select the “tran” option and set the stop time as 100n (n-nano second). Then press ok.
Now go to Outputs->To be plotted, select the nets on the schematic where you want to see the signal.

The final setup for simulation will look as shown in Fig 22:

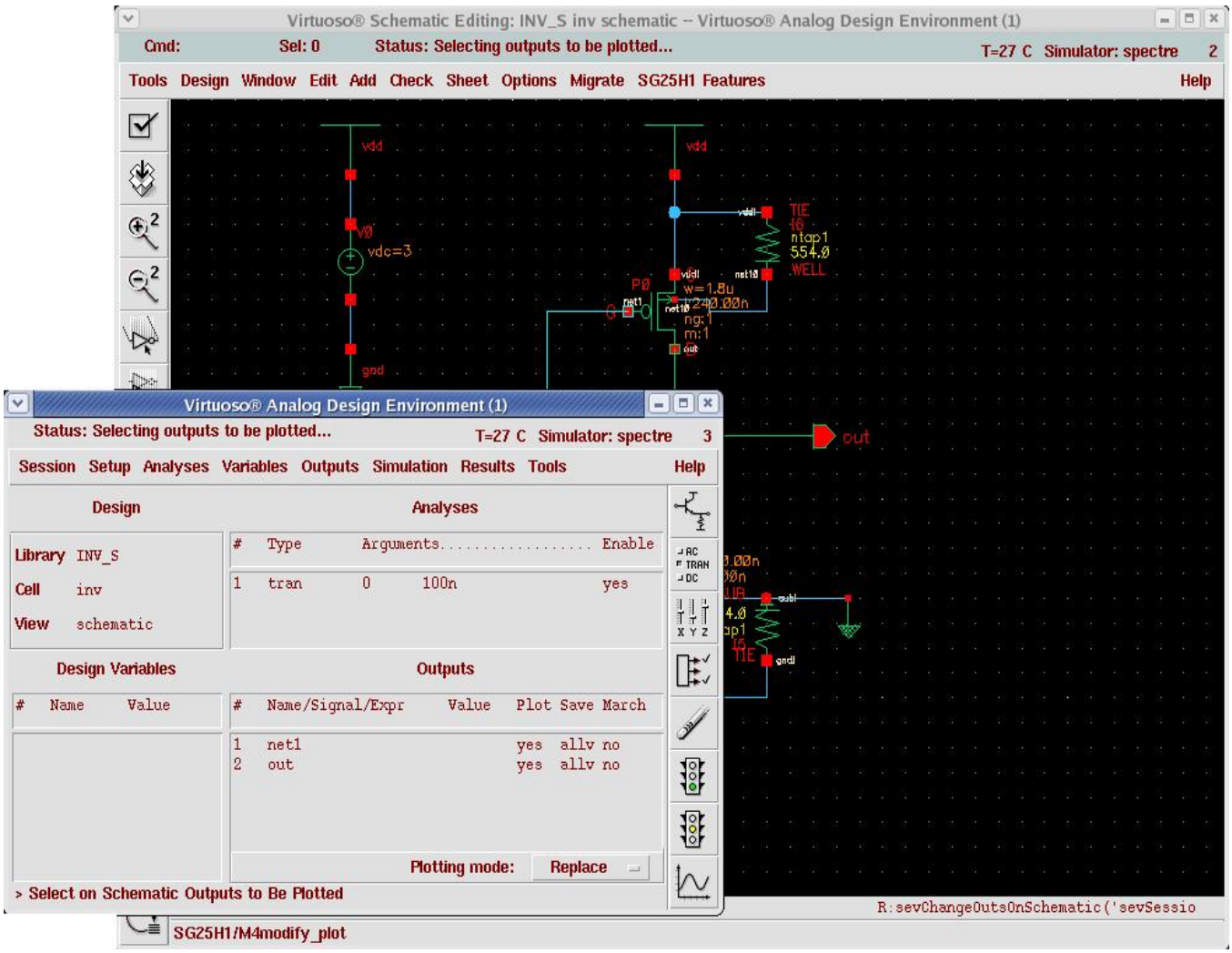

Fig 22

Now press the “Green signal button” for running the simulation.

This will open a window, which will show you the run details. This is as shown in Fig 23:

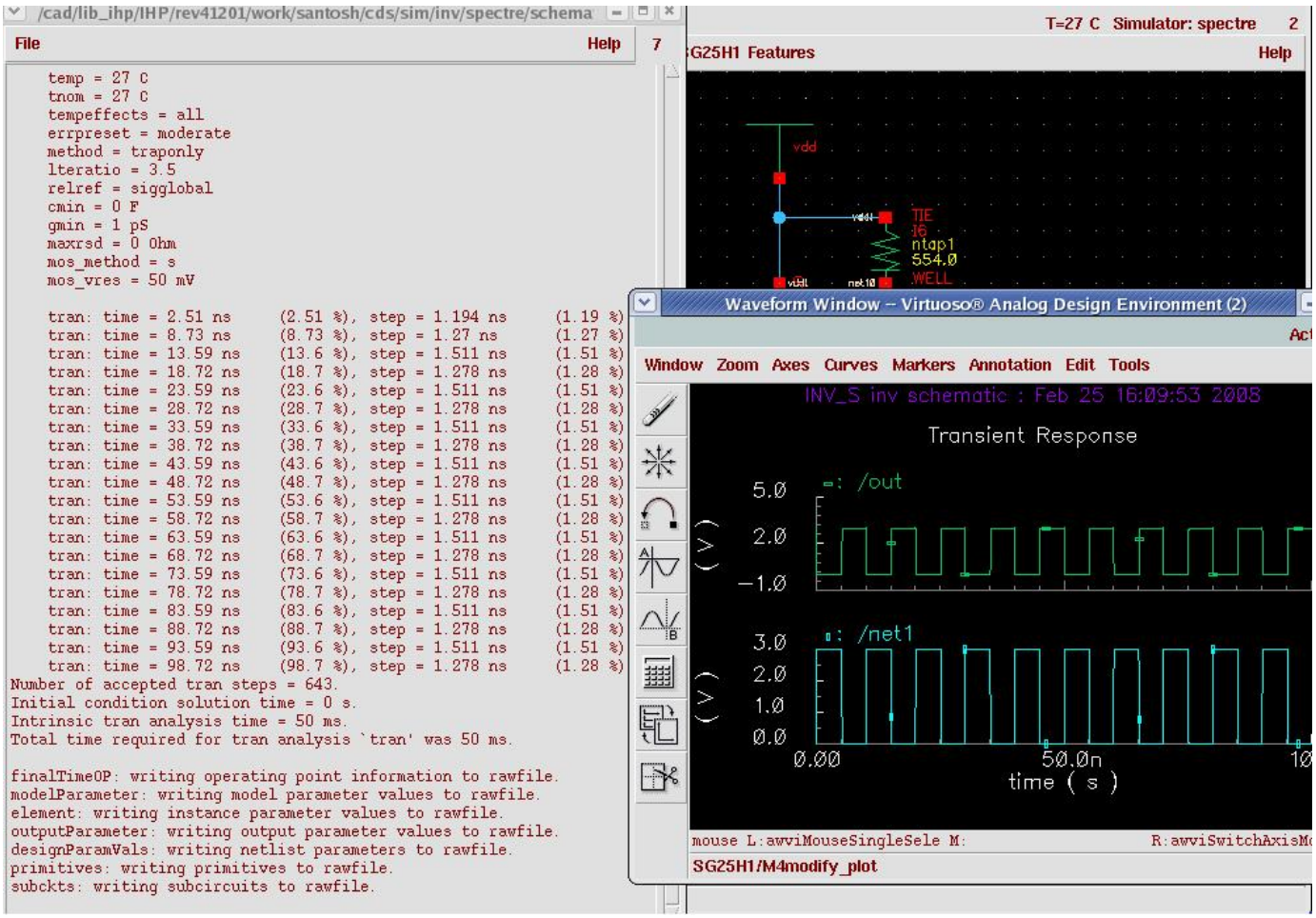

Fig 23

Once your simulation will over, you can see the waveform as shown above.
