Figure 1 limiting-receiver top-level schematics.
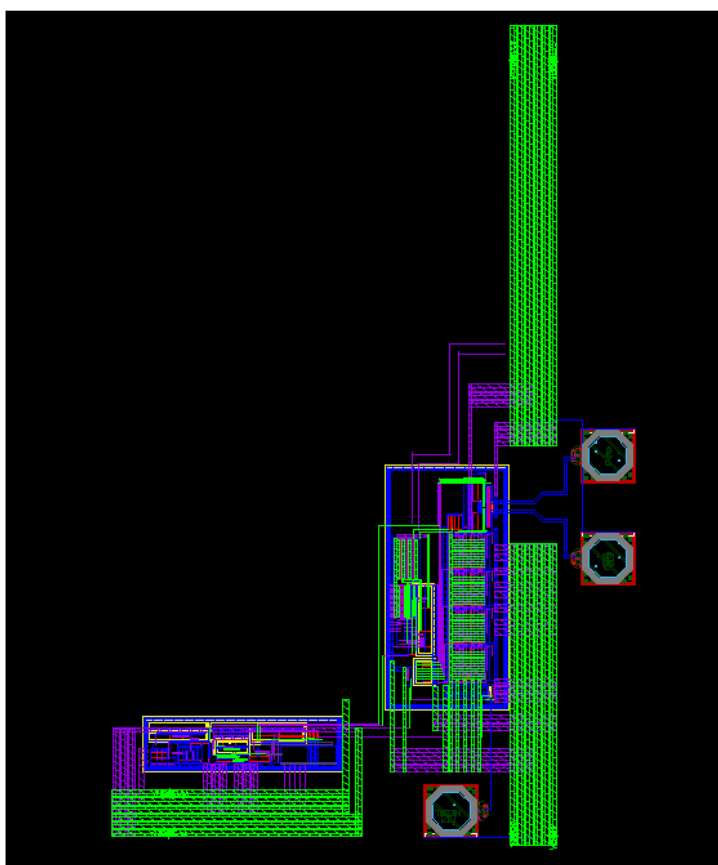

Figure 2 layout of limiting receiver (Figure 1) and bandgap references.
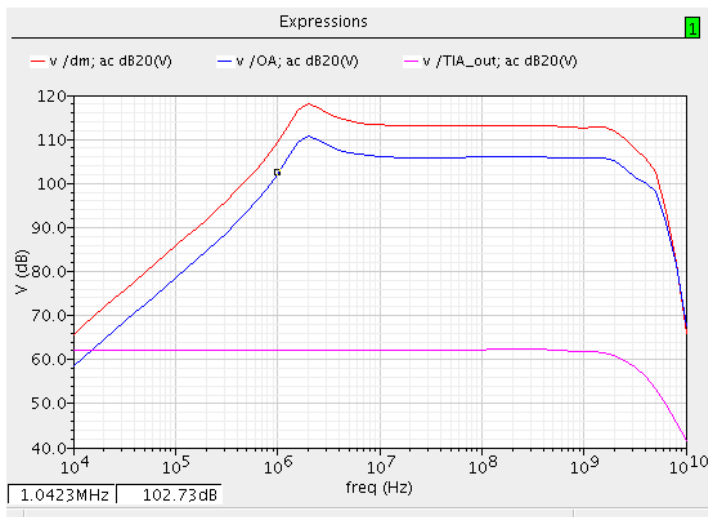
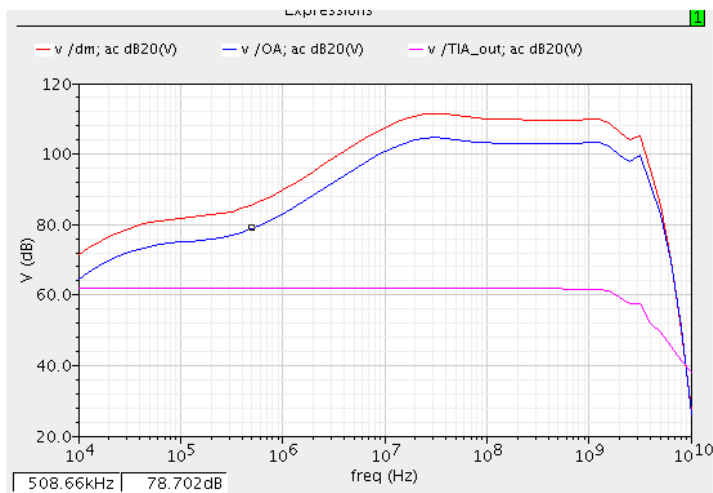**Figure 3 individually extracted sub-blocks simulation results.**

Figure 4 Overall extracted simulation.

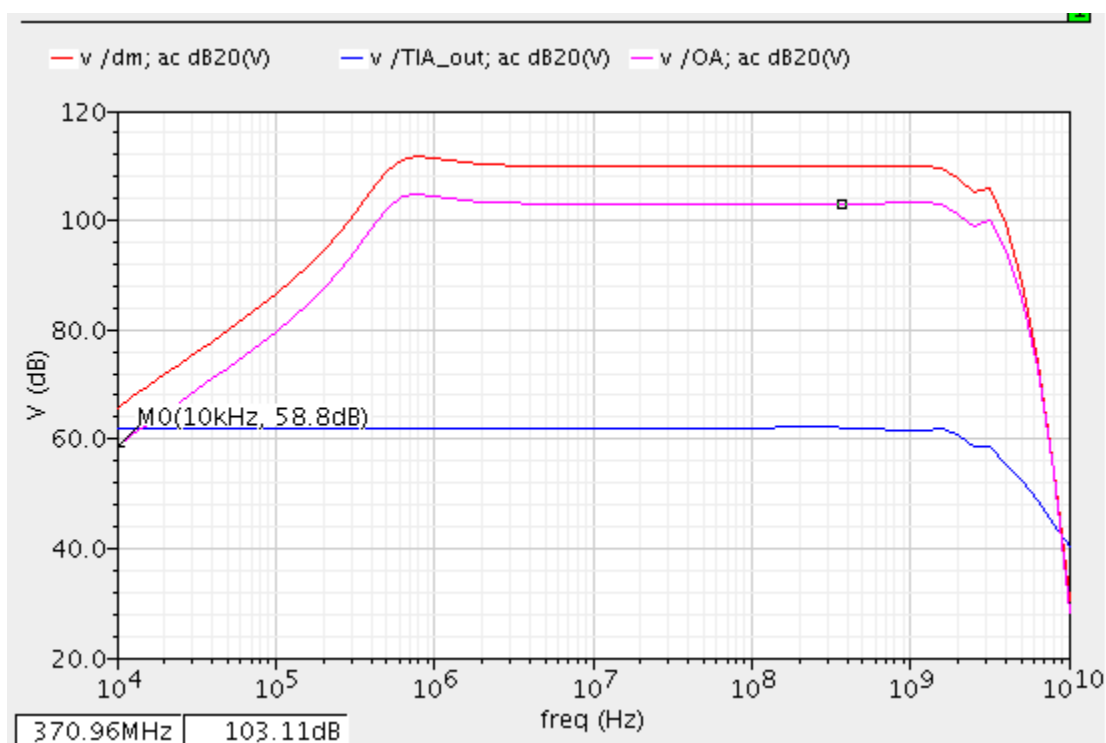**Figure 5 Layout of Figure 1, without bandgap**

Figure 6 simulation of extracted of Figure 5, with extracted bandgap but connect in schematic at the top-level
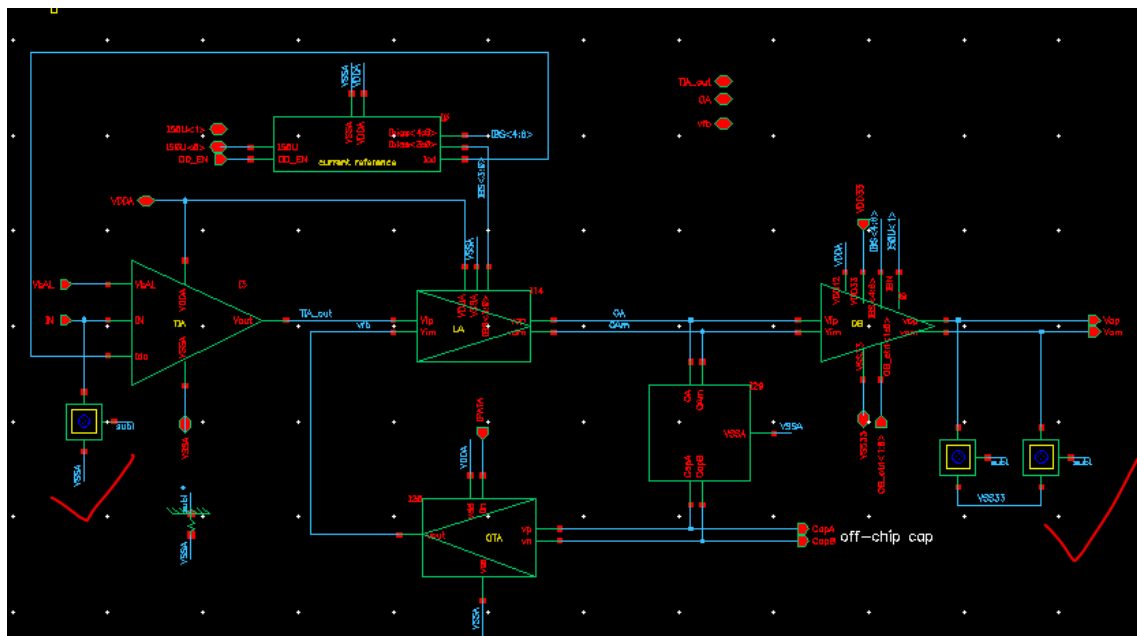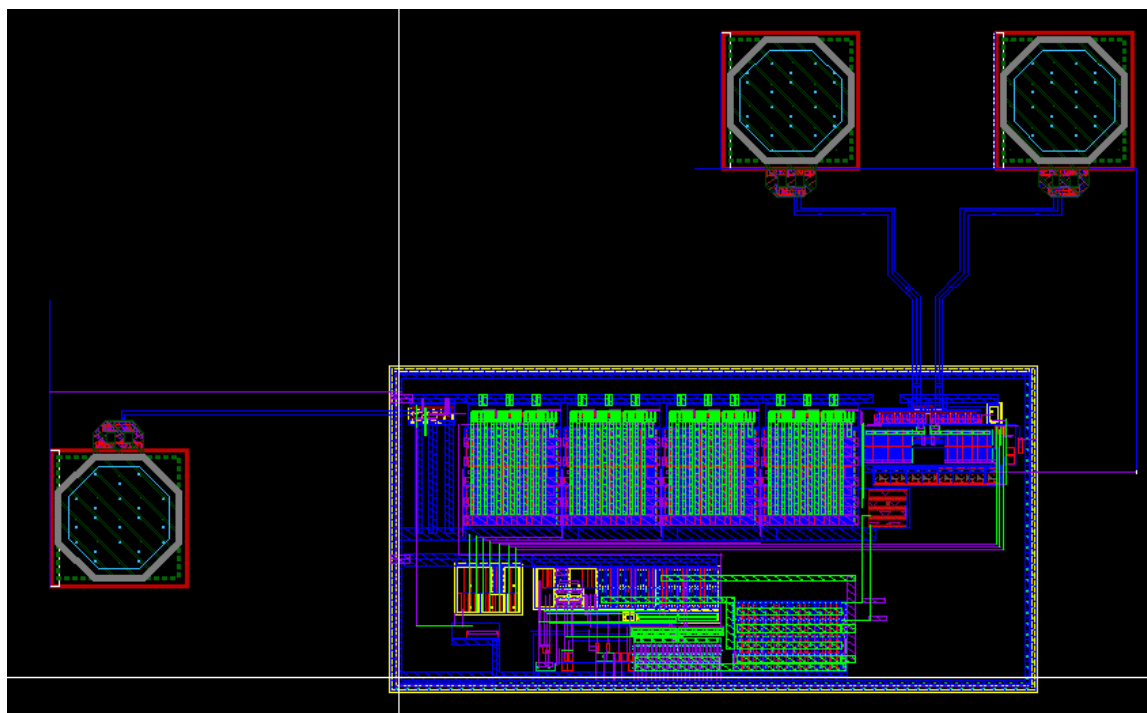
Figure 7 Adding pad for extraction
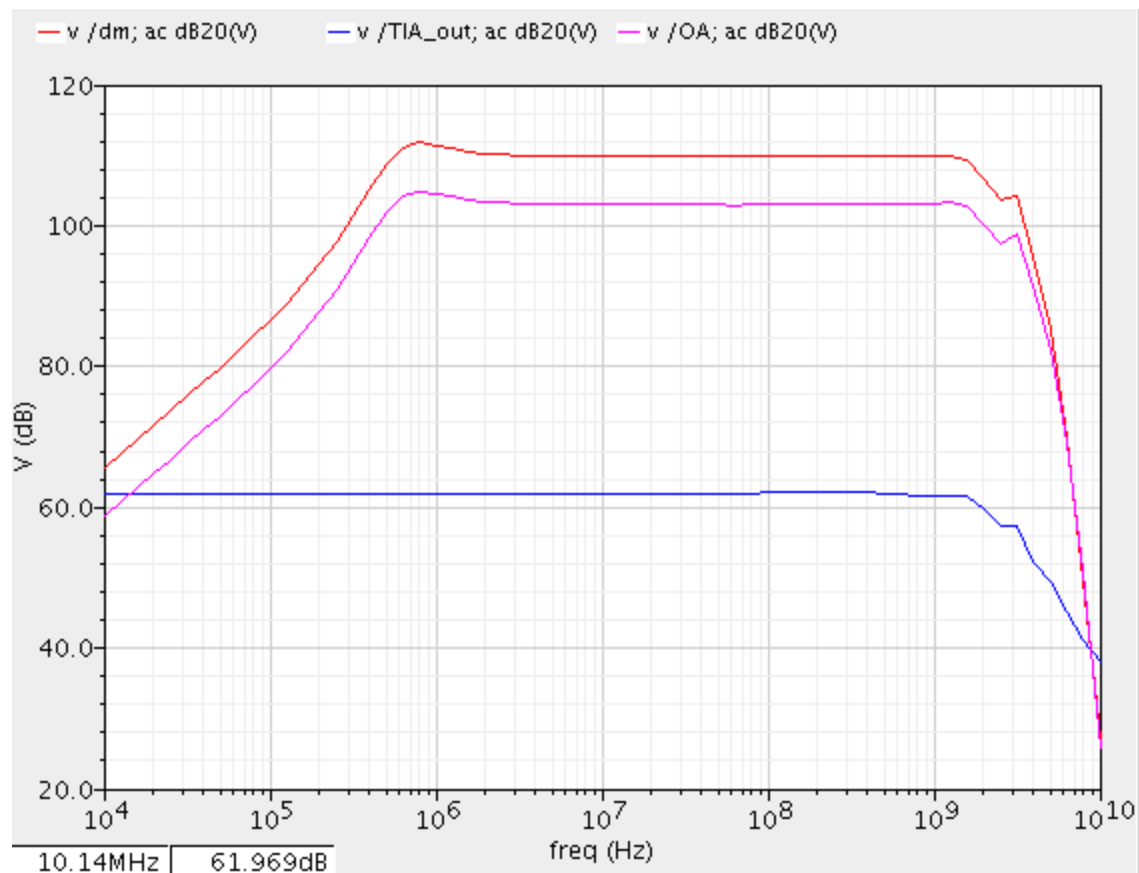

Figure 8 Layout of Figure 7

v /dm; ac dB20(V)   v /TIA_out; ac dB20(V)   v /OA; ac dB20(V)

10.14MHz   61.969dB

Figure 9 simulation of Figure 8, pad added, but not significant changes of the magnitude response.

v /dm; ac dB20(V)   v /TIA_out; ac dB20(V)   v /OA; ac dB20(V)
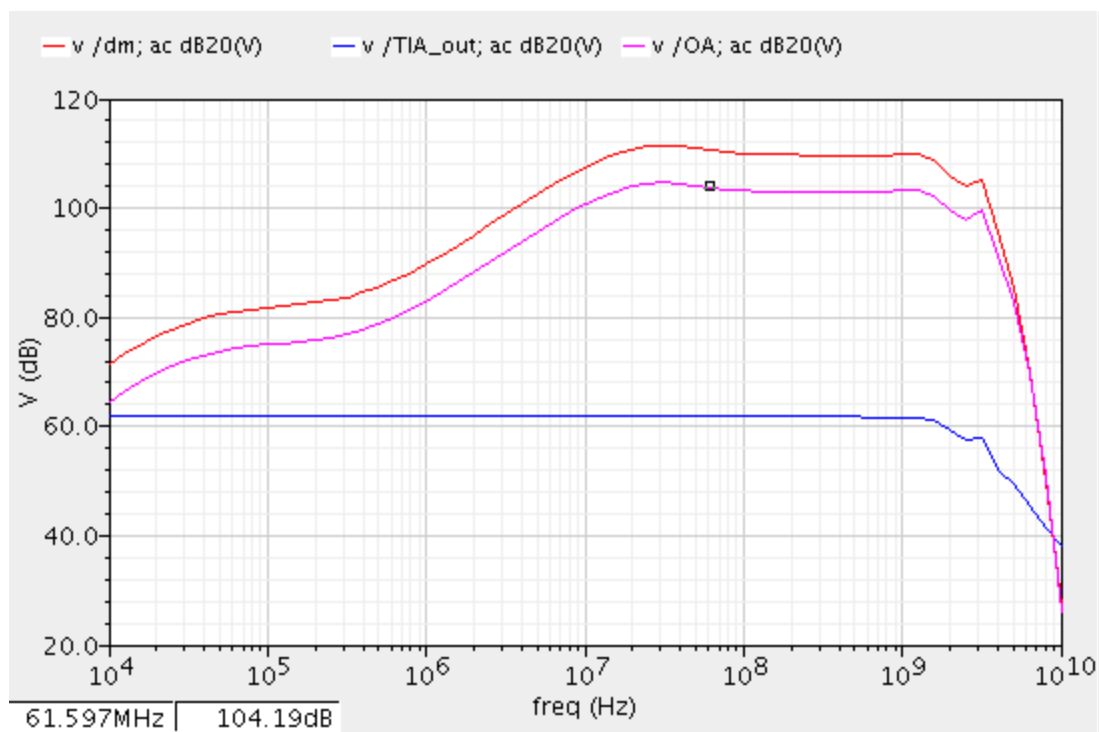
61.597MHz   104.19dB

Figure 10 Same problem exist even changing metal layer for the bias and PTAT current.
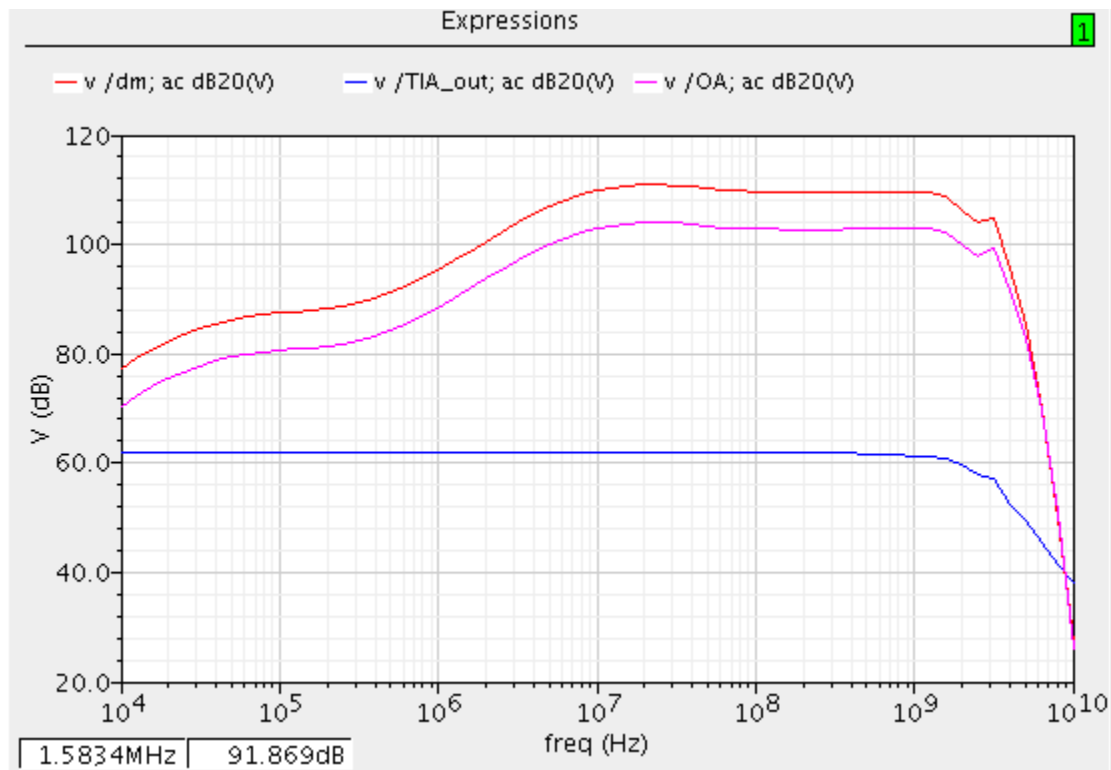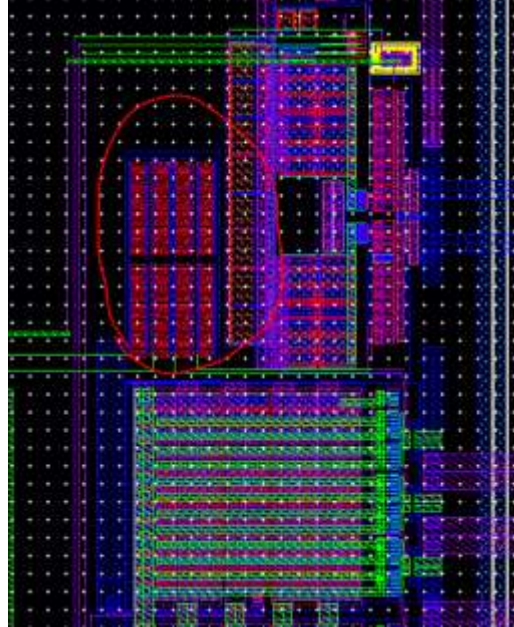

Figure 11 Feedback resistances doubled, just a little effect, still not good.