

Switching Regulator Series

PCB Layout Techniques of Buck Converter

No.12027EBY05

PCB layout design for switching power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. Major problems that arise from inappropriate layout may cause increase in noise superposed by output and switching signal, the deterioration of regulator, and also lack of stability. Adopting an appropriate layout will suppress these problems to occur.

Current Path

Figure 1-a to 1-c shows current path in a buck converter circuit. In Figure 1-a, the red line illustrates the main current flow in the converter when switching element Q1 is ON. CBYPASS is a decoupling capacitor for high frequency and CIN is the capacitor with large capacitance. The instance when the switching element Q1 is turned ON, most of the steep part of current waveform is supplied by CBYPASS and then from CIN.

In Figure 1-b, the red line illustrates the condition of current flow when the switching element Q1 is OFF. Free-wheel diode D1 turns ON and energy stored in inductor L gets released to output side. For Buck converter topology, since inductor is inserted at output in series the output capacitor current is smooth.

Refer Figure 1-c, the red line shows the difference between Figure 1-a and 1-b. Current in this red line changes violently each time the switching element Q1 changes from OFF to ON, and vice versa. These sharp changes induce several harmonics in the waveform. This difference in system needs to be paid maximum attention during PCB layout and an important caution point.

PCB Layout Procedure

General points of PCB layout procedure are as follows.

1. Place input capacitor and free-wheel diode on the same PCB surface layer as the IC terminal and as close as possible to IC.
2. Include thermal via if necessary to improve heat dissipation.
3. Place inductor close to IC, no need to be as close as input capacitor. This is to minimize radiation noise from the switching node and do not expand copper area more than needed.
4. Place output capacitor close to inductor.
5. Keep wiring of return path away from noise causing areas, such as inductor and diode.

Placing of input Capacitor and Free-wheel Diode

First of all, start placing the most important parts, such as the input capacitor and free-wheel diode. A Single ceramic capacitor may serve as both CIN and CBYPASS for smaller capacitance value of input capacitor, in designs with small current power supply ($I_O \leq 1A$). This is because the frequency characteristics get better, as ceramic capacitor's capacitance value gets smaller. But ceramic capacitor has different frequency characteristics, so confirming it for actual parts being used is important.

As in Figure 2, when a large capacitance value capacitor is used for CIN, generally it has bad frequency characteristics. Therefore place a decoupling capacitor CBYPASS for high frequency with good frequency characteristics in parallel to CIN. For CBYPASS, use surface mount type laminated ceramic capacitor with value of 0.1 μ F to 0.47 μ F, X5R or X7R type.

Figure 3-a shows layout example for a suitable input capacitor. Place CBYPASS near IC terminal on the top layer. As in Figure 3-b, large capacitance capacitor CIN can be separated about 2cm from CBYPASS that supplies most of the pulse-current. When difficulty in space occupied, and if cannot place CIN on the same surface as IC, it can be placed at the bottom layer through via like in Figure 3-c. Risks regarding noise can be avoided with this, but there is a possibility of ripple-voltage to increase at high-current, influenced by via resistance.

Figure 3-d shows the layout of CBYPASS and CIN placed on the reverse side. In such case, voltage noise is created by inductance of the via, and the bypass capacitor operates as a reverse effect. Do not carry out this kind of layout design.

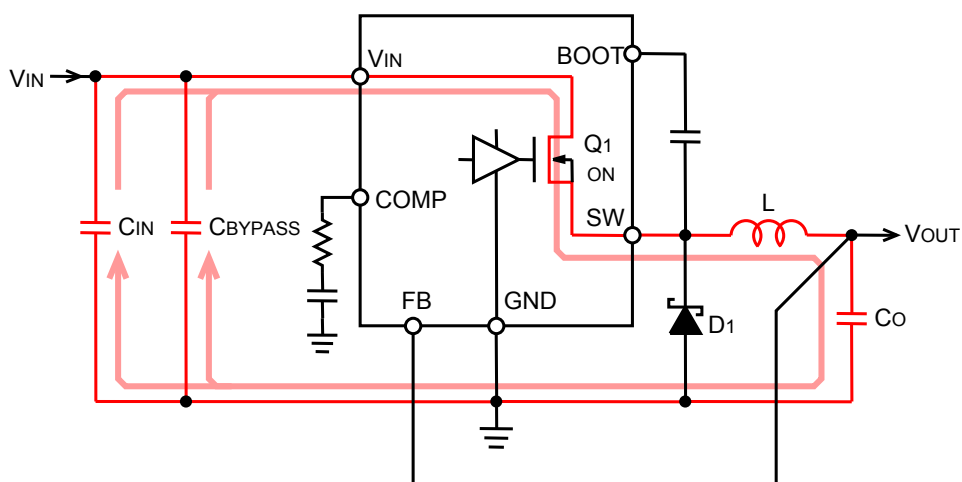


Figure 1-a. Current path when switching element Q1 is ON

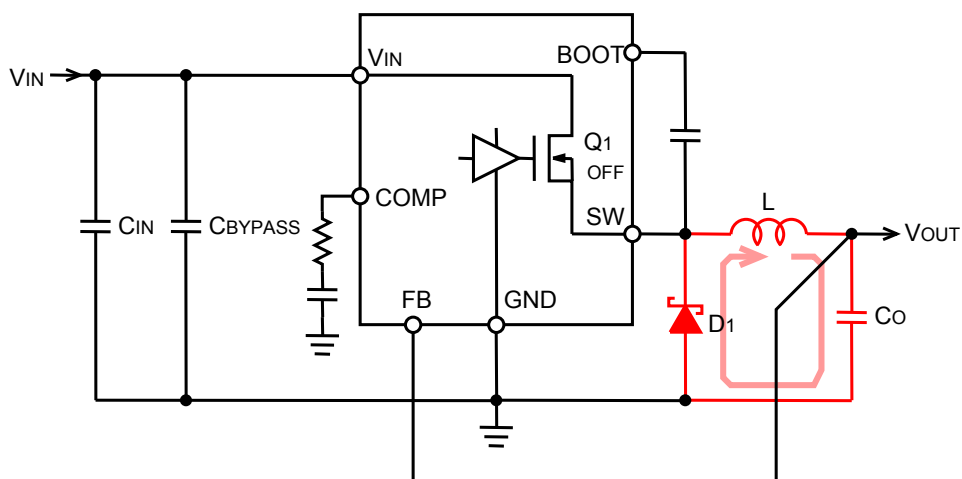


Figure 1-b. Current path when switching element Q1 is OFF

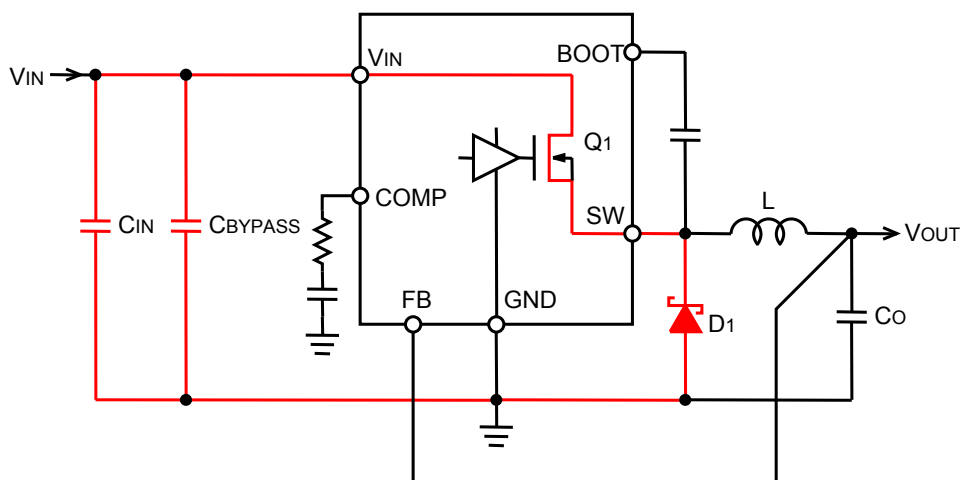


Figure 1-c. Current difference, an important part in layout

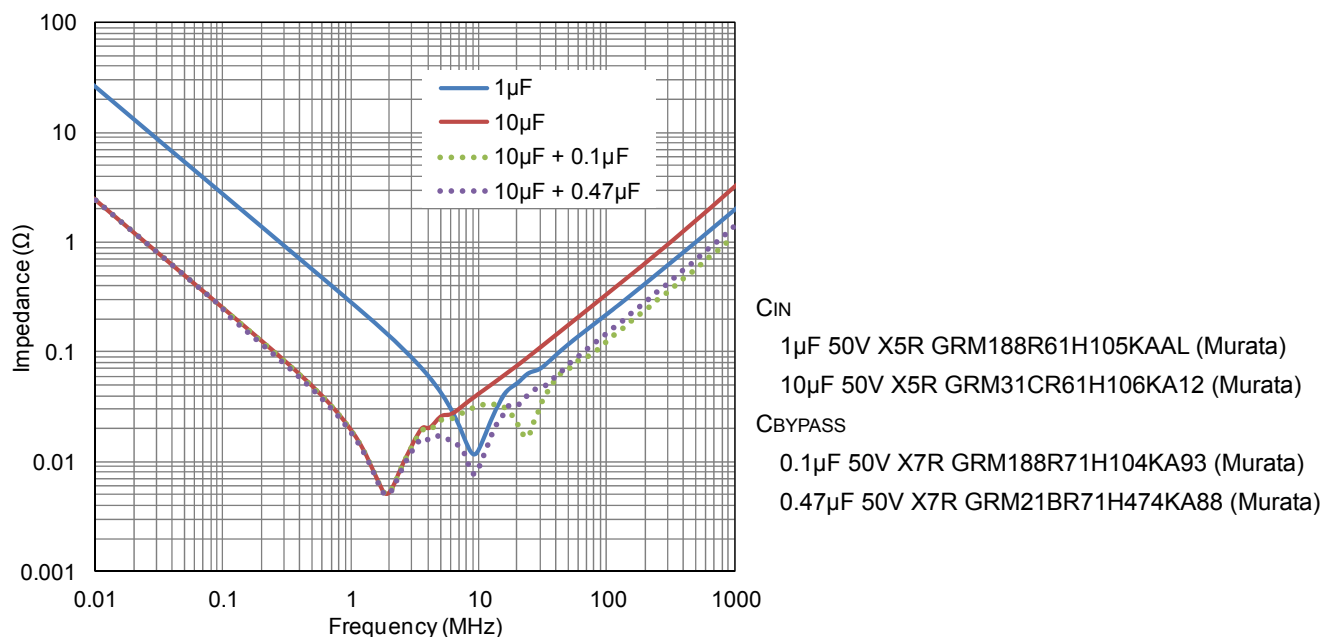


Figure 2. Frequency characteristics of Ceramic capacitor

Figure 3-f shows unsuitable layout. Voltage noise will be generated by the influence of wiring inductance for CBYPASS, VIN terminal and GND terminal of IC has some distance. Shortening the wiring even by 1mm is highly recommended.

In case of buck converter, high frequency of several hundred MHz will be loaded to the ground of CIN even with CBYPASS placed close to IC. Therefore placing ground of CIN and Co must be separated from each other by at least 1cm to 2cm.

Free-wheel diode D1 must be placed closer and on same surface of IC terminal. Figure 3-e shows suitable layout. With long distance between IC terminal and diode, the spike noise will be induced due to wiring inductance, that will be piled up at the output. Use short and wide wiring for free-wheel diode, and connect directly to GND terminal and switching terminal of IC. Do not place it on bottom surface layer through via, as noise will be worse, which is influenced by via inductance.

Figure 3-f shows unsuitable layout. Wiring inductance increases due to distance between diode and switching terminal, and GND terminal of IC and spike noise gets higher. To improve spike noise caused by unsuitable layout the RC snubber-circuit may be added as a countermeasure. This snubber-circuit must be placed closer to switching terminal and GND terminal of IC (Figure 3-g). Placing it at the both ends of diode will not absorb spike noise generated by wiring inductance. (Figure 3-h).

Introduce Thermal Via

Copper area of PCB contributes to heat dissipation, but because it does not have enough thickness, the heat dissipation result that meets area cannot be achieved from limited PCB size. Heat is dissipated using base material of board as a radiator. To deliver heat to opposite layer of the board efficiently and to highly reduce heat resistance, the thermal via are introduced.

Thermal via dimension of HTSOP-J8, reverse-side thermal pad package is shown in Figure 4. To increase heat conductivity, thermal via with small-diameter, inner diameter of 0.3mm which can fill solder, is recommended. With large diameter, problem of solder suction may occur at reflow solder process. Spacing between thermal via is about 1.2mm and placed directly below the thermal pad which is at the reverse-side of IC.

Place additional thermal via around IC like in Figure 3-a, if via below the IC's reverse-side thermal pad are not enough. Heat sink of HTSOP-J8 reverse-side thermal pad package is at ground potential, so EMI does not increase with wide copper pattern.

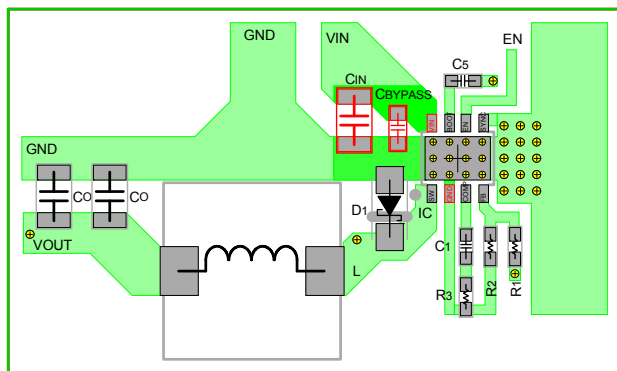


Figure 3-a. Placement of suitable input capacitor

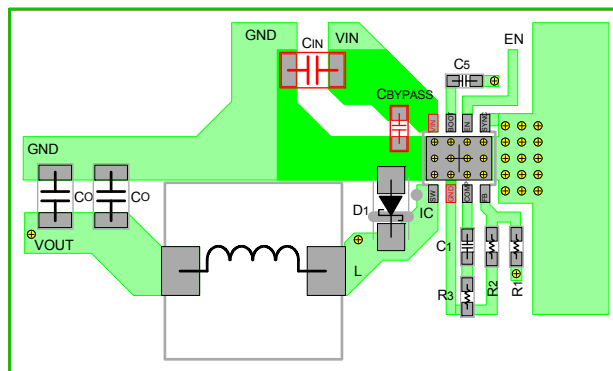


Figure 3-b. No problem with CIN separated about 2cm when CBYPASS is closely placed on same surface

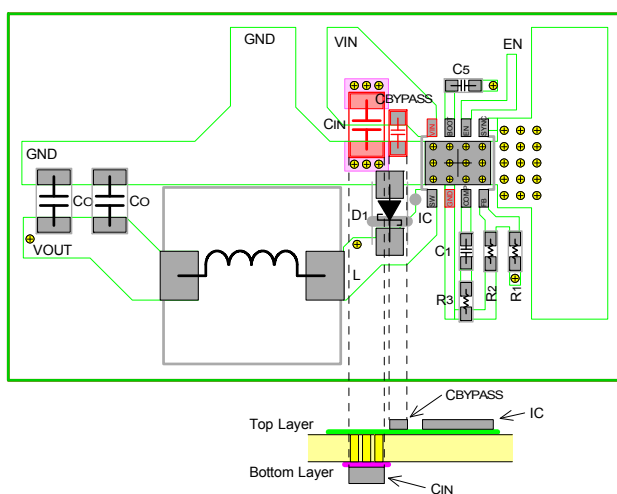


Figure 3-c. Increase of ripple voltage is concerned when CIN is placed on bottom layer.

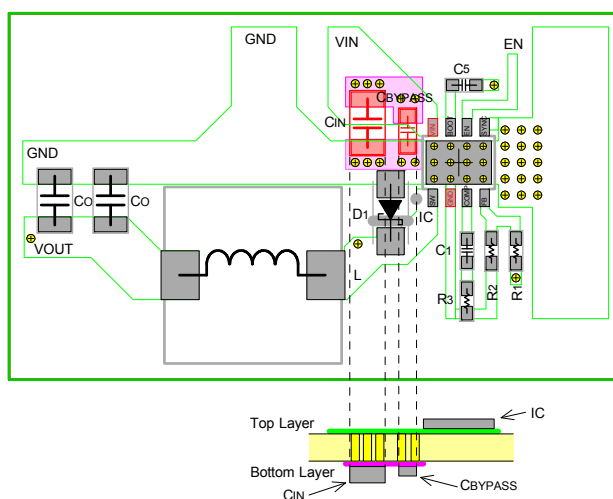


Figure 3-d. Unsuitable layout for input capacitor. Noise increased by via inductance

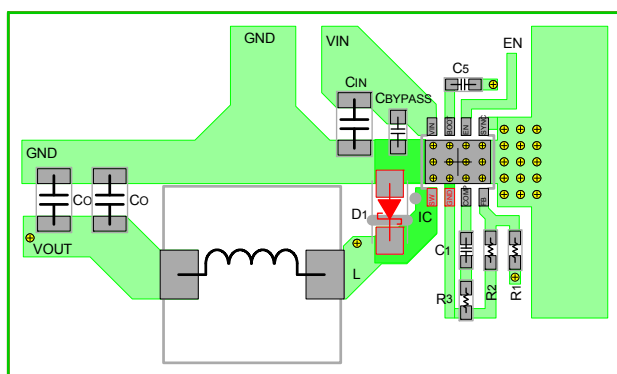


Figure 3-e. Suitable placement of free-wheel diode

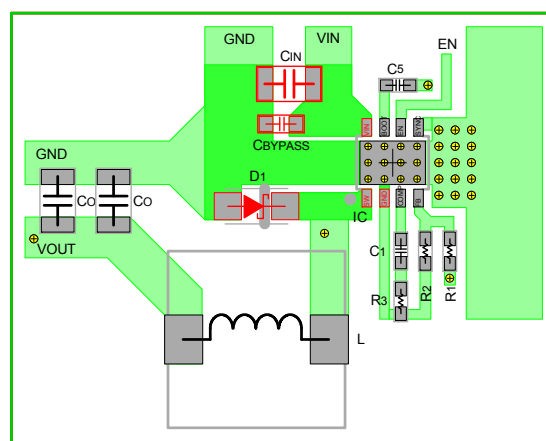


Figure 3-f. Unsuitable layout for diode

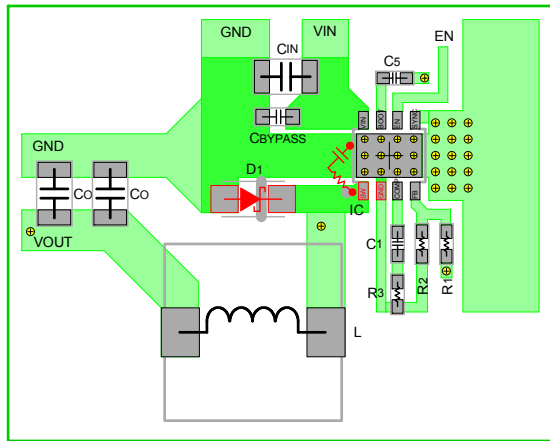


Figure 3-g. Suitable placement of snubber circuit

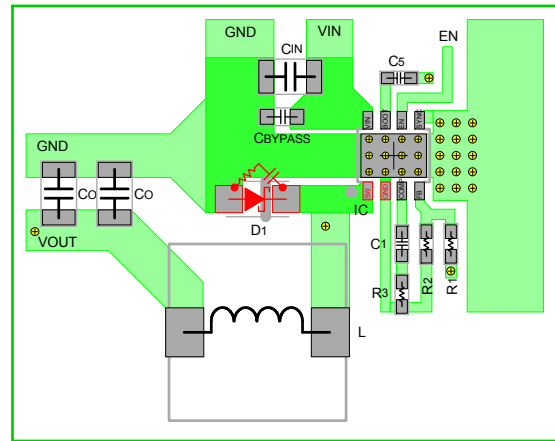


Figure 3-h. Unsuitable placement of snubber circuit

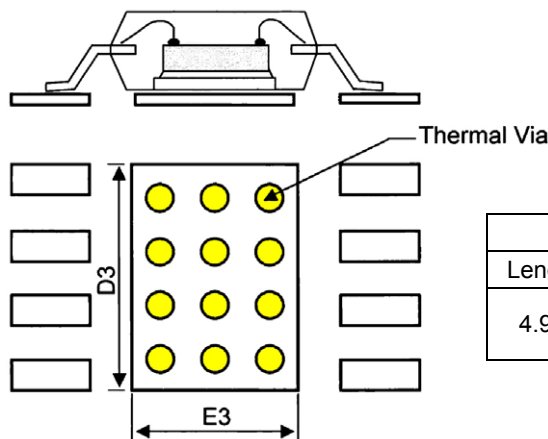


Figure 4. Thermal via dimension of reverse side thermal pad package

Placing Inductor

Place inductor close to IC, no need to place it as close as the input capacitor, to minimize radiation noise from switching node, and do not expand copper pattern area if not necessary. Increasing copper area is most likely to be thought of to improve wire resistance and to cool down device, but enlarged area may work as an antenna and may lead to increase in EMI.

Permissible current flow is one of the guideline to determine wiring width. Figure 5 shows a graph of rising temperature due to self-heating and conductor width when certain amount of current is flowing. For example, when 2A current is flowing through the wire with conductor thickness of 35μm, keeping conductor width of 0.53mm is suitable to prevent temperature to rise by 20°C.

Wiring can be affected by heat from surrounding parts and surrounding temperature, therefore using conductor width with enough margins is recommended. As an example, for 1 ounce (35μm) board conductor, width more than 1mm per 1A, and for 2 ounce (70μm) board conductor, width more than 0.7mm per 1A is used for wiring.

Figure 6-a shows layout considering wiring area from EMI point of view. Also, unsuitable layout which has unnecessary wide copper area is shown in Figure 6-b.

Not placing ground layer directly below the inductor (Figure 6-c) is also a point to pay attention to, when placing inductor. Due to the eddy current occurring in the ground layer, the inductor value decreases and the loss increases (decrease of Q) with set-off effect from line of magnetic force. Signal line other than ground also has the possibility of propagating switching noise caused by eddy current. It is better to avoid wiring directly under inductor. If wiring is unavoidable, please use closed magnetic circuit structured inductor with small leak from line of magnetic force.

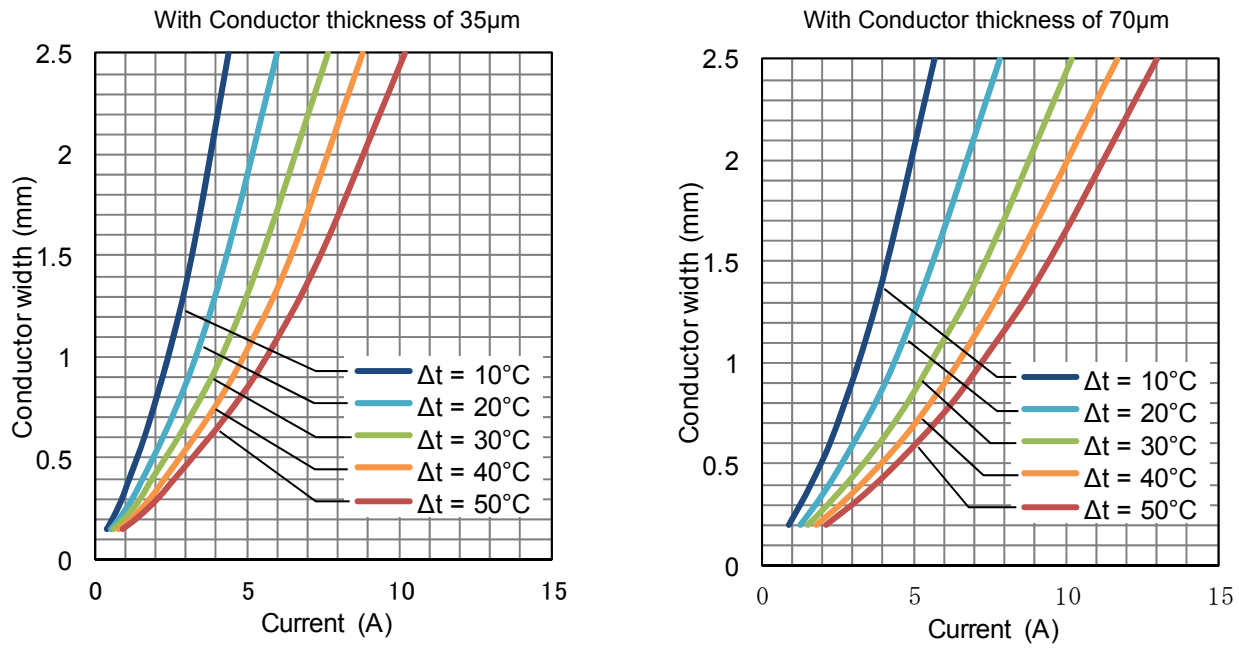


Figure 5. Temperature increase by wiring conductor thickness and width, with current flow

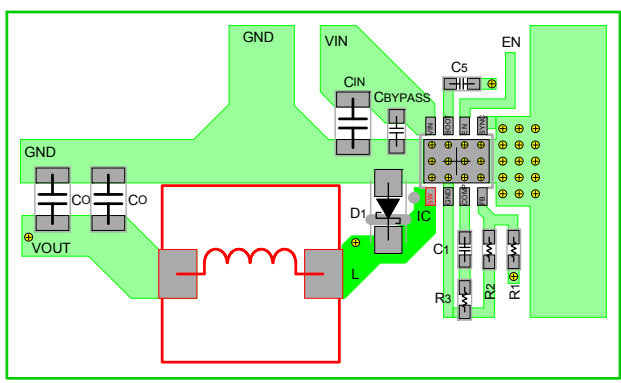


Figure 6-a. Suitable wiring to inductor

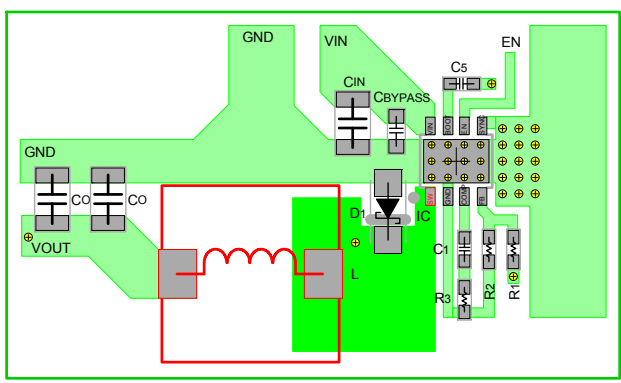


Figure 6-b. Unsuitable wiring to inductor
Unnecessary wide copper area

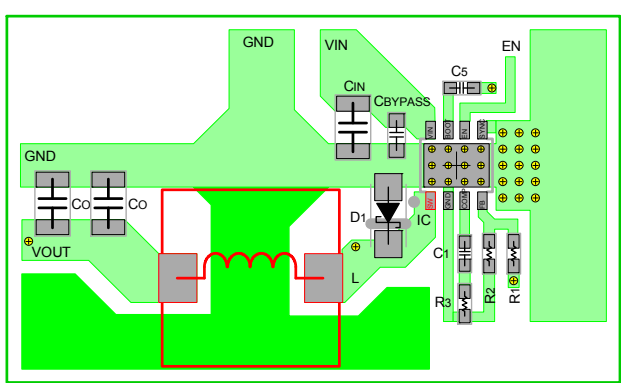


Figure 6-c. Unsuitable wiring directly below inductor

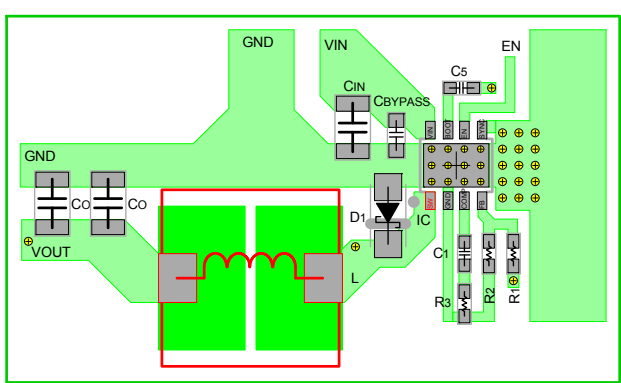


Figure 6-d. Unsuitable wiring between inductor terminals

Space between inductor terminals must also be paid attention. If distance between terminals are close like in Figure 6-d, high frequency signal of switching node is induced to output through stray capacitance.

Place Output Capacitor Close to Inductor

Output current is smooth in buck converter as inductor is inserted to output in series. Place output capacitor close to inductor; no need to place it as close as input capacitor. Because high frequency of several hundred MHz is loaded on ground of input, so placing ground of C_{IN} and C_O 1cm to 2cm apart is recommended. If they are close to each other, high frequency noise of input may be propagated to output through C_O .

Wire Feedback Route

Feedback signal route is a wire which needs most attention in signal wiring. If this wire has noise, an error will occur in output voltage and the operation will become unstable.

Figure 7-a, shows the points to be aware of when wiring feedback route.

- Feedback terminal of IC which inputs feedback signal, is normally designed with high impedance. Output of this terminal and resistor crossover network must be connected with short wire.
- Part which detects the output voltage must be connected after output capacitor or at both ends of output capacitor.
- Wiring the resistor-divider circuit nearby and parallel, makes it better for noise tolerance.
- Draw wire far away from switching node of inductor and diode. Do not wire directly below the inductor and diode, and not parallel to power supply line. Multilayer board must be also wired in the same way.

In wiring of Figure 7-b, the voltage drops due to resistor component of ground wiring and gets slightly affected by load regulation, but if voltage alternation is within target specification, this drawing is worth examining. Layout example is shown in Figure 7-c. Transfer the feedback route to bottom layer of PCB through via, and the layout away from the switching node.

Feedback route is laid parallel beside inductor in Figure 7-d. In this case, noise is induced to feedback route by magnetic field generated around the inductor.

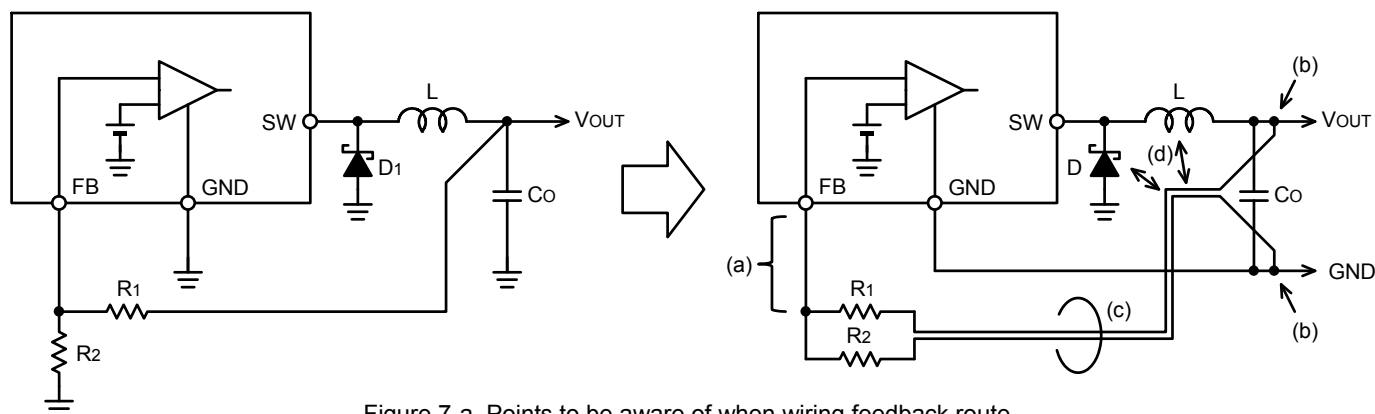


Figure 7-a. Points to be aware of when wiring feedback route

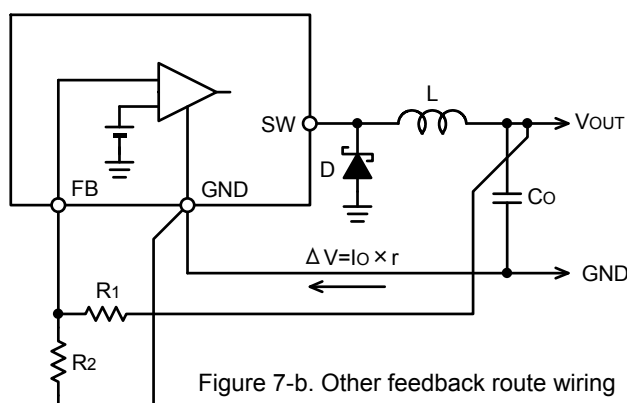


Figure 7-b. Other feedback route wiring

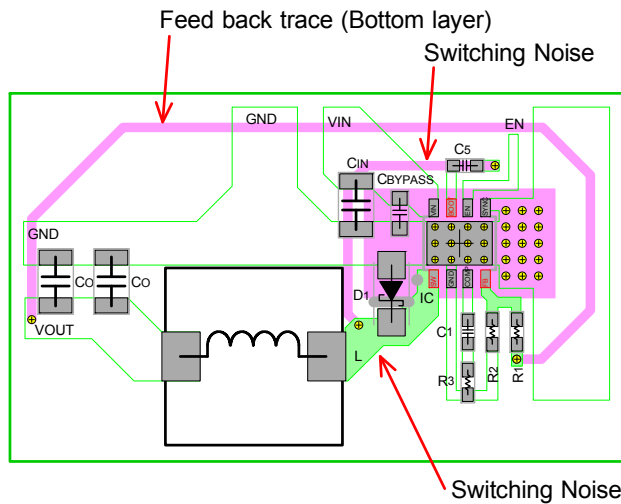


Figure 7-c. Layout example of feedback route.
Wiring through bottom layer

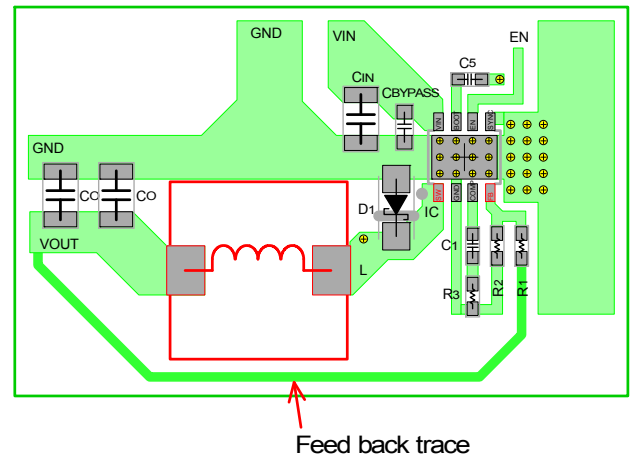


Figure 7-d. Unsuitable feedback route layout
Wiring beside inductor

Ground

Analog small-signal ground and power-ground must be isolated. Laying power-ground without separating from top layer is very ideal (Figure 8). Connecting isolated power-ground on bottom layer through via causes losses and aggravate the noise due to the effect of inductance and resistance of via. Providing ground plane in PCB inner layer and bottom layer is to reduce and shield DC loss, and to radiate heat better, but it is only a supplementary ground.

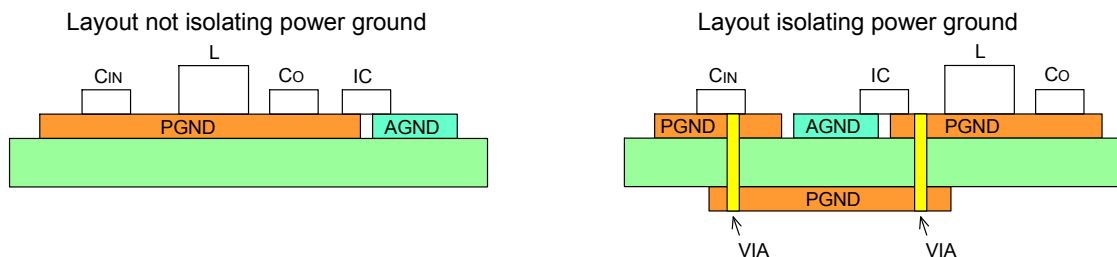


Figure 8. Layout of power ground

When placing ground plane on bottom layer, and in PCB inner-layers of a multilayer board, connection of input power-ground and the ground for free-wheel diode with high frequency switching noise, must be taken care. With power-ground plane in 2nd layer to reduce losses like in Figure 9, connect top layer and 2nd layer with many via and reduce impedance of power-ground. Also, with common-ground in 3rd layer, signal-ground in 4th layer, connect only the power-ground around output capacitor with lower high-frequency switching noise, to power-ground and 3rd / 4th layers. Never connect the power-ground with high noise of free-wheel diode and the input.

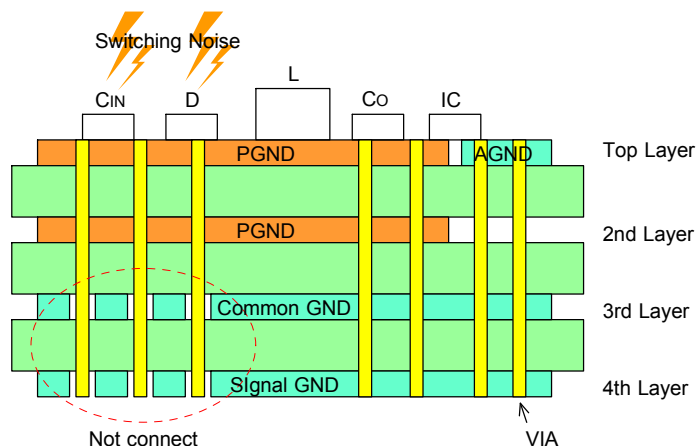


Figure 9. Power ground connecting method for multilayer board

Resistance of Copper and Inductance

1. Resistance of Copper

Figure 10 shows resistance value per unit area of copper. This resistor value is for copper thickness 35μm, width 1mm, and length 1mm.

General resistance can be calculated by following formula.

$$R = \frac{\rho \times l}{t \times w} \times 10 \quad [\text{m}\Omega] \quad (1)$$

l : Conductor length [mm]
 w : Conductor width [mm]
 t : Copper thickness [μm]
 ρ : Resistivity of copper [μΩ cm]
 $\rho(T=25^\circ\text{C}) = 1.72 \mu\Omega \text{ cm}$
 $\rho(T) = \rho(T_a=25^\circ\text{C}) \times \{1 + 0.00385(T-25)\} \quad [\mu\Omega \text{ cm}]$
 T : Temperature

Calculating from resistance value R_P per unit area referring to graph on the right,

$$R = R_P \times \frac{l}{w} \times \frac{35}{t} \quad [\text{m}\Omega] \quad (2)$$

R_P : Resistance value referred from graph [mΩ]
 l : Conductor length [mm]
 w : Conductor width [mm]
 t : Copper thickness [μm]

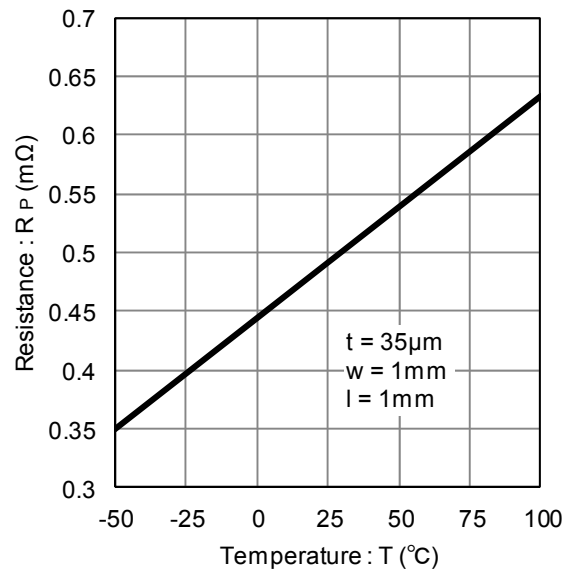


Figure 10. Resistance value per unit area of copper

For example resistance value at 25°C, width 3mm, length 50mm is $R = R_P \times \frac{l}{w} \times \frac{35}{t} = 0.49 \times \frac{50}{3} \times \frac{35}{35} = 8.17 \quad [\text{m}\Omega]$

Voltage drop when 3A current is flowing becomes 24.5mV. In case of temperature at 100°C the resistance value increases 29% and voltage drop becomes 31.6mV.

2. Inductance of Copper

Inductance of copper is calculated by following formula. In PCB wiring the inductance value does not totally depend on thickness of copper.

$$L = 0.2 \times l \times \left(\ln \frac{2 \times l}{w + t} + 0.2235 \times \frac{w + t}{l} + 0.5 \right) \quad [\text{nH}] \quad (3)$$

l : Conductor length [mm]
 w : Conductor width [mm]
 t : Copper thickness [mm]

Calculated value of copper inductance is shown in Figure 11.

This graph shows that inductance value does not drop as much as expected even with doubled line width. To control the effect from parasitic inductance wiring shorting is the best solution

When current that propagate print pattern of inductance L [H] changes i [A] to time t [s], following voltage occurs in both ends of print pattern.

$$|V| = L \times \frac{di}{dt} \quad [\text{V}] \quad (4)$$

For example, when 2A current flow in 6nH print pattern for 10ns the following voltage is generated.

$$|V| = 6 \times 10^{-9} \times \frac{2}{10 \times 10^{-9}} = 1.2 \quad [\text{V}] \quad (5)$$

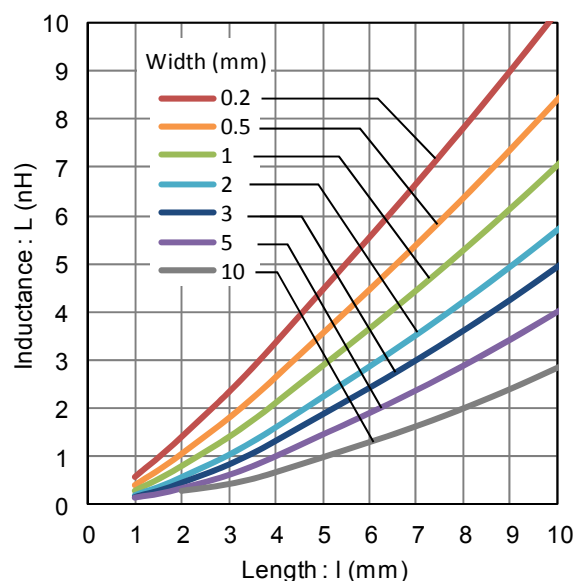


Figure 11. Inductance of Copper

Resistance and Inductance of Via

1. Resistance of Via

Resistance of via can be calculated by following formula. Figure 12 shows via resistance value when board thickness 1.6mm metal planting thickness 0.015mm (15μm)

$$R_v = \frac{\rho \times h}{\pi \left\{ \left(\frac{d}{2} \right)^2 - \left(\frac{d}{2} - t_m \right)^2 \right\}} \times 0.01 \quad [\text{m}\Omega] \quad (6)$$

h : Board thickness [mm]

d : Via diameter [mm]

t_m : Through hole metal planting thickness [mm]

ρ : Copper resistivity [μΩ cm]

$$\rho(T=25^\circ\text{C}) = 1.72 \mu\Omega \text{ cm}$$

$$\rho(T) = \rho(T_a=25^\circ\text{C}) \times \{1 + 0.00385(T-25)\} \quad [\mu\Omega \text{ cm}]$$

T : Temperature

2. Inductance of Via

According to Frederick W. Grover the inductance of via can be calculated by following formula. Figure 13 shows the result.

$$L = \frac{h}{5} \times \left(\ln \frac{4 \times h}{d} + 1 \right) \quad [\text{nH}] \quad (7)$$

h : Board thickness [mm]

d : Via diameter [mm]

Wire bending in right angle makes EMI worse even with small inductance. Refer to “Corner wiring” described at end of this page.

3. Allowable Current of Via

π multiplied by diameter of Via is equivalent to line width. Allowable current value can be expected from the graph on Figure 5, the temperature increases with conductor current, but current capacity will drop compared to conductor thickness 35μm graph for via metal planting thickness is 18μm.

In previous wiring passage, conductor width of more than 1mm/A was recommended in wiring when conductor thickness was 35μm. But in case of via, half of the thickness is metal planting, so conductor width of more than 2mm/A is recommended. Figure 14 shows example of allowable current.

Number of via must be placed so the value of allowable current, resistance, inductance satisfies with the standards of the usage.

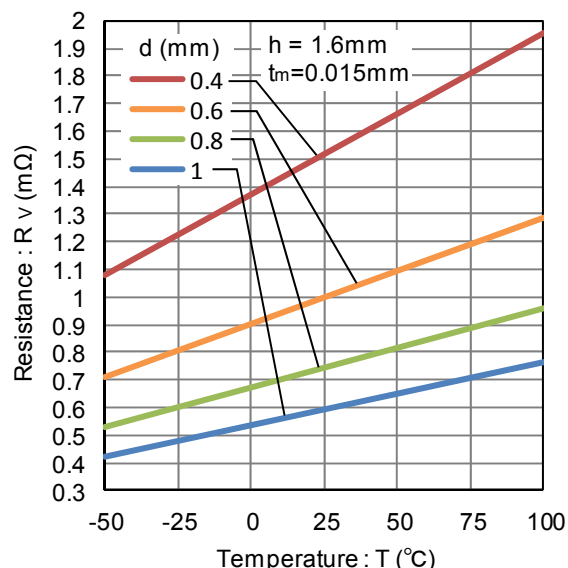


Figure 12. Resistance of Via

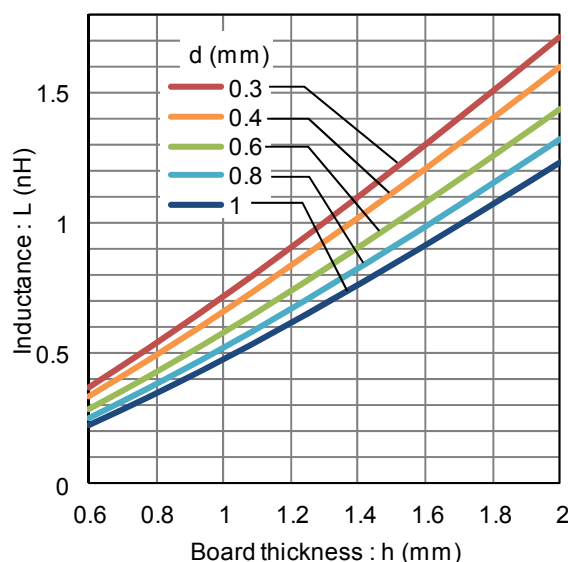


Figure 13. Inductance of Via

Via diameter d (mm)	Conductor width d×π (mm)	Allowable Current (A)
0.3	0.94	0.4
0.4	1.26	0.6
0.6	1.88	0.9
0.8	2.51	1.2
1	3.14	1.5

Figure 14. Example of allowable current of via

Corner Wiring

Bending corner wiring in right angle can cause current waveform to reflect and to be disordered for impedance changes at the corner. Wire with high frequency such as switching node causes EMI to degenerate. Corner must be bent at 45° or circularly. With bigger diameter of bending, smaller will be the change in impedance.



Figure 15. Layout of Corner wiring

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