Effectiveness Analysis of Low Power Technique of Dynamic Logic under Temperature and Process Variations

Jinhui Wang*, Wuchen Wu, Na Gong, Wang Zhang, and Ligang Hou

Abstract — *Using multiple-parameter Monte Carlo method, the effectiveness of the dual threshold voltage technique (DTV) in low power domino logic design is analyzed. Simulation results indicate that under significant temperature and process variations, DTV is still highly effective to reduce the total leakage and active power consumption for domino gates with speed loss. Also, regarding power and delay characteristics, different structure domino gates with DTV have different robustness against the temperature and process variation*[1].

Index Terms — domino gate, temperature and process variation, effectiveness.

I. INTRODUCTION

Dynamic circuits, in particular domino gates are often applied in high speed digital circuits due to their fast evaluation and small area merits [1]-[3]. However, as technology scales down, the leakage power of domino logic increases exponentially with the scaling of the threshold voltage (V_t) and gate oxide thickness (t_{ox}). By the sub-65nm generation, leakage power may constitute as much as 50 percent of the total power consumption [4], [5].

The dual threshold voltage technique (DTV) [6] is one of most popular techniques to suppress leakage power. However, as the technology scales down below 65 nm node, the increasing die-to-die and with-in chip variations bring a great challenge to low power techniques, including DTV. Two main contributors to variations are changes in process parameters and changes in operating temperatures. Also, the exponential relation between leakage current and temperature makes the effect of process variations vary at different temperature. Therefore, there exists the need to investigate the effectiveness of DTV under process and temperature variations to help designers judge if the DTV application in circuits could meet the frequency-leakage requirements in sub-65 nm era. Many researchers have utilized Monte Carlo method to analyze the effectiveness of DVT with variations, but they still could not solve the problem completely. Some of them only focus on one variation and ignore the relations of two variations [7]. Others analyze process variations only under worse case temperature and fail to consider the uniform change of temperature in practice [4], [8]. In this paper, utilizing multiple-parameter Monte Carlo method, the effectiveness of DTV in low power domino logic is analyzed at the presence of simultaneous variations of process and temperature.

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II. DYNAMIC CIRCUITS WITH DTV

DTV could suppress the leakage power efficiently and therefore it has been applied widely in VLSI design [6]. As can be seen from Fig.1, taking the domino OR gates with DTV as an example, the critical signal transitions determining the domino circuit delay occur along the evaluation path. In a dual V_t domino circuit, therefore, all of the transistors, activated during the evaluation phase (Nclk, N1……Nn, Pr), have a low V_t. Alternatively, the precharge/predischarge phase transitions (P1, P2, Nr) are not critical for the performance of a domino circuit and they are high V_t transistors [9]. It is operated as follows. In the precharge phase, the clock is set low. P1 is turned on. And the evaluation phase begins when the clock is set high. P1 is cut off. Provided that the necessary input combination to discharge the evaluation node is applied, the circuit evaluates and the dynamic node is discharged to ground. Otherwise, the high state of the dynamic node will be preserved until the following precharge phase [10].

In the idle stage, the leakage power of domino circuits is produced by leakage current which is dominated by the sub-threshold leakage current, which can be expressed by equation (1) [11]. In the active stage, the active power of domino circuits also contains two parts: the dynamic switching power and the leakage power.

$$I_{sub} = u_{eff}\frac{W_{eff}}{L_{eff}}\sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\Phi_s}}V_T^2\exp\left(\frac{V_{gs}-V_t}{nV_T}\right)\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right) \quad (1)$$

where u_{eff}, W_{eff}, L_{eff}, ε_{si}, N_{ch}, Φ_s, and V_T are effective carrier mobility, effective channel width, effective channel length, thermal voltage, permittivity of silicon, effective channel doping, surface potential and sub-threshold swing, respectively. From (1), it can be seen that the sub-threshold leakage current decreases exponentially with the increasing of V_t. Thus, DTV can lower both the leakage and active power.

III. TEMPERATURE AND PROCESS VARIATIONS

Process variations occur due to proximity effects in photolithography, non-uniform conditions during deposition, random dopant fluctuation, etc. [12]. These cause fluctuations in parameters such as channel length, width, oxide thickness,

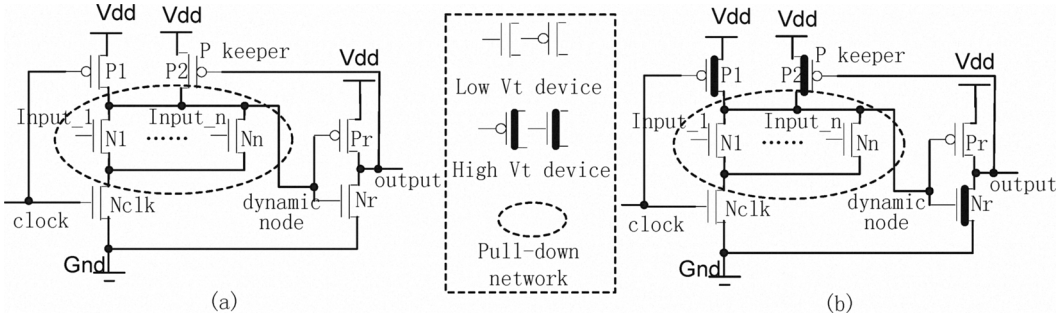

Fig.1 Domino OR gates (a) domino gate with Low V_t (b) domino gate with dual V_t

as well as dopant concentrations, and result in variations in V_t which determines the delay and the leakage of the circuits. Among the variations in transistor parameters, variations in gate length and threshold voltage are found to have the most significant impacts on circuit performance and power consumption [7]. The standard deviation of the intrinsic threshold voltage for long channel devices is analytically modeled as:

$$\sigma V_t = \left(\frac{q}{t_{ox}}\right)\sqrt{\frac{N_{ch}W_{DEP}}{3WL}} \quad (2)$$

where q is the charge, t_{ox} is the gate oxide capacitance, N_{ch} is the weighted doping concentration, W_{DEP} is the channel depletion width, and W and L are the channel width and gate length, respectively. This equation is derived for long channel devices which do not exhibit short channel effects. As shown in equation (2), the variation in threshold is caused by the doping un-uniformity and is proportional to the square root of doping concentration and inversely proportional to the square root of device gate length and channel width.

In nanometer technologies, the shorter device gate length reduces the effective threshold voltage to

$$V_{th} = V_{th0} - \Delta V_{th}\left(V_{th}\_roll\_off\right) - \Delta V_{th}\left(DIBL\right) \quad (3)$$

where V_{th0} is the intrinsic threshold voltage, $\Delta Vth(Vth\_roll\_off)$ and $\Delta Vth(DIBL)$ are the drop in threshold voltage due to short channel effect and *DIBL,* respectively. The relation between the gate length and threshold roll-off and DIBL is exponential and thus when there are variations in gate length, the net effect is increased variation in threshold voltage.

Changes in the operating temperature occur due to power dissipation in the form of heat. On-chip thermal variations have a significant bearing on the mobility of electrons and holes, as well as the threshold voltage of the devices. An increase in the operating temperature causes the mobility to decrease, thereby decreasing the on-current, which, in turn, can reduce the speed of the circuit. Further, elevated temperatures also lead to an increase in the leakage current [13]. The impact of temperature fluctuations on the leakage current and V_t in a MOSFET is identified utilizing BSIM4 MOSFET equations. V_t and u_{eff} of a MOSFET are [14]

NMOS:

$$V_t(T) = V_t(T_0) + \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff}KT2\right)\times\left(\frac{T}{T_0} - 1\right) \quad (4)$$

PMOS:

$$V_t(T) = V_t(T_0) - \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff}KT2\right)\times\left(\frac{T}{T_0} - 1\right) \quad (5)$$

$$u_{eff}(T) = \left(U_0\left(\frac{T}{T_0}\right)^{U_{te}}\right)\cdot \left\{1 + \left(\frac{V_{gsteff} + 2V_t(T)}{T_{OXE}}\right)^2 U_b(T) + \left(U_c(T)V_{bseff} + U_a(T)\right)\left(\frac{V_{gsteff} + 2V_t(T)}{T_{OXE}}\right)\right\}^{-1} \quad (6)$$

where *KT1, KT1L, KT2, V_{bseff}, U_0, U_{te}, T_{OXE}, U_a, U_b, U_c, T_0,* and T are the temperature coefficient for threshold voltage, channel length dependence of the temperature coefficient for threshold voltage, body-bias coefficient of threshold voltage temperature effect, effective substrate bias voltage, mobility at the reference temperature, mobility temperature exponent, electrical gate-oxide thickness, first order mobility degradation coefficient, second order mobility degradation coefficient, body effect of mobility degradation coefficient, reference temperature, and the operating temperature, respectively. *KT1, KT1L,* and *KT2*, are constant empirical parameters while U_a, U_b, and U_c, are temperature dependent. (1), (4), (5), and (6) indicate that temperature fluctuation lead the variation of V_t which determines the delay and the leakage of the circuits.

IV. Monte Carlo Analysis

TABLE I
PARAMETER OF DEVICES

Technology Node	45nm	
	Low V_t	High V_t
NMOS threshold voltage	0.22V	0.35V
PMOS threshold voltage	-0.22V	-0.35V
Supply voltage	0.8V	0.8V

In this section, a quantitative analysis is provided to investigate the effectiveness of DTV in suppressing the power consumption of domino gates under temperature and process fluctuations. Domino circuits with different structures of the pull-down networks (PDN), such as 2-input, 4-input, 8-input, and 16-input domino OR gate (OR2, OR4, OR8, and OR16, respectively), 2-input and 8-input domino AND gates (AND2 and AND8), 2-bit and 16-bit domino multiplexer (MUX2 and

MUX16), are employed as the benchmark circuits. They are simulated based on 45nm BSIM4 models [15] by the HSPICE tool. Each domino gate drives a capacitive load of 8fF. The parameters of devices are listed in table I. All gates are turned to operate at 1GHZ clock frequency and W/L in PDN is set to 5-20 [16]. When simulating the leakage power, all of the domino OR gates are set in CHIH (clock=1, In_1= In_2=… In_n =1) state, which can ensure every gates in the lowest leakage state [6].

To evaluate the impact of process and temperature variations on the effectiveness of DTV, process and temperature variations aware power and speed characteristics of domino circuits with DTV is evaluated using multiple-parameter Monte Carlo analysis. In our simulation, three most important process parameters to influence the performance of the MOSFET are considered: gate length (L_{gate}), channel doping concentration (N_{ch}), and gate oxide thickness (t_{ox}). And these parameters are all assumed to have normal Gaussian statistical distributions with a three sigma (3σ) variation of 10%. In addition, temperature is assumed to have uniform distribution and varies the normal value (75°C) by ±50°C. 1000 Monte Carlo simulations are run to evaluate the power and delay distribution of different domino gates.

Taking 4-input dual V_t OR gate as an example, its leakage power, active power and delay characteristics at the presence of process and temperature variations are shown in Fig. 2. As can be seen from it, the leakage power distribution curves of the low V_t and dual V_t domino OR gates cross at 388nW. Leakage power consumption of 88% of the samples with DTV is lower than 388nW. Alternatively, 70% of the samples with the low V_t transistors consume leakage power higher than 388nW. These results indicate that DTV is highly effective to reduce the total leakage power consumption even under significant process and temperature variations. Also, two active power distribution curves intersect at 15uW. The active power consumption of 91% of the dual V_t samples is lower than 15uW and 90% of the low V_t samples consume active power higher than 15uW. This is because the active power consists of the switching power and the leakage power and DTV can be effective to suppress leakage power, thereby reducing the total active power.

As also can be seen from Fig. 2, the delay of all 4-input OR sample gates (100%) with DTV is lower than 490pS, while that of all low V_t samples (100%) is higher than 490pS. Obviously, under the effect of the temperature and process variations, the inferior speed characteristics of the high V_t transistors in circuit with DTV still induce the speed penalty as expressed in equation (7) [9]

$$v \propto \frac{V_{dd}^{0.3}\left(1-\frac{V_t}{V_{dd}}\right)^{1.3}}{t_{ox}^{0.5}} \quad (7)$$

where v is the speed of the transistor, and other parameters have their usual meanings. (7) shows that v decreases greatly as V_t increases,

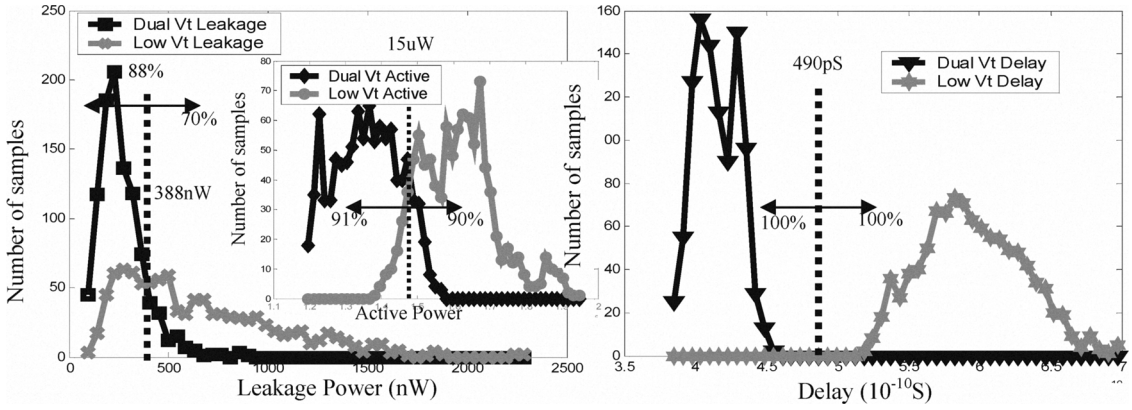

Fig. 2 Leakage power, active power and delay distribution of 4-input dual V_t domino OR gate

TABLE II

DISTRIBUTION OF LEAKAGE POWER, ACTIVE POWER AND DELAY OF THE DOMINO GATES (L: LEAKAGE POWER; A: ACTIVE POWER; D: DELAY)

Gate	Cross			Dual Vt			Low Vt		
	L/nW	A/uW	D/pS	L<Cross/%	A<Cross/%	D>Cross/%	L>Cross/%	A>Cross/%	D<Cross/%
OR2	279	13	480	93	77	100	72	70	100
OR4	388	15	490	88	91	100	70	90	100
OR8	611	16	530	86	74	100	70	66	100
OR16	938	19	540	65	66	100	60	79	100
AND2	705	19	591	82	87	100	61	64	100
AND8	2021	20	676	69	61	100	52	90	100
MUX2	388	22	460	88	86	100	70	95	100
MUX16	1650	23	632	63	96	100	61	94	100

TABLE III
THE AVERAGE AND STANDARD DEVIATIONS (SD) OF THE DOMINO GATES (L: LEAKAGE POWER; A: ACTIVE POWER; D: DELAY)

Gate	Dual Vt			Low Vt		
(Average/SD)	L(nW)	A(uW)	D(pS)	L(nW)	A(uW)	D(pS)
OR2	195/72.0=2.70	13/0.94=13.83	589/34.8=16.91	590/371=1.58	15.4/1.1=14.00	425/15.2=28.00
OR4	286/115=2.49	13.1/0.9=14.89	598/35.4=16.91	682/394=1.73	16.2/1.1=15.12	417/15.1=27.64
OR8	467/200=2.33	15.0/1.0=15.03	656/45.6=15.07	865/450=1.92	17.2/1.1=15.54	446/12.2=36.68
OR16	913/411=2.22	18.7/1.2=16.22	489/32.7=17.97	1338/625=2.14	21.0/1.2=18.23	315/12.2=25.85
AND2	583/253=2.30	18.1/1.00=18.1	683/29.5=23.19	984/491=2.01	20.2/1.84=10.99	450/11.0=40.90
AND8	1939/868=2.23	19.6/2.00=9.79	787/25.8=30.47	2398/1089=2.20	23.5/2.62=8.98	584/15.6=37.27
MUX2	285/114=2.49	21.9/0.89=24.5	532/28.8=18.45	685/398=1.72	24.4/1.01=23.10	409/16.10=25.37
MUX16	1711/754=2.27	21.5/0.87=24.61	544/36.8=14.78	2.64/934=2.21	24.8/1.11=22.28	362/12.75=28.43

Table II lists the leakage power, active power and delay characteristics of OR2, OR4, OR8, OR16, AND2, AND8, MUX2, and MUX16 domino gates. As indicated in it, with the increasing number of the inputs, the values of the point of intersection of the leakage power, active power and delay all increase gradually. As to leakage power and active power, over 50% samples of all of the dual V_t domino gates are smaller than the cross, and alternatively over 50% samples of all of the low V_t domino gates are lager than the cross. Therefore, under the effect of the temperature and process variations, DTV is still quite effective to reduce the total leakage and active power consumption for all style of domino gates with speed loss.

The average and standard deviations (SD) of dual V_t and low V_t domino gates are listed in Table III. The Average/SD values of the leakage power of all the dual V_t gates are larger than that of the low V_t gates, which shows that DTV can sustain the availability of suppressing leakage power with the process and temperature variation.

Also can be seen form Table III, the Average/SD value of delay of all domino gates with DTV are less than that of the low V_t gates and therefore DTV could weaken the immunity of the domino gates to process and temperature variation regarding the delay characteristics.

In addition, as to domino OR gates with DTV, the Average/SD value of active power are less than that of the low V_t OR gates, but the Average/SD value of active power of AND and MUX gates with DTV are larger than that of the low V_t gates. This is because in the PDN of AND and MUX gates, the transistors are cascaded and thereby produce stack effect to lower the leakage power, which improve the robustness of domino gates against effect of process and temperature variation.

V. CONCLUSION

Effectiveness of the dual threshold voltage technique (DTV) in domino logic design is analyzed based on multiple-parameter Monte Carlo simulation. Simulation results indicate that DTV is highly effective to reduce the total leakage and active power consumption for domino gates with speed loss under significant temperature and process variations. And DTV can sustain the availability of suppressing leakage power in domino gates with different structures. However, DTV could weaken the immunity of the domino gates to process and temperature variation regarding the delay characteristics. As to the active power, the domino AND and MUX gates with DTV have more robustness against process and temperature variation than domino OR gates.

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