New Step-Up/Step-Down DC–AC Converter

Gleyson Luiz Piazza and Ivo Barbi, *Fellow, IEEE*

***Abstract*—This paper introduces a new dc–ac converter with the feature that it produces an instantaneous output voltage higher or lower than the input dc voltage without an intermediate power stage or transformers. This feature is provided by using one switching cell including two switches, two diodes, one inductor, and one capacitor on each inverter leg. Validating the theoretical analysis, a prototype was designed, built, and tested for an output rated power of 1 kW, a dc input voltage of 96V_{dc}, and output voltage of 110 V_{rms}. Furthermore, the fundamental output frequency was established at 60 Hz and the switching frequency at 20 kHz.**

***Index Terms*—DC–AC converter, switching cell.**

I. Introduction

DC–AC converters are devices developed to convert a continuous input voltage to an alternated output voltage, whose instantaneous value, in several situations, may become higher than the input voltage. There are different approaches to this kind of application, as presented in [1]–[20]. Discussions related to the use of the step-up converter for different purposes can be found in [1]–[8]. According to [1], it is possible to obtain a step-up static gain employing two dc–dc boost converters, connecting the load in a differential form and applying a 180° phase-shift modulation in each converter. Similar analysis can be extended to other dc–dc converters explored in the literature.

The Z-source structure is another alternative for inverters whose topology provides the step-up feature, since it is possible to combine the inductances and capacitances in order to obtain a single impedance between the input and output, as described in [9]–[15]. Additionally, [16]–[20] present an intermediate power stage connected in cascade with the inverter stage, leading to a two-stage structure.

This paper proposes a new topology for voltage inverters, in an application where the instantaneous output voltage can be higher or lower than the input dc voltage. From theoretical and experimental results, some important aspects related to the proposed converter can be highlighted:

1) the converter operates with the step-up/step-down feature;
2) the output inductor and output capacitor designs are not dependent on the duty cycle;
3) the constructive aspects have similarities with the buck inverter.

Manuscript received June 14, 2013; accepted July 26, 2013. Date of current version April 30, 2014. Recommended for publication by Associate Editor J. R. Espinoza.

The authors are with the Department of Electrical Engineering (EEL), Power Electronics Institute (INEP), Federal University of Santa Catarina (UFSC), Florianópolis 5119-88040-970, Brazil (e-mail: gleyson@inep.ufsc.br; ivobarbi@inep.ufsc.br).

Digital Object Identifier 10.1109/TPEL.2013.2277961

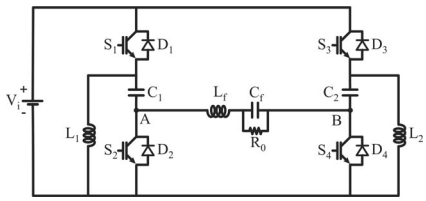


Fig. 1. Proposed output power stage of converter.

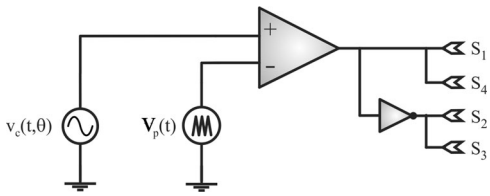


Fig. 2. Representative scheme of the bipolar modulator applied to the proposed converter.

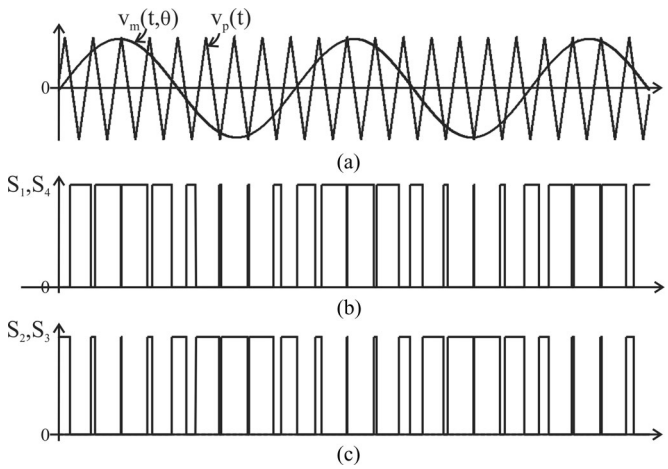


Fig. 3. Waveforms obtained for bipolar modulation: (a) modulator signal and triangular carrier signal; (b) signals applied in switches S_1 and S_4; (c) signals applied in switches S_2 and S_3.

II. Proposed Converter, Operation Principle, and Waveforms

The proposed dc–ac converter output power stage is shown in Fig. 1. This structure is composed of an input voltage source V_i, a high frequency filter formed by L_f and C_f, a load resistance R_0, and two switching cells, whose elements are S_1, D_1, C_1, S_2, D_2, and L_1 and S_3, D_3, C_2, S_4, D_4, and L_2, respectively.

Several modulation strategies can be applied to control the proposed converter, for example, space vector, unipolar, and bipolar modulations; however, in this study, a bipolar modulation scheme is employed. From the representative diagram in Fig. 2, the waveforms indicated in Fig. 3 were obtained.

0885-8993 © 2013 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

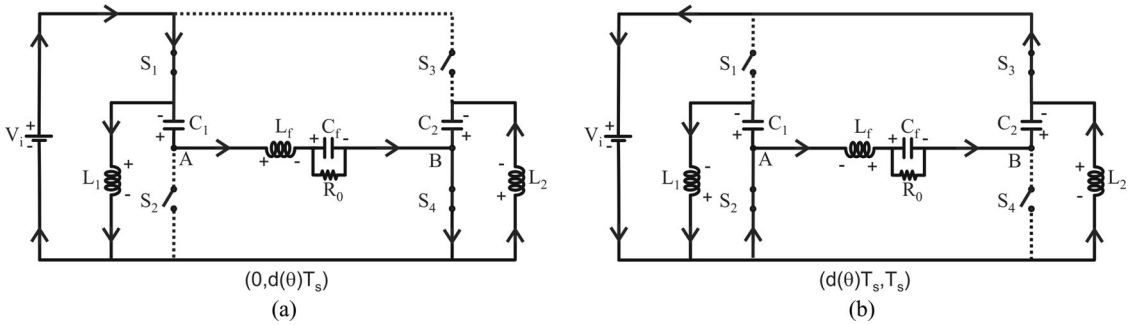


Fig. 4. Equivalent circuits for duty cycle higher than 0.5: (a) stage related to the interval (0, $d(\theta)T_S$); (b) stage related to the interval $(d(\theta)T_s, T_s)$.

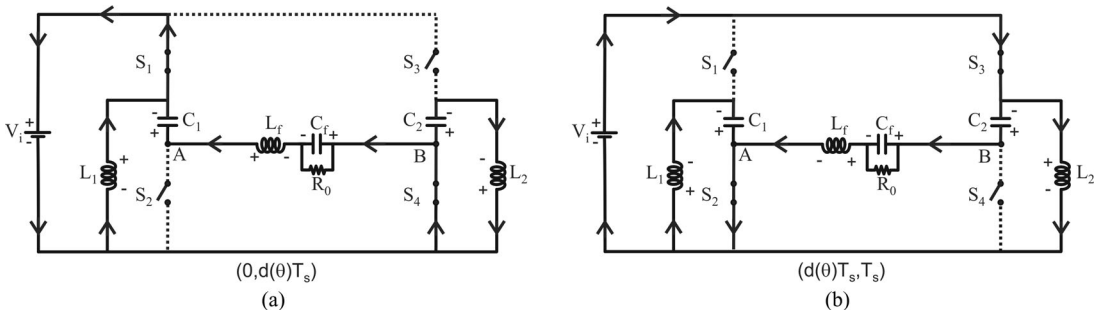


Fig. 5. Equivalent circuits for duty cycle lower than 0.5: (a) stage related to the interval (0, $d(\theta)T_S$); (b) stage related to the interval $(d(\theta)T_s, T_s)$.

It is important emphasize that the system waveforms present a high frequency (from commutation) and a low frequency (from grid) component. In order to standardize the system mathematical and graphical descriptions, the variable time (t) will be employed to represent the system from the switching period point of view and the variable angle (θ) will describe the system from the grid period point of view.

In order to gain an understanding of the system operation stages, the switches presented in Fig. 1 will be replaced by their bidirectional models. In order to illustrate the equivalent circuits of the system, two particular cases were chosen: the first refers to system operation with a duty cycle higher than 0.5, as shown in Fig. 4, and the second the system operates with a duty cycle lower than 0.5, as depicted in Fig. 5.

On comparing Figs. 4 and 5, it can be noted that the equivalent circuits for the two cases are similar, thus, for an extended analysis, only the stages represented by Fig. 4 will be considered.

Fig. 6 shows the voltage between terminals A and B, the voltage across capacitor C_f, the current across inductor L_f and the command signals applied to switches S_1, S_4, S_2, and S_3. Inductor voltage, current through L_1, L_2 and input current and the command signals applied to switches S_1, S_4 are shown in Fig. 7. Capacitor voltage, current through C_1, C_2 and the command signals applied to switches S_1, S_4 are shown in Fig. 8.

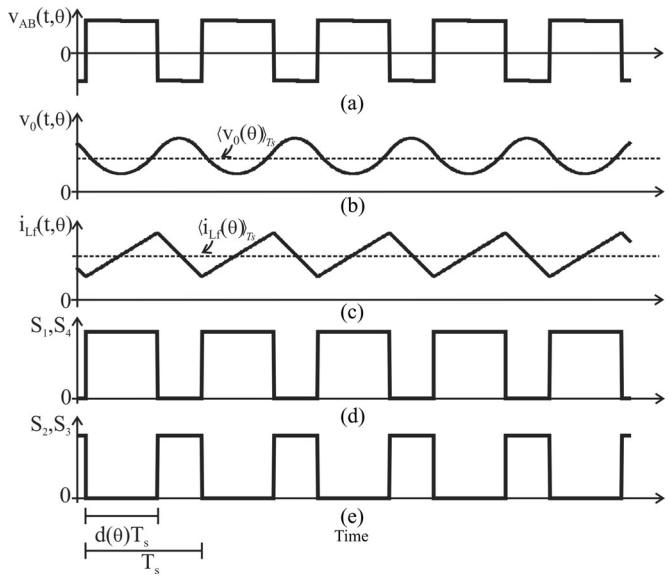


Fig. 6. Simulation waveforms: (a) voltage between terminals A and B; (b) voltage across capacitor C_f; (c) current through inductor L_f; (d) command signal applied to switches S_1 and S_4; (e) command signal applied to switches S_2 and S_3.

III. Theoretical Analysis

The functions involved in each operation stage and their respective equations are obtained for a fixed duty cycle considering one switching period and steady-state analysis, since transitory conditions and/or load variations were not considered.

Table I shows the parameters and the mathematical functions for each variable of interest considering all operational stages and a duty cycle d(θ) higher than 0.5. These functions are sufficient to evaluate the instantaneous average values for the capacitor voltages and inductor currents.

A. Average Voltage in Capacitor C_1

Equation (1) presents the inductor voltage across L_1 for both operational stages. The expressions are indicated by the

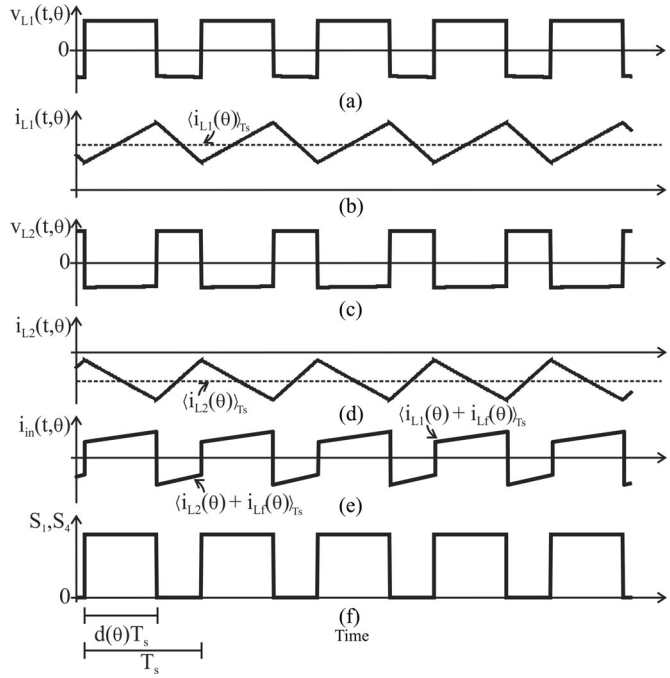


Fig. 7. Simulation waveforms: (a) voltage across inductor L_1; (b) current through inductor L_1; (c) voltage across inductor L_2; (d) current through inductor L_2; (e) input current; (f) command signal applied to switches S_1 and S_4.

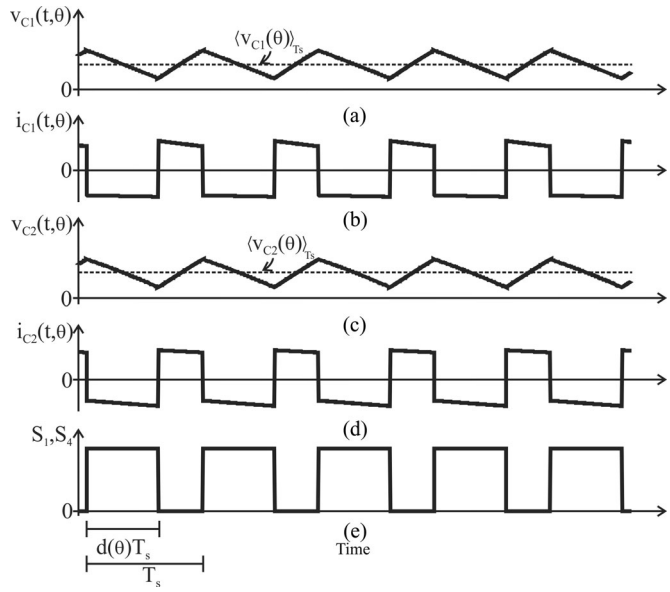


Fig. 8. Simulation waveforms: (a) voltage across the capacitor C_1; (b) current through capacitor C_1; (c) voltage across the capacitor C_2; (d) current through capacitor C_2; (e) command signals applied to switches S_1 and S_4.

superscript numbers

$$\langle v_{L1}(t,\theta)\rangle_{T_S} = \frac{1}{\mathrm{T_s}} \cdot \left\{ v_{L1}^{(1)}(t,\theta) \cdot [d(\theta) \cdot T_S] + v_{L1}^{(2)}(t,\theta) \cdot [1-d(\theta)] \cdot T_s \right\}. \quad (1)$$

Substituting the functions of $v_{L1}(t,\theta)$ shown in Table I into (1), it is possible to write (2), which represents the average voltage applied to the capacitor C_1

$$\langle v_{C1}(\theta)\rangle_{Ts} = V_i \cdot \left[\frac{d(\theta)}{1-d(\theta)}\right]. \quad (2)$$

The duty cycle is given by (3), where M represents the modulation index

$$d(\theta) = \frac{1}{2}\left[1 + M\sin(\theta)\right]. \quad (3)$$

TABLE I
PARAMETERS AND INDICATIVE FUNCTIONS FOR THE STAGE OF OPERATION

Parameters	Stage 1	Stage 2
Time interval	$d(\theta)\cdot T_S$	$[1-d(\theta)]T_s$
Inductor (L_1) voltage	V_i	$-\langle v_{C1}(\theta)\rangle_{Ts}$
Inductor (L_2) voltage	$-\langle v_{C2}(\theta)\rangle_{Ts}$	V_i
Capacitor (C_1) current	$-\langle i_0(\theta)\rangle_{Ts}$	$\langle i_{L1}(\theta)\rangle_{Ts}$
Capacitor (C_2) current	$-\langle i_{L2}(\theta)\rangle_{Ts}$	$\langle i_0(\theta)\rangle_{Ts}$
v_{AB} voltage	$\left[V_i+\langle v_{C1}(\theta)\rangle_{Ts}\right]$	$-\left[V_i+\langle v_{C2}(\theta)\rangle_{Ts}\right]$

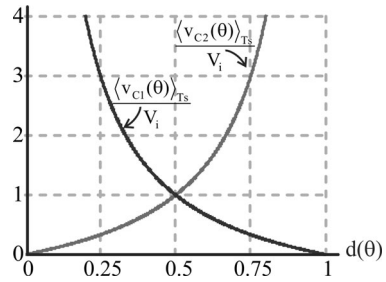


Fig. 9. Average capacitor voltage normalized with respect to the input voltage.

B. Average Voltage Across Capacitor C_2

In (4) the voltage across inductor L_2, for the related operational stages, is represented

$$\langle v_{L2}(t,\theta)\rangle_{T_S} = \frac{1}{T_s} \cdot \left\{ v_{L2}^{(1)}(t,\theta) \cdot [d(\theta) \cdot T_S] + v_{L2}^{(2)}(t,\theta) \cdot [1-d(\theta)] \cdot T_s \right\}. \quad (4)$$

Substituting the functions related to the voltage across inductor L_2, detailed in Table I, in (4), it is possible to find (5), which represents the average voltage across capacitor C_2

$$\langle v_{C2}(\theta)\rangle_{Ts} = V_i \cdot \left[\frac{1-d(\theta)}{d(\theta)}\right]. \quad (5)$$

Fig. 9 shows the average voltage across capacitors C_1 and C_2 normalized with respect to the input voltage.

C. Average Current Through Inductor L_1

Based on the instantaneous average values, the current $i_{C1}(t,\theta)$ is presented as follows:

$$\langle i_{C1}(t,\theta)\rangle_{T_s} = \frac{1}{T_s} \cdot \left\{ i_{C1}^{(1)}(t,\theta) \cdot [d(\theta) \cdot T_s] + i_{C1}^{(2)}(t,\theta) \cdot [1-d\theta)] \cdot T_s \right\}. \quad (6)$$

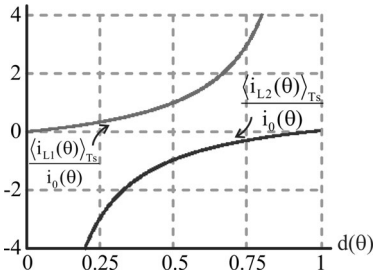


Fig. 10. Average currents through inductors L_1 and L_2 normalized with respect to the average output current.

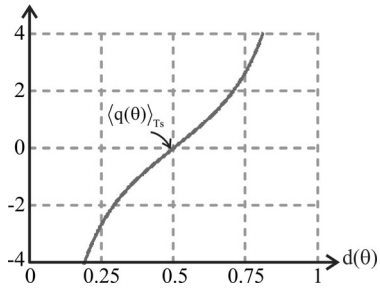


Fig. 11. Static gain in function of the duty cycle.

On applying the operational stage functions, given in Table I, it is possible to obtain (7), which represents the average current through inductor L_1

$$\langle i_{L1}(\theta)\rangle_{Ts} = \langle i_0(\theta)\rangle_{Ts} \cdot \left(\frac{d(\theta)}{1-d(\theta)}\right). \tag{7}$$

D. Average Current Through Inductor L_2

A similar procedure applied to obtain the average current through L_1 is performed for L_2. In (8) the current $i_{C2}(t,\theta)$ is shown, considering one switching period. Substituting the functions presented in Table I in (8), (9) is obtained. This expression represents the average current through inductor L_2

$$\langle i_{C2}(t,\theta)\rangle_{T_s} = 0 = \frac{1}{T_s}\cdot\left\{i_{C2}^{(1)}(t,\theta)\cdot[d(\theta)\cdot T_s] + i_{C2}^{(2)}(t,\theta)\cdot[1-d(\theta)]\cdot T_s\right\} \tag{8}$$

$$\langle i_{L2}(\theta)\rangle_{Ts} = -\langle i_0(\theta)\rangle_{Ts}\cdot\left(\frac{1-d(\theta)}{d(\theta)}\right). \tag{9}$$

Fig. 10 shows the average currents through inductors L_1 and L_2 normalized with respect to the average output current.

E. Static Gain, Current Ripple and Voltage Ripple

The static gain is determined by the relation between the average voltage $\langle v_{AB}(\theta)\rangle_{Ts}$ and the input voltage V_i. In (10), the equation for $v_{AB}(t,\theta)$ is given for one switching period

$$\langle v_{AB}(t,\theta)\rangle_{T_S} = \frac{1}{T_s}\cdot\left\{v_{AB}^{(1)}(t,\theta)\cdot[d(\theta)\cdot T_s] + v_{AB}^{(2)}(t,\theta)\cdot[1-d(\theta)]\cdot T_s\right\}. \tag{10}$$

The functions that represent $v_{AB}(t,\theta)$ in the related operational stages are indicated in Table I. On substituting these functions into (10), we obtain (11), which represents the static gain of the converter herein. In Fig. 11, the curve for the static gain in function of the duty cycle is shown

$$\frac{\langle v_{AB}(\theta)\rangle_{Ts}}{V_i} = \langle q(\theta)\rangle_{Ts} = \left[\frac{(2\cdot d(\theta)-1)}{d(\theta)\cdot(1-d(\theta))}\right]. \tag{11}$$

The ripple currents and voltages are presented in Table II.

TABLE II
RIPPLE CURRENTS THROUGH THE INDUCTORS AND RIPPLE VOLTAGES ACROSS THE CAPACITORS

Parameter	Current/Voltage Ripple
Ripple Current through Inductor L_1	$\Delta i_{L1}(\theta) = \frac{V_i}{L_1\cdot f_s}\cdot d(\theta)$
Ripple Current through Inductor L_2	$\Delta i_{L2}(\theta) = \frac{V_i}{L_2\cdot f_s}\cdot(1-d(\theta))$
Ripple Voltage across Capacitor C_1	$\Delta v_{C1}(\theta) = \frac{i_0(\theta)}{C_1\cdot f_s}\cdot d(\theta)$
Ripple Voltage across Capacitor C_2	$\Delta v_{C2}(\theta) = \frac{i_0(\theta)}{C_2\cdot f_s}\cdot(1-d(\theta))$
Ripple Current through Inductor L_f	$\Delta i_{Lf} = \frac{V_i}{L_f\cdot f_s}$
Ripple Voltage through Capacitor C_f	$\Delta v_{Cf} = \frac{1}{8}\cdot\frac{V_i}{L_f\cdot C_f\cdot f_s^2}$

F. Considerations Regarding the New Converter Operation

Due to the nonlinear characteristic inherent to the static gain of the new inverter, it can be concluded that as the duty cycle increases the static gain increases substantially, as highlighted in the static gain curve presented in Fig. 11. Thus, the application of an increase in the cyclic ratio imposes a large increase in the gain, leading to a distortion in the output voltage of the converter.

As a solution for this particularity, the desired voltage gain is used as the reference signal, which is applied at the input of the mathematical block, denominated by $F(\theta)$. The signal obtained at this function output is the operating duty cycle, and it enables the linearization of the relation between the desired static gain and that obtained at the converter output.

The following equations show the steps applied to obtain the mathematical block that allows the representation of a sinusoidal output voltage with low distortion, independently of the desired voltage gain. The static gain of the new inverter topology is defined as follows:

$$d(\theta) = \frac{(\langle q(\theta)\rangle_{Ts}-2)}{2\cdot\langle q(\theta)\rangle_{Ts}} \pm \frac{\sqrt{\left(4+\langle q(\theta)\rangle_{Ts}^2\right)}}{2\cdot\langle q(\theta)\rangle_{Ts}}. \tag{12}$$

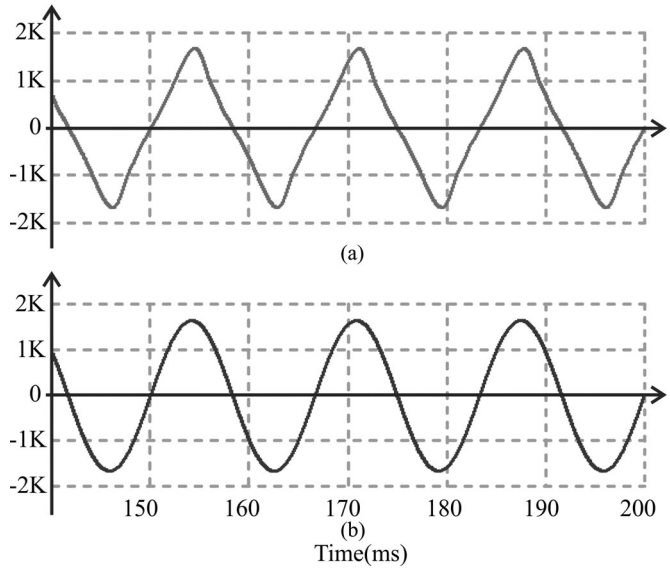


Fig. 12. Simulation results: (a) output voltage without the linearization function; (b) output voltage with linearization function.

Manipulating (12) the duty cycle, as a function of the static gain, is presented as follows:

$$F(\theta) = \frac{(\langle q(\theta)\rangle_{Ts} - 2)}{2 \cdot \langle q(\theta)\rangle_{Ts}} + \frac{\sqrt{\left(4 + \langle q(\theta)\rangle_{Ts}^2\right)}}{2 \cdot \langle q(\theta)\rangle_{Ts}}. \quad (13)$$

In order to demonstrate the efficacy of the linearization function, the simulation results for the converter output voltage without and with $F(\theta)$ are presented in Fig. 12, for a static gain of four. It was verified that the use of the linearization function is sufficient to establish a linear relation between the real and the reference static gain, as shown in Fig. 12.

IV. Transfer Function and Control

The converter transfer function is found employing the average small signals linearization, through which the relationship between the output voltage and duty cycle is obtained, according to (14), where the numerator and denominator coefficients are presented in (15) and (16), respectively

$$\frac{\hat{v}_0(s,\theta)}{\hat{\mathrm{d}}(s,\theta)} = \frac{n_{\mathrm{planta}}(s,\theta)}{\mathrm{d}_{\mathrm{planta}}(s,\theta)} \quad (14)$$

$$n_{\mathrm{planta}}(s,\theta) = b_4(\theta)\cdot s^4 + b_3(\theta)\cdot s^3 + b_2(\theta)\cdot s^2 + b_1(\theta)\cdot s + b_0(\theta) \quad (15)$$

$$d_{\mathrm{planta}}(s,\theta) = a_6(\theta)\cdot s^6 + a_5(\theta)\cdot s^5 + a_4(\theta)\cdot s^4 + a_3(\theta)\cdot s^3 + a_2(\theta)\cdot s^2 + a_1(\theta)\cdot s + a_0(\theta). \quad (16)$$

In order to simplify the analysis, (17) and (18), shown at the bottom of the next page, summarize the numerator and denominator coefficients discarding the parasite resistances of inductors and capacitors. In the mathematical analysis, the inductances L_1 and L_2 are defined by L_C, while capacitances C_1 and C_2 are given by C_C

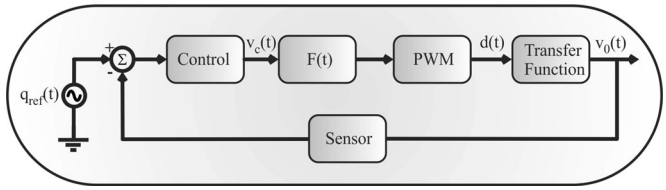


Fig. 13. Block diagram of converter.

Only the output voltage control is achieved by the use of a simple controller. The compensator transfer function is described by (19), where K_C and w_p are the compensator gain and pole frequency, respectively

$$C(s) = \frac{K_C}{s\cdot(s + w_p)}. \quad (19)$$

V. Experimental Results

In order to validate the theoretical analysis, a prototype was implemented with the following features: output rated power of 1 kW, dc input voltage of 96 $\mathrm{V_{dc}}$, output voltage of 110 $\mathrm{V_{rms}}$, fundamental output frequency of 60 Hz and switching frequency of 20 kHz. The maximum gain from input voltage to output voltage is 1.61.

In the power stage, four IGBTs model SK45GB063 from Semikron were used. The inductance and capacitance values implemented were L_1=L_2 = 255 μH, C_1=C_2 = 1 μF, L_f = 1.5 mH, C_f = 5 μF, and R_0 = 12 Ω.

Inductors L_1 and L_2 were constructed with cores model NEE-65/33/26 employing the material IP12R from Thornton, with 56 turns and 11 AWG 21 conductors associated in parallel. The output inductor was designed with one core model NEE 76/50/76 from Thornton using 45 turns and 23 AWG 23 conductors associated in parallel.

In order to obtain the switching cell capacitance, a combination of series and parallel capacitors was implemented, resulting is six capacitors of 680 nF model B32656 S from Epcos. The output capacitance was obtained by the association of 5 capacitors of 1000 nF model B32653 from Epcos in parallel. For the generation of switching signals, a pulsewidth modulation (PWM) was implemented in a PIC model 18F2331 from Microchip. Two drivers model SKHI 20opA from Semikron were employed for the IGBTs command.

In the compensator designing criteria the parameters shown in (19), gain and pole frequency, were adjusted to 1005 and 1960 rad/s, respectively. The block diagram for the proposed control strategy is presented in Fig. 13.

Fig. 14 shows the module, phase and roots locus of converter for the compensated system.

Fig. 15 shows the main waveforms obtained experimentally. The experimental waveforms presented in Fig. 15 are in agreement with the expected results. In Fig. 15(a), the output and input voltage are shown for the converter operating as step-up converter. Fig. 15(d) shows the converter response with closed-loop voltage control, when submitted to a load step change from 0% to 100%.

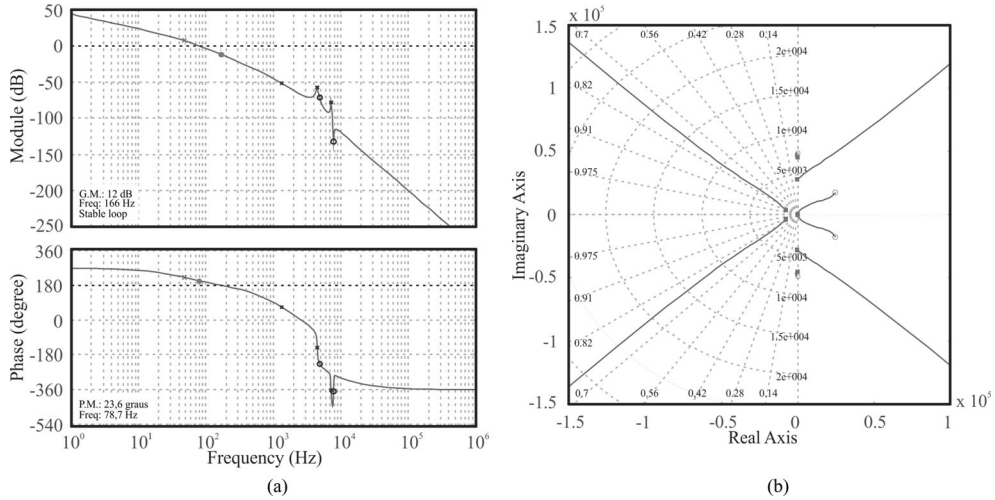


Fig. 14. (a) Module and phase; (b) roots locus.

Fig. 16 shows the experimental results for a closed-loop with *RL* load and nonlinear load. The *RL* load was designed for an output of 1 kVA using a resistance of 12 Ω and an inductance of 9mH. For the nonlinear load, a 24 Ω resistor, 25 mH inductor, and 3 mF capacitor were employed. The load and capacitor were implemented in parallel to rectifier bridge. The experimental processed power was established as 470 W.

$$\begin{cases} b_0(\theta) = -\dfrac{d(\theta)\cdot R_0\cdot V_i\cdot\left(2\cdot d^2(\theta)-2\cdot d(\theta)+1\right)}{(d(\theta)-1)} \\ b_1(\theta) = -\dfrac{i_0(\theta)\cdot L_C\cdot R_0\left(4\cdot d^3(\theta)-6\cdot d^2(\theta)+4\cdot d(\theta)-1\right)}{(d(\theta)-1)^2} \\ b_2(\theta) = \dfrac{R_0\cdot V_i\cdot C_C\cdot L_C\cdot\left(d^2(\theta)-d(\theta)+1\right)}{(d(\theta)-1)^2} \\ b_3(\theta) = -\dfrac{i_0(\theta)\cdot R_0\cdot C_C\cdot L_C^2\cdot(2\cdot d(\theta)-1)}{(d(\theta)-1)^2} \\ b_4(\theta) = \dfrac{V_i\cdot R_0\cdot(L_C\cdot C_C)^2}{\left(\mathrm{d}^2(\theta)-2\cdot d(\theta)+1\right)} \end{cases} \tag{17}$$

$$\begin{cases} a_0(\theta) = -d(\theta)^3\cdot R_0\cdot(d(\theta)-1) \\ a_1(\theta) = d(\theta)^2\cdot(2\cdot L_C+L_f)-L_C-d(\theta)^4\cdot(2\cdot L_C+L_f)-\dfrac{L_C}{(d(\theta)-1)}-4\cdot d(\theta)^2\cdot L_C \\ a_2(\theta) = d(\theta)^3\cdot(2\cdot L_C\cdot R_0\cdot C_f+L_f\cdot C_f\cdot R_0)-d(\theta)^2\cdot(2\cdot C_C\cdot L_C\cdot R_0+4\cdot C_f\cdot R_0\cdot L_C)-\cdots \\ -\cdots\dfrac{C_C\cdot L_C\cdot R_0+C_f\cdot L_C\cdot R_0}{\mathrm{d}(\theta)-1}-d(\theta)^4\cdot(2\cdot L_C\cdot R_0\cdot C_f+L_f\cdot C_f\cdot R_0)-R_0\cdot L_C\cdot C_C-R_0\cdot L_C\cdot C_f \\ a_3(\theta) = -\dfrac{d(\theta)\cdot L_C\cdot C_C\,(L_C+L_f)\cdot\left(2\cdot d(\theta)^2-2\cdot d(\theta)+1\right)}{D(\theta)-1} \\ a_4(\theta) = -\dfrac{d(\theta)\cdot R_0\cdot L_C\cdot C_C\cdot\begin{pmatrix} L_C\cdot C_C+L_C\cdot C_f+L_f\cdot C_f+\cdots \\ \cdots 2\cdot d(\theta)^2\cdot L_C\cdot C_f+2\cdot d(\theta)^2\cdot L_f\cdot C_f-\cdots \\ \ldots-2\cdot d(\theta)^2\cdot L_C\cdot C_f-2\cdot d(\theta)^2\cdot L_f\cdot C_f \end{pmatrix}}{d(\theta)-1} \\ a_5(\theta) = -\dfrac{d(\theta)\cdot L_f\cdot(L_C\cdot C_C)^2}{(d(\theta)-1)} \\ a_6(\theta) = -\dfrac{d(\theta)\cdot R_0\cdot L_f\cdot C_f\cdot(L_C\cdot C_C)^2}{(d(\theta)-1)} \end{cases} \tag{18}$$

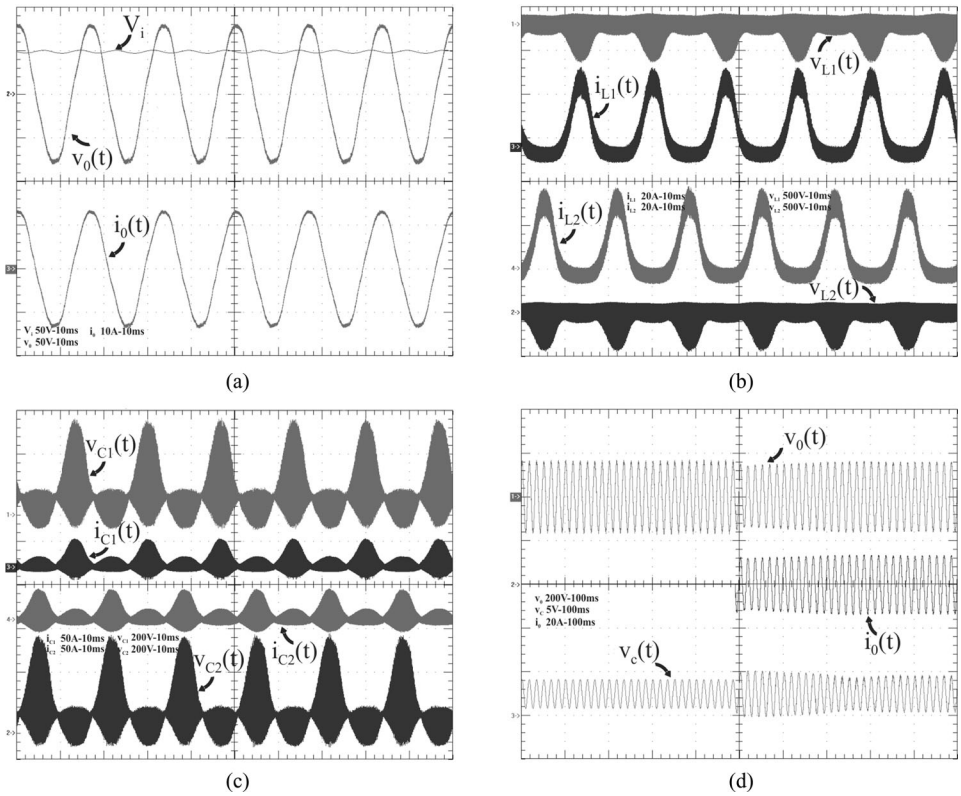


Fig. 15. Experimental waveforms: (a) input voltage V_i (50 V/div), output voltage $v_0(t)$ (50 V/div–10 ms/div) and output current $i_0(t)$ (10 A/div–10 ms/div); (b) voltage across inductor $L_1 v_{L1}(t)$ (500 V/div–10 ms/div), current across inductor $L_1 i_{L1}(t)$ (20 A/div–10 ms/div), voltage across inductor $L_2 v_{L2}(t)$ (500 V/div–10 ms/div) and current across inductor $L_2 i_{L2}(t)$ (20 A/div–10 ms/div); (c) voltage across capacitor $C_1 v_{C1}(t)$ (500 V/div–10 ms/div), voltage across capacitor $C_1 v_{C2}(t)$ (200 V/div–10 ms/div), current across capacitor $C_1 i_{C1}(t)$ (50 A/div–10 ms/div), current across capacitor $C_2 i_{C2}(t)$ (50 A/div); (f) output voltage (200 V/div), output current (20 A/div) and control signal (5 V/div) considering a load step from 0 to 100%.

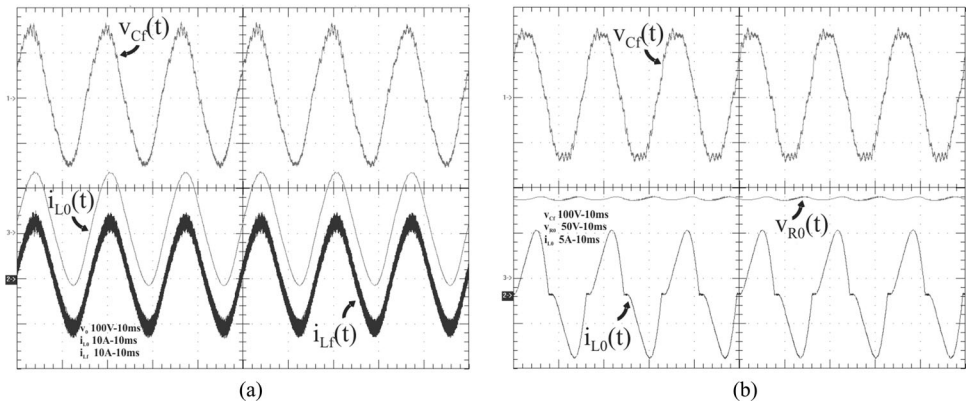


Fig. 16. Experimental waveforms (a) voltage across capacitor $C_f v_0\ (t)$ (100 V/div), current across inductor $L_f\ i_{Lf}\ (t)$ (10 A/div), load *RL* current $i_{L0}(t)$ (10 A/div), (b) voltage across capacitor $C_f v_0(t)$ (100 V/div), nonlinear inductor load current $i_{L0}(t)$ (5 A/div), and load voltage $v_{R0}(t)$ (50 V/div).

The waveforms for the voltage and current across switch S_1, presented in detail during commutation, are shown in Fig. 17. The switches commutation of the new proposed converter is dissipative as highlighted in Fig. 17(c) and (d).

Fig. 18 shows the measured efficiency against the output power for the new proposed dc–ac converter. It can be observed that the maximum efficiency is 89.375%, obtained for a power of 600 W.

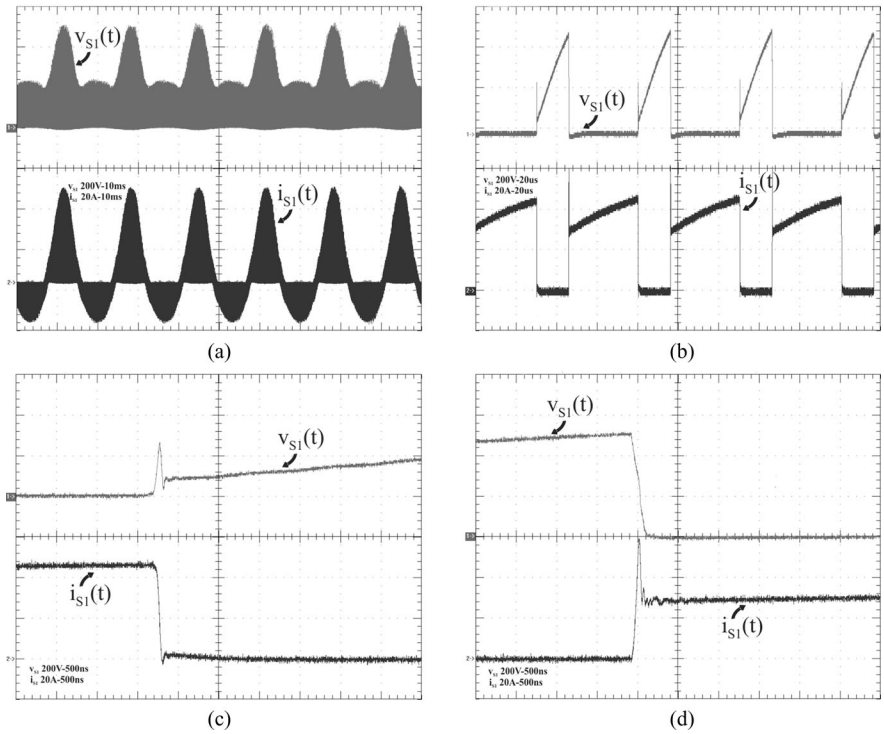


Fig. 17. Experimental waveforms: (a) voltage and current across switch S_1 v_{S1} (200 V/div) and i_{S1} (20 A/div); (b) high frequency detail of voltage and current across switch S_1; (c) switch S_1 turn on in detail; (d) switch S_1 turn off in detail.

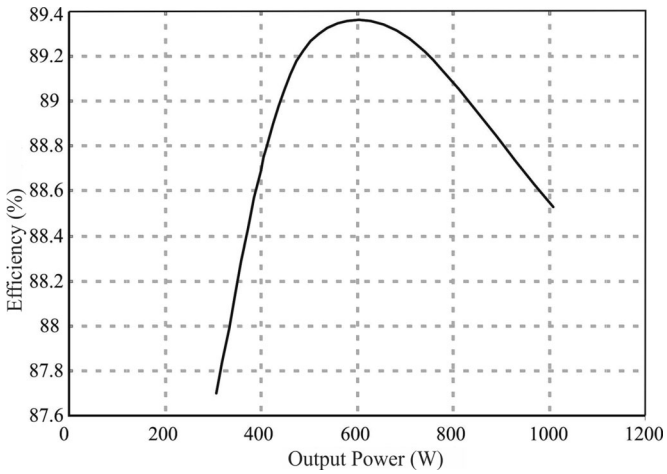


Fig. 18. Measured efficiency against output power for the new proposed dc–ac converter.

VI. Conclusion

This paper presented a new topology for dc–ac converters whose main feature is its capacity to provide an instantaneous output voltage higher or lower than the input voltage without an intermediate power stage or transformer. Based on theoretical analysis and experimental results the following conclusions can be drawn:

1) the experimentally evaluated performance was in agreement with the theoretical analysis;
2) the maximum efficiency (for a power of 600 W) measured in the laboratory was 89%;
3) the effectiveness of the linearization function for the system operating in open loop was verified in the laboratory;
4) the closed-loop converter operation was verified for resistive, resistive-inductive, and nonlinear loads.

References

[1] R. O. Caceres and I. Barbi, "A boost DC–AC converter: analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan. 1999.

[2] N. Vazquez, J. Villegas-Saucillo, C. Hernandez, E. Rodriguez, and J. Arau, "Two-stage uninterruptible power supply with high power factor," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2954–2962, Aug. 2008.

[3] N. Vazquez, J. Almazan, J. Alvarez, C. Aguilar, and J. Arau, "Analysis and experimental study of the buck, boost and buck–boost inverters," in *Proc. 30th Annu. IEEE Power Electron. Spec. Conf.*, 1999, vol. 2, pp. 801–806.

[4] B. S. Prasad, S. Jain, and V. Agarwal, "Universal single-stage grid-connected inverter," *IEEE Trans. Energy. Convers.*, vol. 23, no. 1, pp. 128–137, Mar. 2008.

[5] M. Jang and V. G. Agelidis, "A minimum power-processing-stage fuel-cell energy system based on a boost-inverter with a bidirectional backup battery storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1568–1577, May 2011.

[6] A. M. Salamah, S. J. Finney, and B. W. Williams, "Single-phase voltage source inverter with a bidirectional buck–boost stage for harmonic injection and distributed generation," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 376–387, Feb. 2009.

[7] M. Kaliamoorthy, R. M. Sekar, and I. G. C. Raj, "Solar powered single stage boost inverter with ANN based MPPT algorithm," in *Proc. IEEE Int. Conf. Commun. Control Comput. Technol.* , 2010, pp. 165–170.

[8] H. Patel and V. Agarwal, "MPPT scheme for a PV-fed single-phase single-stage grid-connected inverter operating in CCM with only one current sensor," *IEEE Trans. Energy. Convers.*, vol. 24, no. 1, pp. 256–263, Mar. 2009.

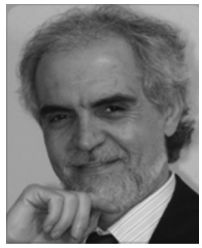
[9] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504, 510, Mar./Apr. 2003.

[10] S. Miaosen and F. Z. Peng, "Operation modes and characteristics of the Z-source inverter with small inductance," in *Proc. 40th IAS Annu. Meeting. Conf. Rec. Ind. Appl. Conf.*, 2005, vol. 2, pp. 1253–1260.

[11] D. Vinnikov, I. Roasto, and T. Jalakas, "An improved high-power DC/DC converter for distributed power generation," in *Proc. 10th Int. Conf. Elect. Power Quality Utilisation (EPQU)*, 2009, pp. 1–6.
[12] K. Beer and B. Piepenbreier, "Properties and advantages of the quasi-Z-source inverter for DC–AC conversion for electric vehicle applications," *Proc. Electr. Power Train Emobility*, pp. 1–6, 2010.
[13] G. Buja, R. Keshri, and R. Menis, "Characteristics of Z-source inverter supply for permanent magnet brushless motors," in *Proc. 35th Annu. Conf. IEEE Ind. Electron. (IECON'09)*, pp. 1234–1239.
[14] A. S. Khlebnikov and S. A. Kharitonov, "Application of the Z-source converter for aircraft power generation systems," in *Proc. 9th Int. Workshop Tuts Electr. Devices Mater. (EDM)*, 2008, pp. 211–215.
[15] A. Florescu, O. Stocklosa, M. Teodorescu, C. Radoi, D. A. Stoichescu, and S. Rosu, "The advantages, limitations and disadvantages of Z-source inverter," in *Proc. 2010 Int. Semicond. Conf. (CAS)*, Oct. 2010, vol. 2, pp. 483, 486.
[16] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.
[17] M. Calais, J. Myrzik, T. Spooner, and V. G. Agelidis, "Inverters for single-phase grid connected photovoltaic systems-an overview," in *Proc. IEEE 33rd Annu. Power Electron. Spec. Conf. (PESC'02)*, pp. 1995–2000.
[18] X. Yaosuo, C. Liuchen, K. Sren Baekhj, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, vol. 19, pp. 1305–1314, 2004.
[19] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems-an overview," in *Proc. IEEE Int. Symp. Ind. Electron. (ISIE'98)*, vol. 1, pp. 224–229.
[20] W. Rong-Jong, W. Wen-Hung, and L. Chung-You, "High-performance stand-alone photovoltaic generation system," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 240–250, 2008.

Gleyson Luiz Piazza was born in São Lourenço do Oeste, Brazil, in 1981. He received the B.Sc. degree in electrical engineering from the Santa Catarina State University (UDESC), Joinvile, Brazil, in 2005, and the M.Sc. and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 2008 and 2013, respectively.

His current research interests include dc–ac power converters, dc–dc power converters, and power factor correction.



Ivo Barbi (M'78–SM'90–F'11) was born in Gaspar, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society and the Power Electronics Institute of the Federal University of Santa Catarina, where he is currently a Professor.