Analysis, design and characteristics of an Ideal Op-Amp & a Practical Op-Amp

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Analysis of an Ideal Op-Amp is carried out using PSpice and Cadence Design Kit. The results are then compared with an actual op-amp uA741 by performing series of simulation tests. A Butterworth filter with Sallen & Key architecture is designed and checked for frequency response.

***Keywords*—operational amplifier, uA741, Butterworth, design methodology**

A. INTRODUCTION

Operational Amplifiers oscillators are widely used in the electronic circuits.First Op-Amps were developedin early 20th century with first models being made by Vacuum tubes used for differentiating and integrating mathematical equations. Later they were technologically improved by solid state Op-amps to now, a more known, IC based Op-amps.[1] The purpose of this document is to Analyze the characteristics of an Ideal Op-amp; compare it with an actual Op-Amp (ua741) and to use this Op-Amp to design a second order Butterworth filter with Cur-off frequency of 1.5kHz. the software used in this analysis is primarily PSpice with basic component library. Supporting software used for validating the results were Cadence Custom IC Design Kit for model amplifier and Butterworth response; and LT Spice IV.

B. OPERATIONAL AMPLIFIERS

An Operational Amplifier, or an Op-Amp, is a high gain differential amplifier with very high Input impedance and a low output impendence. From a schematic point of view we can describe an Op-Amp as shown in figure 1:

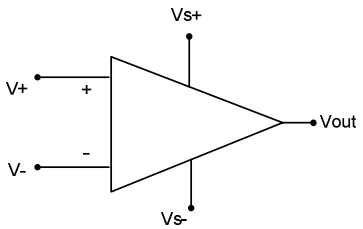


Fig.1: Schematic representation of an Op-Amp

There are different ways of classifying an Op-Amp such as a single-ended operation, where an input signal is applied to either input with the other input terminal connected to the ground, or a double ended operation, where two opposite polarity input signals are applied to each input terminal, or a common-mode operation when the same input is appled to both the input terminals. [2]

Construction wise a simple op-amp consists of 3 stages:

1. A Differential Input Stage
2. A common source amplifier stage
3. An Output Buffer Stage

Each Stage has a specific role in the Op-Amp

A Differential Stage takes in input in the form of a Differential Voltage, V+ w.r.t V-. The Open loop Gain of a Differential Stage is very high and therefore it supplies nearly constant current in the output.

A Common source amplifier with frequency Compensation stage because of its low-pass characteristics acts as an Integrator. Therefore, a constant current input from the First Stage results in linearly increasing output.

The output buffer ensures that the Op-Amp is not being loaded to the output circuitry. In construction it is merely a voltage follower and isolates the Op-Amp circuitry from the output.

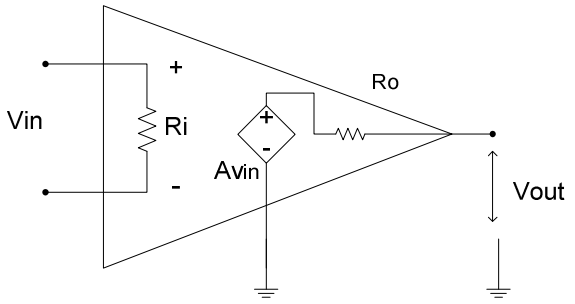


Fig.2: An Op-amp with parameters

Ideally, an Operational Amplifier has the following characteristics [3] :

1. Input Resistance, $R_i = \infty$
2. Output Resistance, R_o = o Ω
3. Voltage Gain ,$A_v = -\infty$, independent of ω
4. Bandwidth = ∞
5. V_o= 0V , when $V_{in-} = V_{in+}$
6. Since $R_i = \infty$ Ω, i- = i+ = 0A

C. SIMULATION FOR IDEAL INVERTING AMPLIFIER

1. Simulation for Inverting Amplifier

We first examine the simulation results for an Ideal Inverting Op-Amp. The values chosen for this simulation are:

V_{source} (shown as V3 in figure 3) = 1 V.
f = 1 kHz
V_{ref+} = +15V
V_{ref-} = -15V
Values of R1 and R5 are chosen such that it satisfies the closed loop gain, A_v =10 given by the equation

$$A_v = -\frac{Z_2}{Z_1}$$

equation (1)

Here we assume the Z_1 (as R1 in the schematic)as 1Ω , therefore Z_2(as R5 in the schematic)= 10 Ω

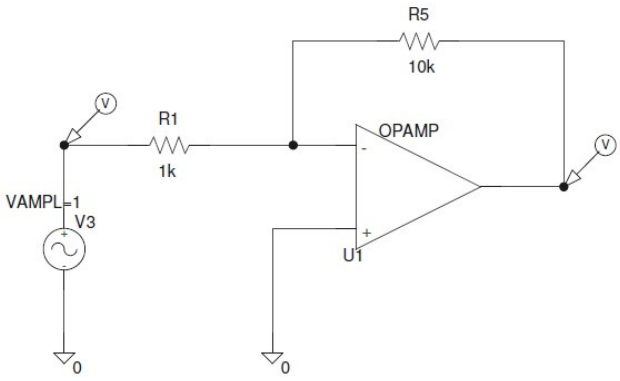


Fig. 3: Simulating the Ideal Op-amp with predetermined parameters

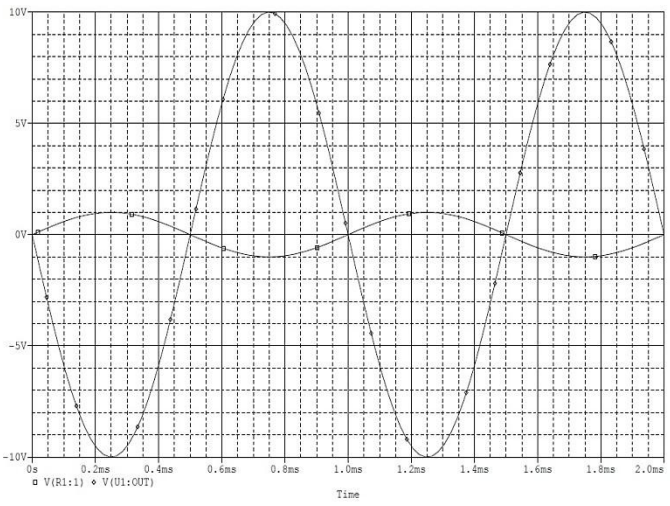


Fig. 4: Transient Analysis of the Op-amp circuit

Figure 4 displays the transient analysis of the Op-Amp w.r.t Input and Output voltages. From the Eqn.(1), we can clearly see that for an Input sinusoidal voltage source of 1 V we attain an inverted Output sinusoidal voltage of 10V

2. Simulation by parametric sweep analysis of an Inverting Amplifier

To see the affect of various values of Z_2 on the output of the Op-Amp we perform a parametric sweep of Z_2 by varying the value of R2 from

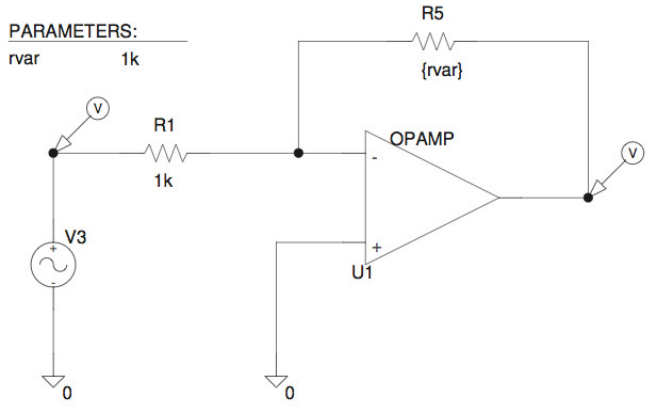


Fig.5: Simulating the Ideal Op-amp with parametric sweep of R2

Figure 5 shows the modified schematic from figure 3 in which we replace the Z_2 with a variable resistor with values ranging from 1kΩ to 10k Ω in steps of 1Ω. This should give us a waveform of the transient output with 10 waves corresponding to each Z_2 (shown as R5 in the schematic) value.

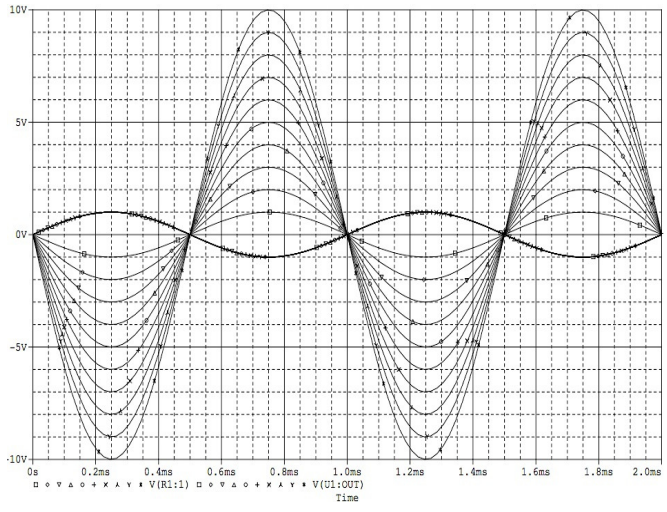


Fig.6: Transient Analysis of Ideal Op-amp with parametric sweep of R5

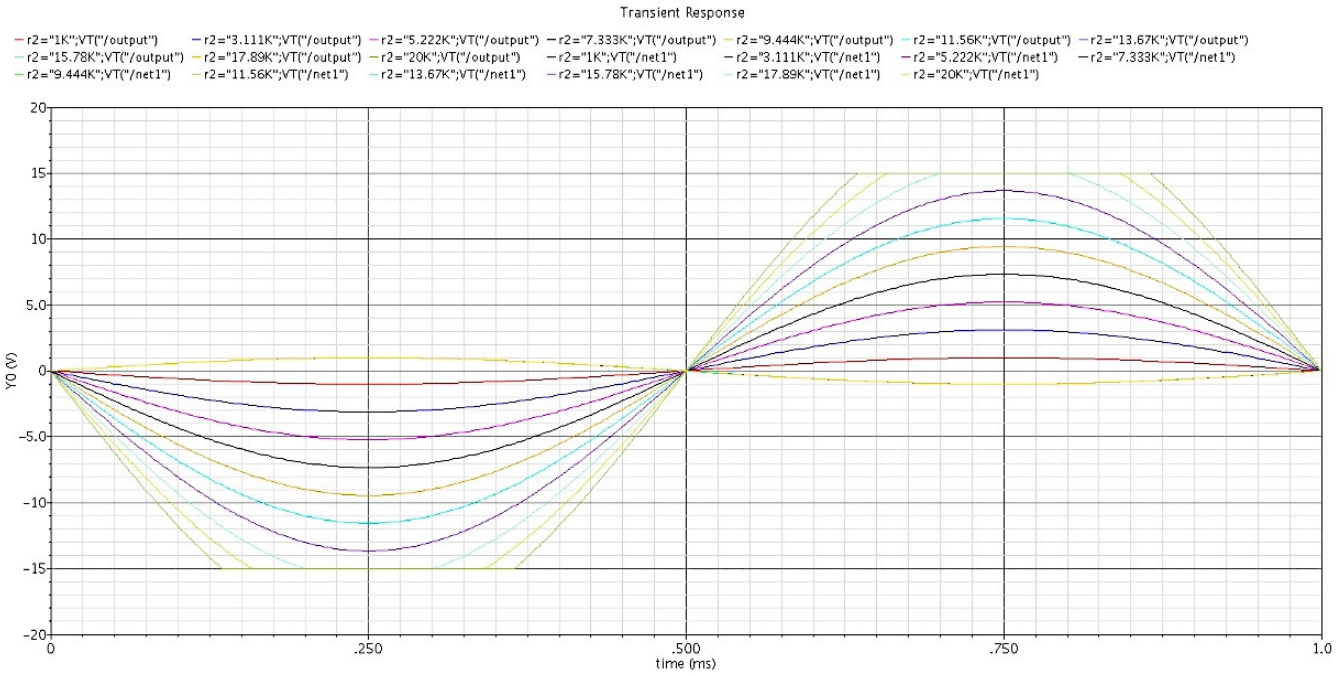


Fig.7: Transient Analysis of an Ideal Op-amp with parametric sweep of Z_2 from 1kΩ to 20kΩ in 10 incremental steps

Figure 6 displays the input voltage (bold line) vs multiple output voltages corresponding to R5= 1 Ω to R5 = 10Ω. It can be observed that the output gain is varying as per equation (1) . Now to take a step further, we will simulate the Op-amp circuit with a parametric sweep such that the value of $A_v > 10$, i.e., $Z_2 > 10$ and observe its effect on the output of the Op-Amp.

Figure 7 shows the effect of varying Z_2 beyond 10Ω. The graph is obtained with colour legends in Cadence AMS Hit Kit to show the affect of varying Z_2 (in graph shown as r2) on the output voltage. As per our setting for the Op-amp, we maintained the V_{ref} at +/- 15V. Therefore when the amplifier is subjected to driving the output the maximum output voltage it can deliver is V_{ref} after which it goes into saturation.

This issue can be corrected in two ways:

1. Increase the V_{ref} levels to allow an operation beyond the existing 15V:
   This means we are subjecting the internal CMOS devices to Source and Sink higher level of Voltages (and currents). Theoretically it is possible to increase the V_{ref} to a value till 100V and assume the output will vary +/- 100 accordingly. But practically, the type of Op-Amp selected for a design provides the maximum possible amplification that can be reached.

2. Reduce the value of Z_2:
   By reducing Z_2 , implying reducing the closed loop gain, A_v, such that the output value does not cross the saturation voltage of 15 V. In this particular case, it means that the value of $Z_2 < 15\Omega$., if $Z_1 = 1\Omega$.

B. SIMULATION FOR UA741 AMPLIFIER

1. Simulation for Inverting Amplifier

A simulation similar to an Ideal Op-Amp will be carried out with a test circuit. In this case, the ideal op-Amp is replaced with uA741 Op-Amp, as shown in figure 8

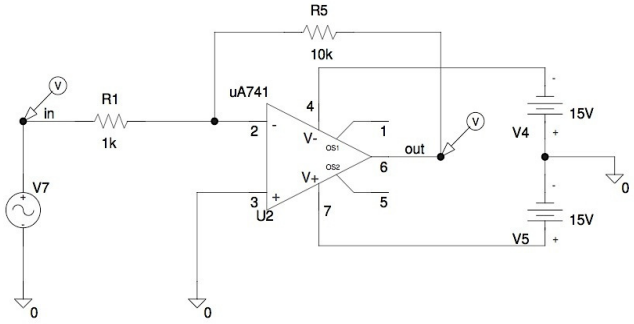


Fig.8: Analysis of uA741 Op-amp

The values for simulation are:
V_{source}(shown as V7 in figure 8) = 1 V.
f = 1 kHz
V+= +15V
V− = -15V
$Z_1 = R1 = 1k\Omega$
$Z_2 = R5 = 10k\Omega$

2. Simulation by parametric sweep analysis of an Inverting uA741 Amplifier

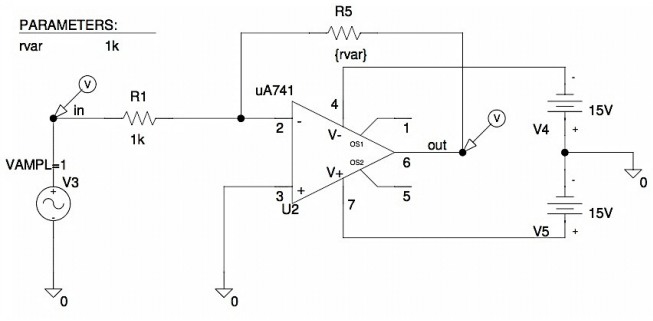


Fig.9: Analysis of uA741 Op-amp by parametric analysis

Figure 9 shows the modified schematic from figure 8 in which we replace the Z_2 with a variable resistor variable, rvar, withvalues ranging from 1kΩ to 10kΩ in steps of 1Ω by parametric sweep . Similar to the Ideal Op-Amp, this should give us a waveform of the transient output with 10 waves corresponding to each Z_2 (shown as R5 in the schematic) value.

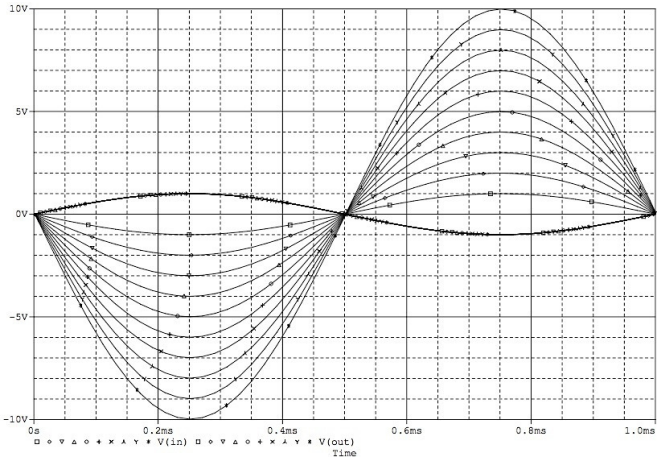


Fig.10: Transient Analysis of uA741 Op-amp with parametric sweep of Z_2 from 1kΩ to 20kΩ in 10 incremental steps

From the figure 10 we observe the behavior of an ideal Op-amp with parametric analysis of Z_2 from 1kΩ to 10kΩ , there by increasing the gain from 1 to 10. Since the gain is adjusted so that the output remains well within the saturation level we get waveforms without clipping at maxima or minima values.

3. Measurement of Input Current into uA741 Op-Amp

Current is measured into the Op-Amp by using Kirchhoff's Current Law (KCL), which states that current at a junction is zero.

In our simulation, we assume the junction under test is the negative input pin of the Op-Amp.

Figure 11 shows the test circuit, junction *vi-* is the input terminal to the Op-Amp.

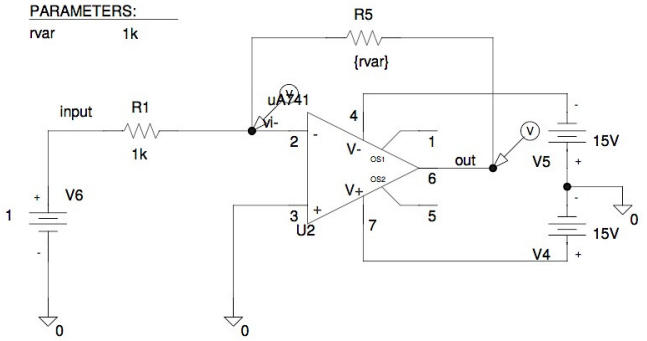


Fig.11: Analysis of uA741 Op-amp for input current

First we simulate the circuit with different values of R2, thereby changing the gain of the closed loop system as per Eqn.(1).

By using the standard KCL definition,

$$\frac{Vinput - Vin}{R1} = \frac{Voutput - Vin}{R2} \text{equation(2) [4]}$$

We calculate the individual currents in R1 and R2 resistor arms, each corresponding to a different R2 value according to the parametric sweep.

Table1: Current in the R1 arm for different values of R2, i.e., Gain .All voltages are in Volts (V)

Gain	Vinput	Vin-	i1 (A)
1	1	2.503E-05	9.999749680000E-04
3	1	3.507E-05	9.999649320000E-04
5	1	4.511E-05	9.999548950000E-04
7	1	5.514E-05	9.999448590000E-04
9	1	6.518E-04	9.993482300000E-04

Table2: Current in the R2 arm & difference between i1 and i2. All voltages are in volts (V)

Gain	Voutput	i2 (A)	i1-i2 (A)
1	-0.9999	9.999250320000E-05	-8.999824648000E-04
3	-2.9996	2.999635068000E-04	-7.000014252000E-04
5	-4.9993	4.999345105000E-04	-5.000203845000E-04
7	-6.99	6.990055141000E-04	-3.009393449000E-04
9	-8.9986	8.999251770000E-04	-9.942305300000E-05

As per table 2, column of *i1-i2* gives the currents going through the Op-amps, i.e., the input current into the Op-Amp.

4. Measurement of Op-Amp parameters

i) Input & Output Offset Voltage

The Input offset voltage is that voltage which must be applied to the input terminals to balance the amplifier, i.e., the output voltage of the Op-Amp becomes zero.

Since we are using an open loop amplifier, i.e., a very high

gain system, we first ensure that the input voltage is sufficiently low so that the output is not driven to saturation. Therefore we try to achieve at a minimum level of input voltage which will give us non-saturated output by using a potentiometer.

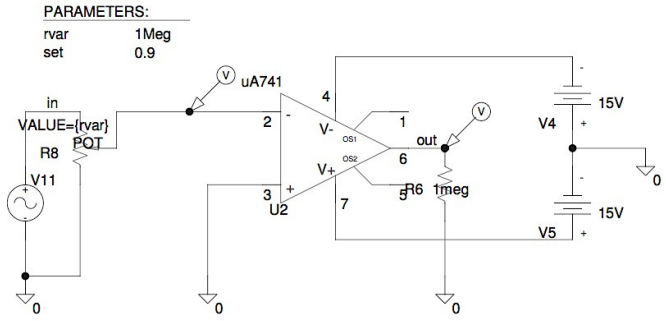


Fig.12: Analysis of input offset voltage of uA741 Op-amp by detecting minimum input voltage using a potentiometer.

By varying the potentiometer arm, called as *set* in the parametric sweep variable (figure 12), we are able to sweep across the input voltage reaching the Op-Amp. We could also use a DC sweep of input Vdc source instead of using a potentiometer.

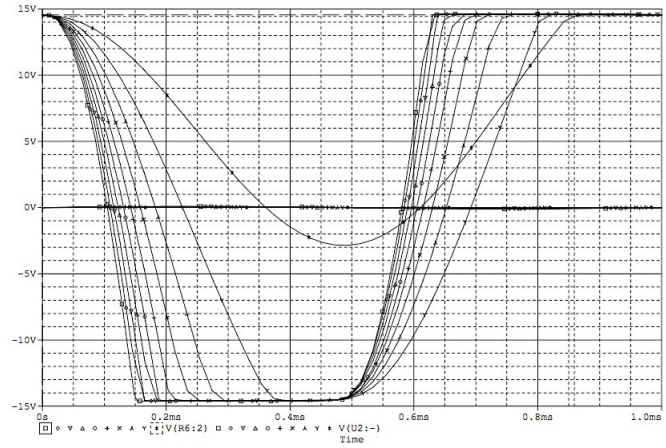


Fig.13: Output waveform by varying the potentiometer arm at input and looking for the non-saturated curve at output.

By observing the output, we can see the value approximate vale of the input where the output begins to come under saturation, which is at $V_{input} < 100\ \mu V$.

By sweeping the input voltage from 10µV to 100µV we observe the input vs output voltage characteristics.

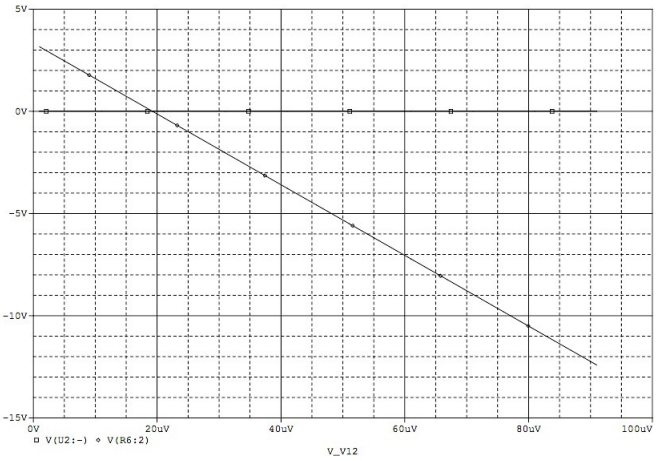


Fig.14: Input vs Output voltage characteristics

From the figure 14, we can see the output voltage crosses 0V at Input voltage = 19.241µV.

Therefore, Input Offset Voltage = 19.241µV.

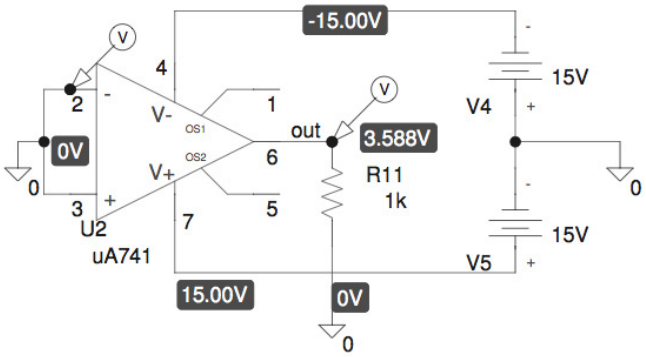


Fig.15: Analysis of output offset voltage of uA741

The output-offset voltage of an Op-Amp is the DC voltage present at the output of the amplifier w.r.t ground when the puts are grounded.

Figure 15 gives us the information of Output offset voltage of 3.588V , for uA741 Op-Amp.

ii) Open Loop Voltage Gain

To calculate the Open loop gain we look at values at

Input voltage >19.241µV

so that the offset voltage is negated , & corresponding

Output voltage < 15 V,

avoiding output saturation voltage. Practically the output voltage will not go beyond 15 V for it to be measured.

The Gain is therefore given by

Gain = Output/(Input-offset voltage)

i.e., |Gain| = 5.3469/(50.159µ-19.241µ)

$$\text{Open Loop Gain} \approx 1.7 \times 10^5$$

iii) Input &Output Resistance R_i & R_o

The output resistance of an operational amplifier can be

obtained from the values of Open Loop Gains at $R_L = \infty$ and $R_L \neq \infty$ as,

$$A_V = \frac{R_L}{R_L + R_O} A_v$$

Where, A_V is the Open- loop gain with $R_L = \infty$, and Av is the Open-Loop gain with $R_L \neq \infty$.

In PSpice the Input and output resistance is calculated by the Transfer Function operator in PSpice simulation. For a given open loop system (for example in figure 9) with a given input voltage and a resulting output voltage, we can easily simulate the transfer function which gives the resistances values.

Transfer_function.txt

INPUT RESISTANCE AT V_V13 = 9.963E+05

OUTPUT RESISTANCE AT V(out) = 1.410E+02

Therefore,

Input resistance, $R_i \approx 9.96 \times 10^5 \Omega$

Output resistance, $R_o \approx 140\ \Omega$

5. Frequency Response the Op-Amp

The corner frequency is said to be that frequency of the circuit where the power of the input signal is cut down by a factor of 2. Typically, power is represented in decibels (dB); Therefore, the corner frequency is that frequency at which the signal power is attenuated by 3 dB. Figure 16 shows the circuit used to generating the frequency response. The Resistance R6 is varied from 1kΩ to 10kΩ in steps of 1kΩ for each frequency response.

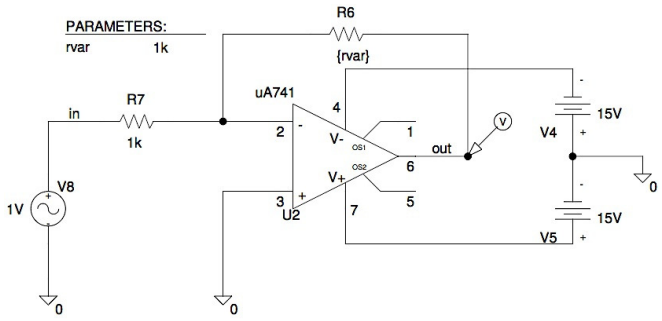
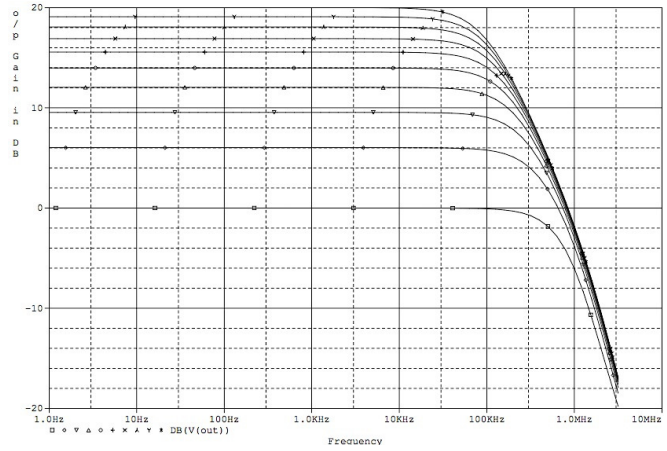
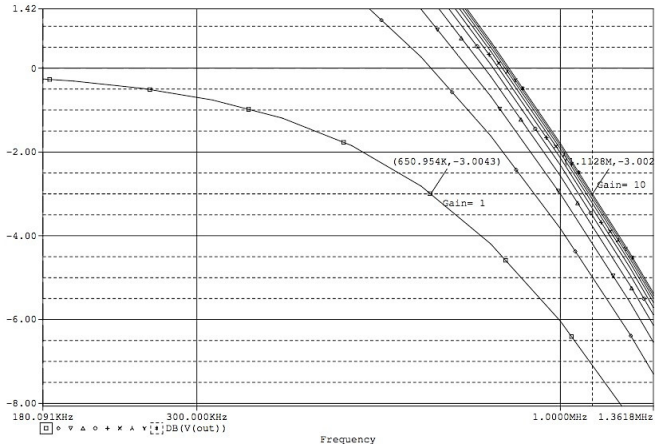


Fig.16: AC Sweep of the circuit with varying R6 value to get different response at different gains.



(a)



(b)

Figure17: Frequency response of the system. (a) Overall frequency response, (b) Zoomed in view at -3dB

After plotting the frequency response we measure for individual corner frequencies corresponding to R5 values. There for each Gain value, A_v the corner frequencies are given in table 3

Table 3: Closed Loop – 3dB frequencies

Av	Corner Frequency (Hz)
1	651k
2	916k
3	1M
4	1.04M
5	1.06M
6	1.07M
7	1.09M
8	1.1M
9	1.106M
10	1.11M

A similar frequency response is plotted for an open loop system, see figure 18 & 19. As calculated earlier the gain of an open loop Op-Amp is very high, therefore in order not to saturate the output, we will investigate the frequency response with an input AC signal of 10μV.

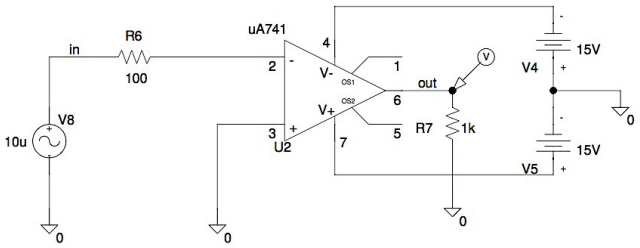


Fig.18: Frequency response circuit for an open loop system

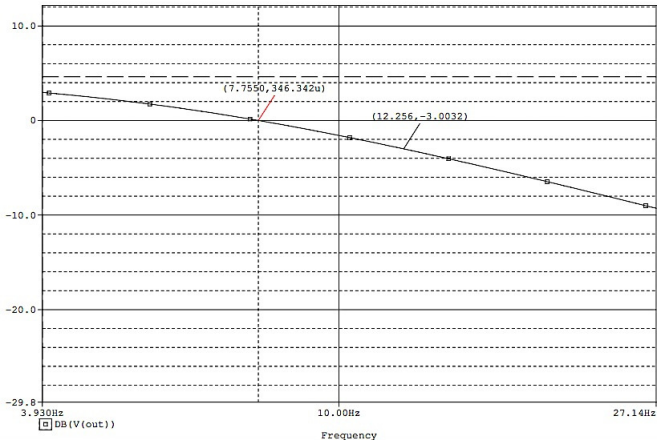


Fig.19: Zoomed in Frequency response & Unity gain frequency and corner frequency

Therefore,

The unity gain frequency = 7.75 Hz
The corner frequency = 12.25Hz

C. OP-AMP APPLICATION AS A FILTER

1. Introduction

Many analog systems are constructed using the Op-Amps as their basic building blocks. These Op-Amps are used along with external components either singularly or in a combination to form a large variety of analog systems like the analog computer, voltage-to-current converters, current-to-voltage converters, amplifiers, filters and so on.[4]

In this section we aim to understand the filter construction using these Op-Amps, more specifically a Sallen & Key filter architecture. As per figure 20 which is redrawn with impedences in figure 21,

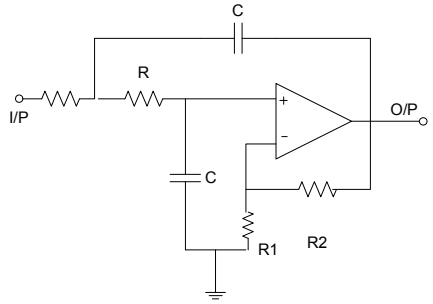


Fig.20: 2nd Order filter

We know the dc voltage gain is given by:

$$A_v = 1 + \frac{Z_2}{Z_1}$$

In order to form an integrator or a differentiator, we modify the Respective impendences. For example for an integrator we modify the impedances as:

Z_2 = C,
Z_1 = R.

Hence it can be shown that

$$v_o = -\frac{1}{C}\int i\,dt = -\frac{1}{RC}\int v\,dt$$

- equation (3)

Where, *i* is the Input current flowing through the Z_1 arm. We can rewrite the gain equation (1) for an integrator as a function of complex variable *s* as:

$$A_v = \frac{V_o(s)}{V_i(s)} = -\frac{Z_2}{Z_1} = -\frac{1}{RCs}$$

-equation (4)

Similarly, a differentiator is constructed by:

Z_2= R,
Z_1=C.

Implying that

$$v_o = -Ri = -RC\frac{dv}{dt}$$

-equation (5)

Where, *i* is the Input current flowing through the Z_1 arm. Also, can rewrite the gain equation (1) for a differentiator as a function of complex variable *s* as:

$$A_v = \frac{V_o(s)}{V_i(s)} = -\frac{Z_2}{Z_1} = -RCs$$

-equation (6) [3]

By analyzing equation (4) & (6), we see the significance of adding a differentiator and integrator to any circuit is to introduce Poles and Zeroes which is basis in any filter design.

2. Sallen& Key Filters

Figure 21 shows a generalized form of a Sallen Key Architecture. The Impedances, Z, are used for passive filter components and R3 & R4 are used to set the Pass band Gain frequency [5]

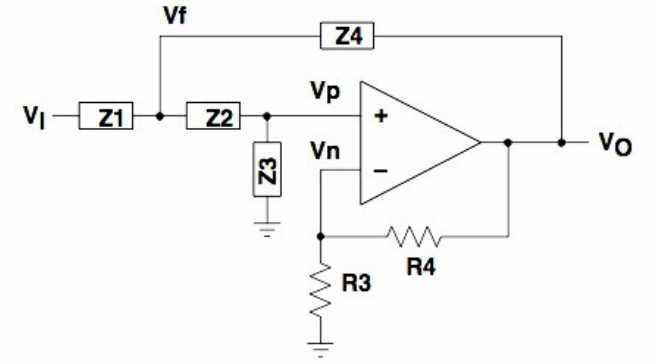


Fig.21: Generalized Sallen& Key filter architecture

Note also that the dc gain of each stage, |H(0)|, is given by $A_v$as

$$A_v = 1 + \frac{R4}{R3} \qquad \text{equation (7)}$$

and, when several stages are cascaded, the overall dc gain of the filter will be the product of these individual stage gains. This feature of the Sallen and Key structure gives the designer the ability to combine easy-to-manage amplification with prescribed filtering. [6]

There are a few steps before implementing the Values for passive components in the figure 21, which depends on:

Q, called the quality Factor

fc, called the Cut-off Frequency, or corner frequency.

Attenuation at stop band of a filter.

A_v, dc gain of the amplifier.

In this exercise we intend to compare the results between a Practical Op-Amp and an Ideal Op-Amp with the same passive component values, therefore we can safely assume:

The filter is a 2nd Order Butterworth Filter.

The Gain of the filter is 10.

Stop Band frequency is invariably adjusted by selecting a 2nd Order Filter.

We can now begin to simulate the Sallen& Key Architecture, 2nd Order Butterworth Filter in PSpice.

3. Designing the filter

Butterworth Low Pass Filter is an all pole filter with a basic frequency response as shown in the figure 22

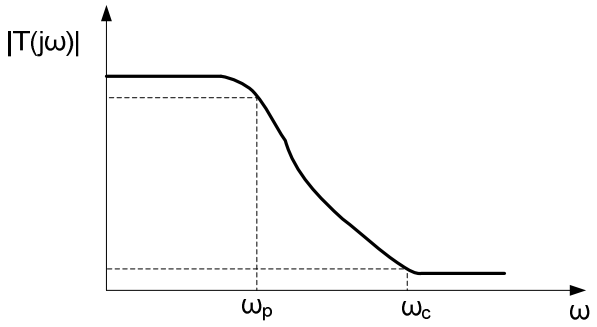


Fig. 22 Behaviour of a Butterworth filter [7]

The order of the Filter can be found out by using

$$|T\ (jw)|^2 = \frac{G_o}{1+\left(\frac{\omega_S}{\omega_C}\right)^{2N}} \qquad \text{- equation (8)}$$

Where, G_o is the DC gain.
ω_c is the Cut off frequency
ω_s is the Stopband frequency
N is the order of the filter

In our analysis the order of the Filter is given in the specification as 2nd Order.

N	Normalised Denominator Polynomials in Factored Form
1	(1+s)
2	(1+1.414s+s^2)
3	(1+s)(1+s+s^2)
4	(1+0.765s+s^2)(1+1.848s^2)
5	(1+s)(1+0.618s+s^2)(1+1.618s^2)
6	(1+0.518s+s^2)(1+1.414s+s^2)(1+1.932s+s^2)
7	(1+s)(1+0.445s+s^2)(1+1.247s+s^2)(1+1.802s+s^2)
8	(1+0.390s+s^2)(1+1.111s+s^2)(1+1.663s+s^2)(1+1.962s+s^2)
9	(1+s)(1+0.347s+s^2)(1+s+s^2)(1+1.532s+s^2)(1+1.879s+s^2)
10	(1+0.313s+s^2)(1+0.908s+s^2)(1+1.414s+s^2)(1+1.782s+s^2)(1+1.975s+s^2)

Fig. 13 Normalised Denominator Polynomials in Factored Form [8]

The Gain of a 2nd order Filter is dependent on the damping factor, ζ. Therefore we keep the coefficient of "s" in the Butterworth polynomial of the specific order (here the 7th Order) such that, ζ. = 0.707.

Also, to ensure cut-off frequency, *fc*, we need to adjust the gain. Therefore we ensure

$A_v = 3 - \alpha$ - equation (9) [9]

where A_v should be satisfied in both the equations, Eqn. (7) &Eqn. (9)

In our specification the DC Gain of the Butterworth is not specified. Therefore we substitute a gain of filter as R_4 = 10kΩ and R_3 = 1kΩ.

R and C, as shown in Figure 20, determine the Cut-off frequency as $f_c = \frac{1}{2\pi RC}$ -equation (10)

Therefore, for a given frequency of

$$f_c = 1.5kHz$$

We can assume, R = 1kΩ. And substitute the value of f_c in Eqn.(10) , to find

$$C = 0.106\mu F$$

Replacing the Sallen & Key architecture with the values of passives calculated so far, we have a circuit as shown in figure 24

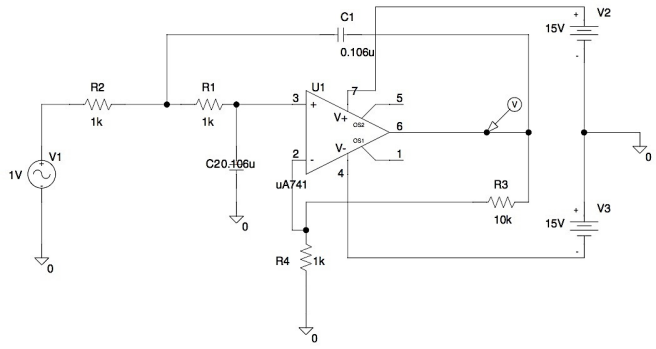


Fig.24: 2nd Order Butterworth Filter with Sallen & Key filter architecture

Circuit parameters:

Z_1=Z_2 =1kΩ, shown by R1 & R2

Z_3=Z_4=$0.106\mu F$, shown by C1 & C2

R3 = 10kΩ,

R4=1kΩ,

Simulating the frequency response of the filter in PSpice gives us the graph, shown in figure 25.

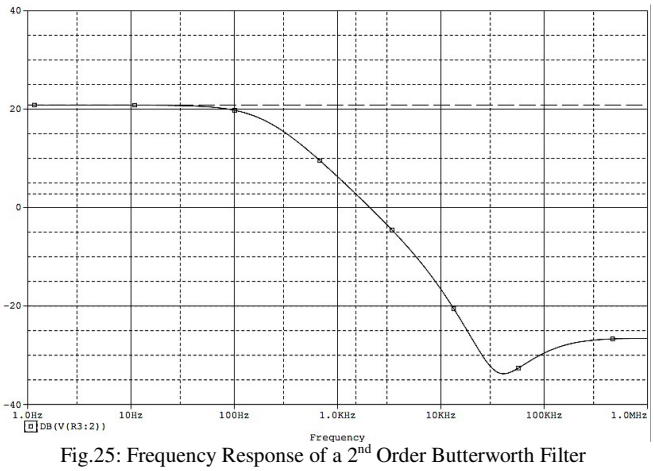


Fig.25: Frequency Response of a 2nd Order Butterworth Filter

From the graph, the Cut-off frequency is checked to be

$$f_c \approx 1.5\ kHz$$

D. RESULT & CONCLUSION

The Ideal operational Amplifier was tested and analyzed for its characteristics using PSpice& Cadence design Kit. A Practical amplifier, uA741, was tested and simulated using similar tests. All the test results and graphs are presented in this report for further investigation.

A sallen & key architecture butterfilter filter is explained and then implemented using uA741 amplifier.

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