Lesson 1: Allegro User Interface

Learning Objectives

◆ Identify the user interface (UI) components of Allegro.

◆ Navigate within the Allegro Editor window and access UI features.

Summary

In this section you will be introduced to the Allegro® PCB Layout System. You will explore the Allegro graphical user interface as well as the various programs that comprise the Allegro PCB Layout System. You will also view Allegro classes and subclasses, work with setting colors and visibility of objects, and learn how to use the **Display > Element** command to query design objects.

Primary Allegro Programs

When you install Allegro software on your computer, the installation program automatically includes several tools, some of which are:

◆ Allegro Editor

◆ Padstack Designer (Padstack Editor)

You can access these tools through the Windows **Start** button.
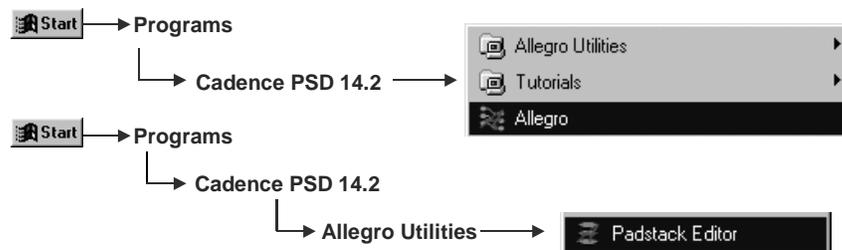
In UNIX you can enter the following commands:

allegro

pad_designer

More Information

The Allegro Editor lets you create printed circuit board designs and footprint symbols required by those designs.

The Padstack Editor lets you create or edit library padstacks, including:

- Defining the parameters of your padstacks

- Creating blind and buried via padstacks

- Adding padstack layers

- Copying padstack layers

- Deleting layers in a padstack

Other Programs

Start > Programs > Cadence PSD 14.2 > Allegro Utilities

Windows   **UNIX**

Allegro to SPECCTRA	——	**spif**
Batch DRC	——	**batch_drc**
DB Doctor	——	**DB Doctor**
Environment Editor		
Pads Translator		
Padstack Editor	——	**pad_designer**
Pcad Translator		
QuickView Update		
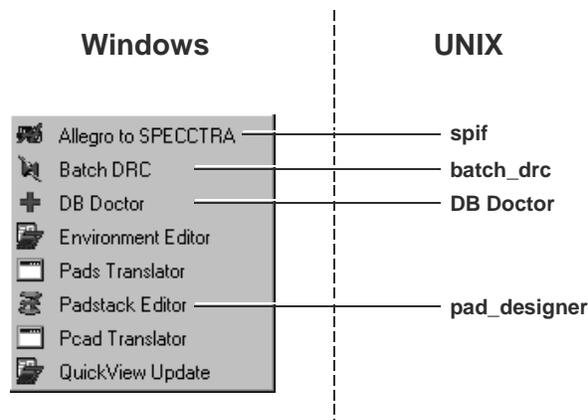
More Information

The following tools are available from your Allegro software installation directory. When using a PC, you can create your own desktop shortcuts to these tools. On a UNIX workstation, you type the commands into a terminal window.

Allegro to SPECCTRA®

The Allegro to SPECCTRA Interface tool lets you automatically prepare Allegro design data for the SPECCTRA autorouter. The UNIX command is "spif".

Batch DRC

Batch DRC lets you run a design rule check on your database without having to open the Allegro Editor. The UNIX command is "batch_drc".

DB Doctor

The DB Doctor utility lets you check the database integrity and automatically fixes file corruption problems. The UNIX command is "dbfix_ui".

Cadence PSD Tools
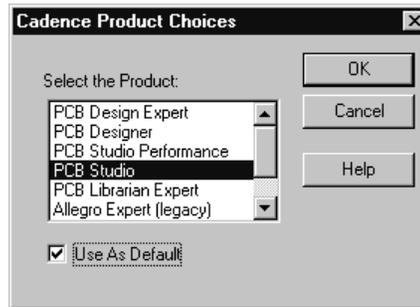
PCB Design Expert	Top of the line product. Includes high speed design rules in both electrical and physical
PCB Designer	Same as PCB Design Expert EXCEPT no electrical high speed rules
PCB Studio Performance	Same "Allegro" tool as PCB Designer
PCB Studio	Base line product. no high speed rules, no SKILL access.

More Information

If you purchased more than one type of Allegro tool, the Product Choices form will appear when you invoke Allegro or one of the other PSD tools, such as Concept. You must select from the list of Products which license you wish to use. If you do not enable the Use As Default option, the Product Choices form will be redisplayed each time you use a PSD tool. If you do enable the Use As Default option, you can still change the license you wish to use from within Allegro by using the **File > Change Editor** command.

Course Directory Structure

c:\course_install_dir (c:\user1\… for Windows NT/2000 OS)

or /<course_install_dir>/.. (UNIX OS)

allegro

project1   **project2**   **project3**   **advanced**   **symbols**   **play**   **solutions**

worklib   **devices**

root

physical

symbols
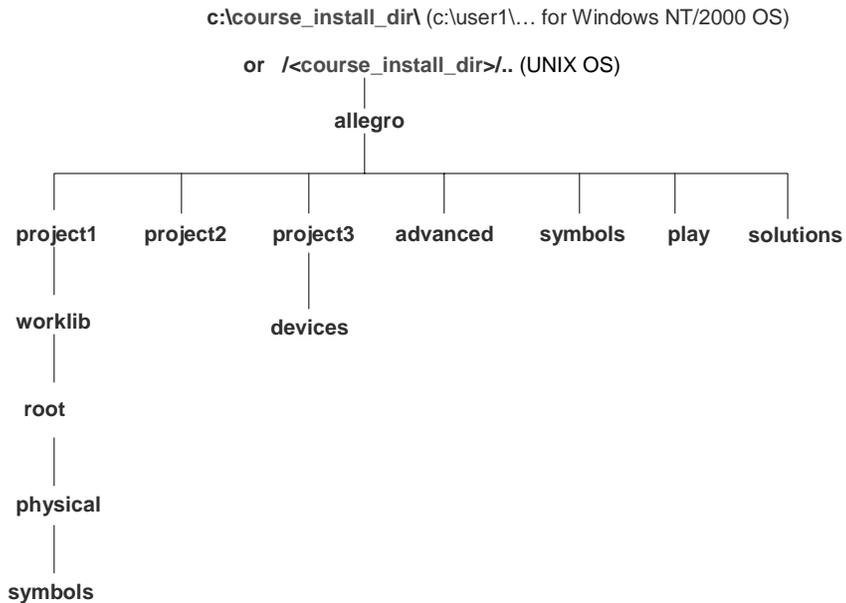
Summary

It is very important to understand and remember the directory structure presented, especially when working with the labs. Since this course has been designed for use with different schematic capture tools, several different directories have been established.

The *project1* directory is the working directory for students who are taking the Concept-to-Allegro front-to-back sequence. This *project1* directory includes the following subdirectories, in order of descending hierarchy: *worklib*, *root*, *physical*, *worklib*, and *symbols*. This directory structure is typical of the standard Project Manager tool.

The *project2* directory is for those using Capture as the front end schematic capture tool. When working with Capture, you need a *release.opj* file for netlisting, as well as the *pst*.dat* and **view.dat* netlist and back annotation files.

Finally, *project3* is for those netlisting and backannotating between Allegro and a third-party tool. The *devices* subdirectory contains all the **.txt* device files needed for importing a third-party netlist.

More Information

Other directories that you will see within the course installation are:

> *advanced* - This is the working directory for the advanced portion of the Allegro course.

symbols - All the *.psm.* and *.dra* symbols used for Allegro *.brd* designs reside in this subdirectory.

play - This is the working directory where you build library files and practice using the Allegro tool.

solutions - This directory holds all the reference board files for the labs as backup files.

Setting and Changing Your Working Directory

All files that are created or saved from within Allegro are written to the current directory by default. When opening or creating files, you can change the directory to a new location by browsing to the desired directory.
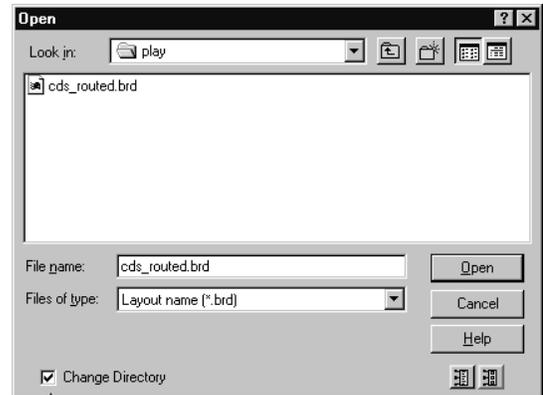
Use this option to change to the directory selected.

Summary

When opening and saving files, you must pay attention to the directory that is set as your Current Directory. This directory is displayed in the title bar of the Allegro window. When you open or save files, you can change the Current Directory by using the standard browser. If you browse to a different directory, you can make that directory the Current Directory by selecting the Change Directory option at the bottom of the window.

The first time you invoke Allegro, the Current Directory is set to a location that is specified during the software installation.

Allegro Editor and Workspace

Title Bar

Menu Bar

Icons/ toolbars

route tool set   **dimensioning tool set**

Design Window

Status Window

Console Window
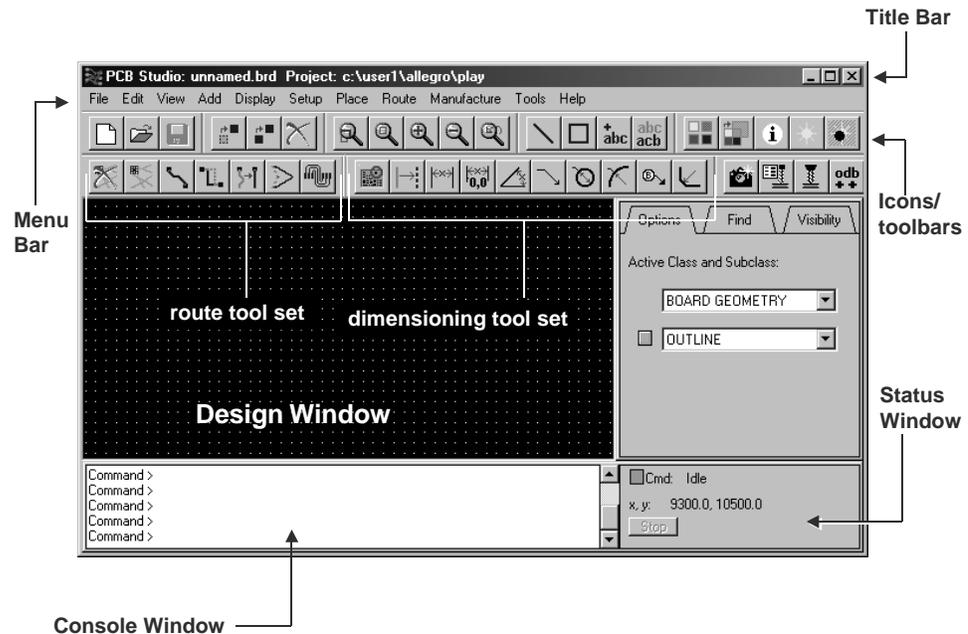
More Information

There are several different areas that you need to become familiar with when using Allegro.

Title bar - Located at the very top of the window. This specifies the Allegro product that is currently running, the database that is currently opened, and the working directory.

Menu bar - Located directly underneath the title bar. These menu items contain all the commands required to create and modify a design. To execute a command, select with the left mouse button on the menu, then select with the left mouse button again on the command to be executed. For example, to execute the **Open** command, select the **File > Open** option from the menu bar with the left mouse button.

Icon toolbar - Located immediately below the menu bar. This area will be discussed shortly.

Design window - This is where you will do most of your work on the printed circuit board design.

Console window - The bottom left portion of the Allegro window. This window has two major functions. The first function is to display messages and prompts to you. The second function is to allow you to type in Allegro commands.

Status window - Located to the right of the Console window. The Status window contains the current command being executed. In this case, the word **idle** is displayed because no command is currently active.

The Status window also contains the X and Y coordinates of your cursor location when your cursor is placed in the Design window. The X and Y coordinates are relative to the 0,0 point of the design. The Status window includes the **Stop** button, which you can use to interrupt a current command. The **Stop** button is presently grayed out or not available because there is no command currently active.

To the left of the CMD text string, there is a box that is colored green, yellow or red. If the box is green, that means Allegro is ready for your command. If the box is yellow, the system is working—but you can interrupt the system by using the **Stop** button, hitting **Ctrl-C**, or hitting the **Escape** button. If the box is red, the system is working and there is nothing you can do to interrupt it. You must wait until the box turns either yellow or green again.

Toolbar

Toolbars are used to store common icons in a group. Toolbars can be added, modified, or made invisible by using the **View > Customization > Toolbar** command.
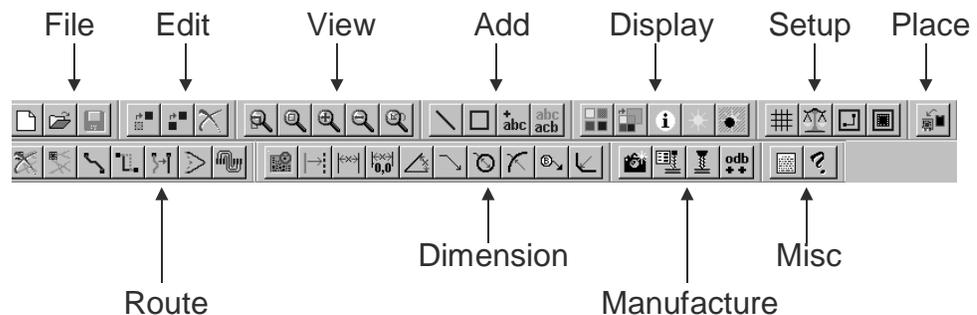

More Information

The icon toolbar is located immediately below the menu bar. Using icons is a faster way to initiate some of the more common Allegro commands. For example, the second icon from the left on the top row is the **File Open** icon.

Icons are further grouped into toolbars. As you can see in the second row of icons, the seven icons to the left are grouped into a toolbar called ROUTE. Each toolbar can be turned on or off by choosing the **View > Customization > Toolbar** option from the menu bar.

Control Panel and World View Window
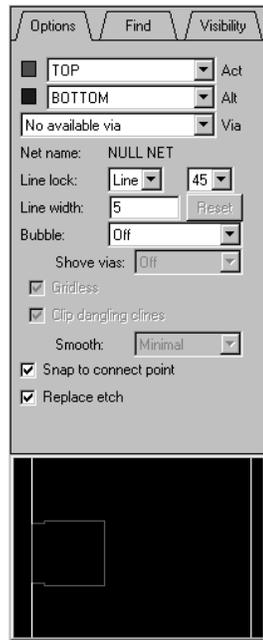
◆ Options Folder Tab
  ▪ Displays current parameters and values for the active command
  ▪ Contains fields that let you control the actions performed by the current command

◆ Find Folder Tab (Find Filter)
  ▪ Controls which objects are found when directly selecting objects
  ▪ Can also select objects by entering their name

◆ Visibility Folder Tab
  ▪ Controls visibility/invisibility of conductor/etch elements in the design

◆ World View Window
  ▪ Allows you to display a particular section of your design
  ▪ Displays the current viewing area relative to entire design

More Information

The area immediately to the right of the Design Window contains the Control Panel and the World View Window. The Control Panel has three folder tabs titled Options, Find, and Visibility. The Options folder tab contains parameters that are used to control the current interactive command. The Find Folder tab is used to control what type of objects are selected. This folder tab has options for use when selecting items with the mouse or when selecting items by their name. The Visibility Folder tab is a quick way to control the visibility of conductor elements in your design such as etch, pins, vias and so forth.

The bottom portion of the Control Panel is a graphical area titled World View Window. Using the World View Window is another way that you can control panning, zooming, and redrawing of your graphical area.

You can change the position of the Control Panel by selecting the **View > Customization > Display** option from the menu bar.

Getting Help

- ◆ WinHelp
- ◆ Online HTML-based documentation
- ◆ Education Services training materials
- ◆ SourceLink service (on the Internet): sourcelink.cadence.com

    OR . . .

    - From within certain tools you can select Help-Cadence

    OR . . .

    - Go to the Cadence home page (http://www.cadence.com). Select the Customer Support link.

    You must have a maintenance contract to log in (authorization number)
- ◆ Customer Response Center (CRC) 1-877-237-4911
- ◆ Users Group
- ◆ Methodology Services
  Contact your sales representative for more information.

More Information

There are several ways to get help with your software from Cadence. Each tool has its own task-oriented help menu, which is accessed from the common Help user interface found with other Windows applications. There are also HTML-based manuals that you can access by choosing **Help > Allegro > Documentation** from the Allegro menu.

SourceLink is a Cadence website where users can search for known problems and solutions, as well as find application notes written by Cadence application engineers. You can get to SourceLink with your Web browser at *www.cadence.com* or by selecting **Help > SourceLink** from the Allegro menu.

If you need to report a bug in the software or documentation, you can contact the Cadence Customer Response Center via telephone at 1-877-237-4911 or you can send an email to *support@cadence.com.*

Cadence also has a team of engineers available to help customers in a variety of fashions, ranging from customized live classroom training to printed circuit board and multi-chip module design services.

Allegro Online Help

Help > Contents
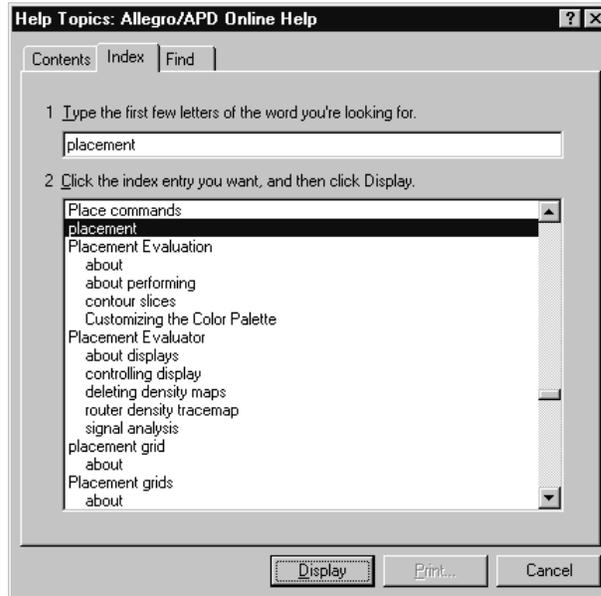
More Information

The Allegro online help system is similar to the standard Windows help mechanism. The Contents folder tab contains help topics that are organized in a reference manual format. The Index folder tab is a mechanism whereby you can search for help on certain topics, such as placement. You use the Find folder tab to search the help files for a specific phrase or word, such as ROUTE_PRIORITY.

Lab

- ◆ Lab: Allegro Tour
  - ■ Starting Allegro and other programs
  - ■ Choosing a tool from the Allegro program suite
  - ■ Traversing the course directory structure
  - ■ Setting your working directory
  - ■ Opening a board design
  - ■ Touring the Allegro user interface
  - ■ Accessing online Help, Allegro documentation, and properties information

More Information

The following lab will teach you how to start Allegro, set your current working directory, explore the user interface, and access the online help files.

Lab 1-1:   Allegro Tour

Objective: Learn how to log in and start Allegro, set your working directory, view a printed circuit board design within the Allegro editor, preview the menus, and access the online Help system.

◆ If you are working in the Windows environment, you may see icons for starting Allegro executables on the desktop display, but instructions in this book will refer to the Windows Start button.

◆ If you are working on a UNIX system, then you can type commands in a shell.

Note

The method you use for starting Allegro in this lab will be the same one you use in later labs whenever you are instructed to start Allegro.

Logging on

Logging on requires that you issue a username and a password, which depends on whether you are working in a Windows or a UNIX environment.

Windows NT/2000

1. To log onto a Windows system, press **CTRL+ALT+DEL** (all keys at the same time).

   The Login Information dialog box displays.

2. Provide the following information in the Login Information dialog box, then click **OK**:

Username	**user1** (or whatever username your instructor specifies)
Password	**training** (or whatever password your instructor specifies)
Domain	**ES** (or whatever domain your instructor specifies)

UNIX

1. To log onto a UNIX system, at the command prompt, enter the following:

   user10 (or whatever username your instructor specifies).

2. At the command prompt, enter the following:

   training (or whatever password your instructor specifies).

3. To start X Windows and the Motif window manager, enter the following:

xwin

Several windows appear on your screen. One of the windows has the banner title *Cadence*.

4. Place your cursor in the command line of the Cadence window and enter the following:

cd ~/allegro/play

This changes your location to the *play* working directory, where you will perform much of your work for the first few labs. The *solutions* directory is where the reference files are stored.

At this point, you should be logged onto your system and ready to start Allegro.

Choosing Products and Starting Allegro

In this lab, you will open a routed PCB design in the Allegro Editor window, then explore aspects of the design as well as the Allegro user interface.

1. Start Allegro in one of the following two ways, depending on whether you are working in Windows or UNIX:

    a. If you are working in Windows, start the Allegro Editor by clicking the Windows **Start** button (bottom left of your screen) and choosing the **Programs > Cadence PSD 14.2 > Allegro** menu option.

    b. If you are working in UNIX, type the following command at the shell prompt:

    allegro

    If this is the first time you have launched Allegro, the Cadence Product Choices dialog box may appear. Otherwise, the Allegro Editor window appears, as shown in the following figure.

2. If the Cadence Product Choices dialog does not appear, choose **File > Change Editor** from the top menu bar in the Allegro Editor.

The Change Product Choices dialog box appears.
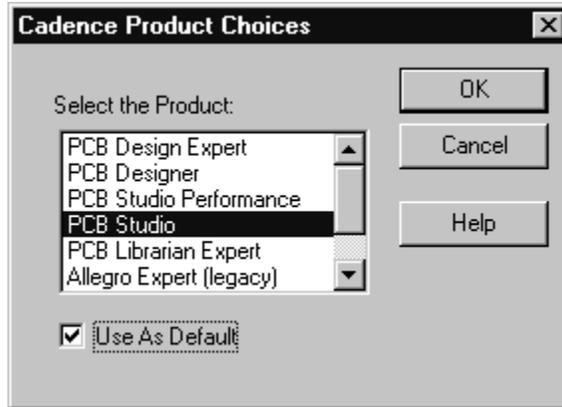
3. Select **PCB Studio** and check the **Use As Default** option, then click **OK**. This sets the PCB Studio version of Allegro as your default. This is the version we will use throughout the course.

4. If the **Help Topics:** window displays, select **Cancel** to close this window. You will investigate the help menus later.

Your window will look something like the following:
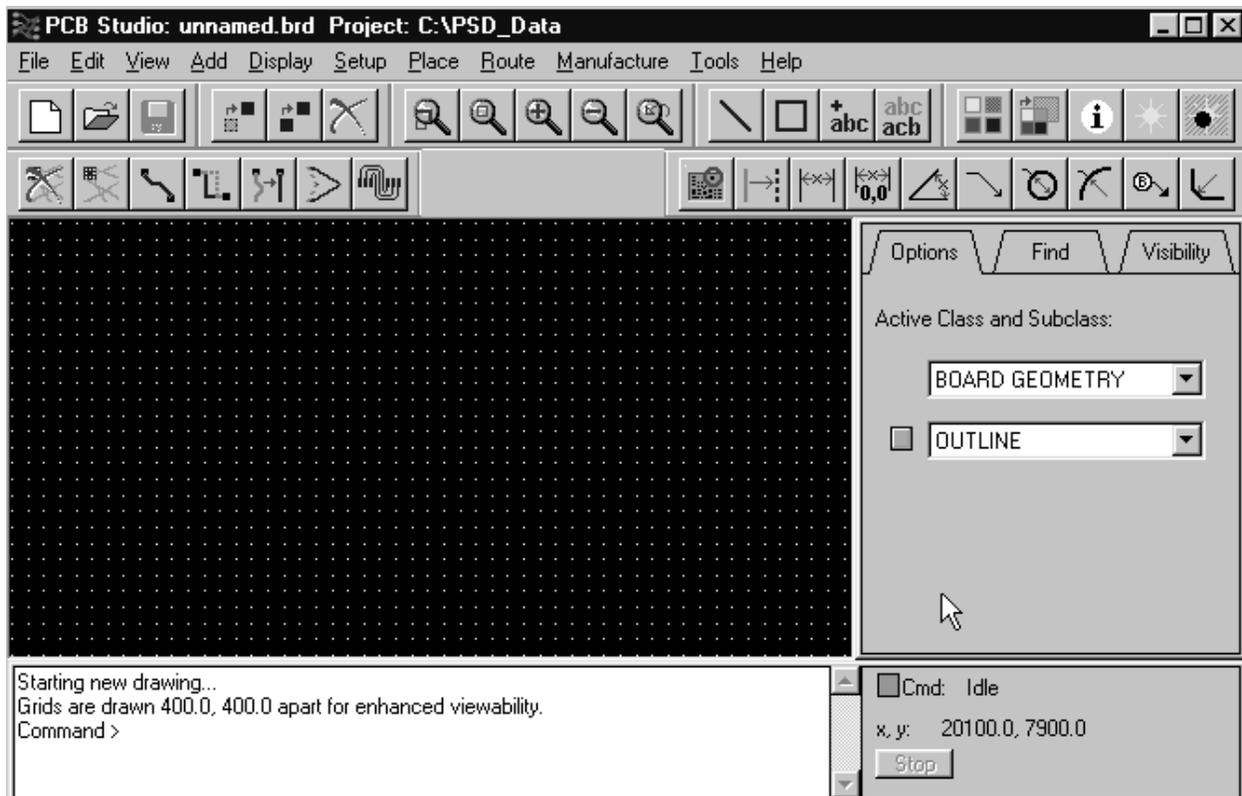
Setting Your Working Directory, Opening aBoard Design, and Viewing Tool Sets

1. From the top menu bar choose **File > Open**. An Open file browser window appears.

2. Navigate to the *play* directory, and select the ***cds_routed.brd*** file.
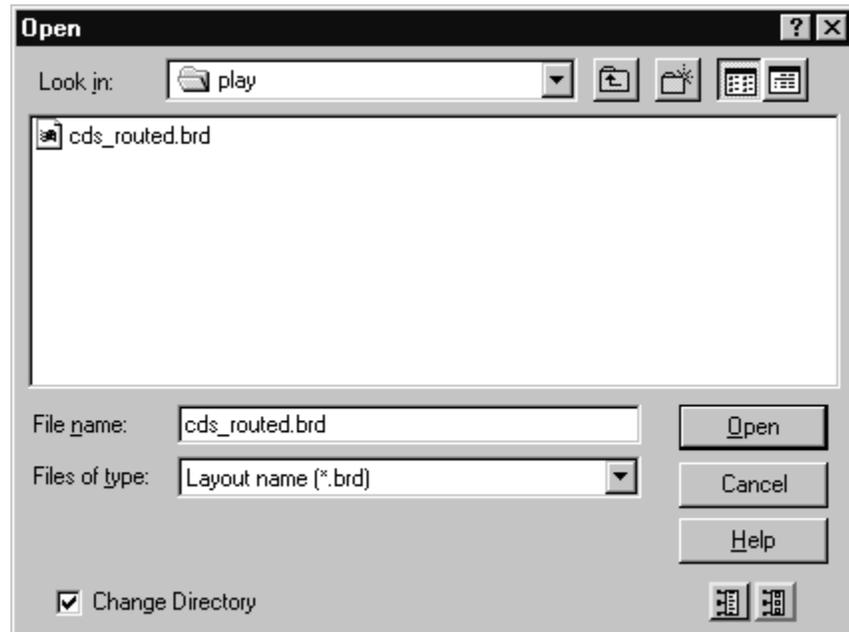
3. Verify that the Change Directory box is checked.

    This option sets your working directory to *play.*

4. Click **Open**.

    The *cds_routed.brd* design file is displayed in your Allegro work area.

Note

You can also open a file by double clicking it.

Exploring the Allegro User Interface

In this part of the lab, you will explore various menus and buttons in the Allegro Editor window to see how the user interface works.

1. Click the maximize button to fill your screen with the Allegro Editor window, if it is not already maximized.

2. Referring to the overview in the previous lecture, identify the following parts of the Allegro Editor window:

    ■ Menu bar organization and options

    ■ Icon ribbon toolbar

■   Toolbars for placement, route, analysis, and manufacturing

■   Design window

■   Console window (and command line)

■   Status window with its "traffic light" and coordinate readouts

■   Control panel: Options, Find and Visibility tabs

■   World View Window

You will access all these features in more detail in later labs.

3. View the menu options.Click the **File** menu option and note the available options. Slowly pass your cursor over the menu items (**Edit, View, Add** and so on) from left to right. Note the various menu options available under each menu item.

4. Select any place in the Allegro work area to close your latest pull-down menu.

5. View the tool tips on the toolbar icons.Slowly drag your cursor across the toolbar from left to right and read the tool tips that appear. DO NOT CLICK. When you come to the **Zoom Fit (F9)** icon, click it.

The entire *cds_routed.brd* design is framed in your editor.

6. View the names of the commands associated with the toolsets for placement, route, analysis, and manufacturing by slowly dragging your cursor across toolset icons from left to right and reading the tool tips as they appear.

Accessing the Help System

1. From the top menu, choose **Help > Allegro Help**.

The Help Topics dialog box appears.

2. Activate the **Index** tab by clicking on it.

From the index you can find out information about almost any detail of Allegro.

3. Enter the word **placement** in the field under 1 as shown in the figure, but do **NOT** click Display.
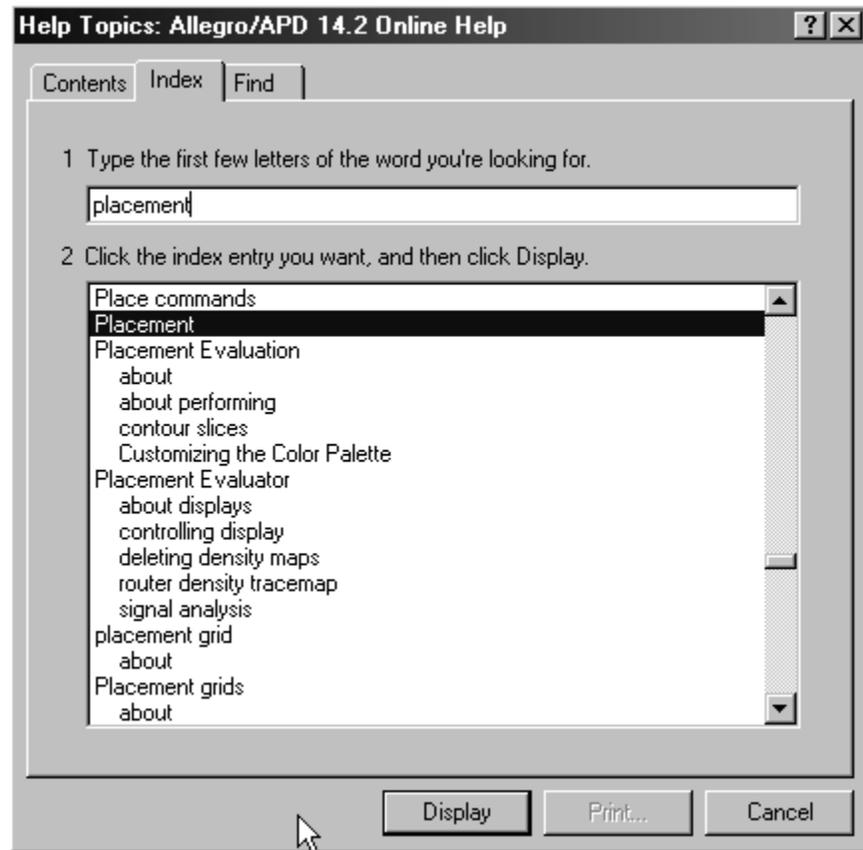
The list of topics associated with the *placement* keyword is displayed in a Topics Found dialog box.

For some index terms there are multiple topics available with information about the term. If a term has only one corresponding topic, a Help window automatically opens to that topic.

4. Experiment by typing in various index terms, clicking the **Display** button, and viewing different topics.

5. When you are finished experimenting with Help, close any open Help windows.

**STOP** **End of Lab**

Mouse Buttons
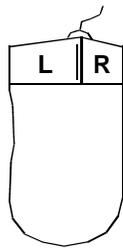
Two-button mouse:

◆ **Left mouse button (LMB)** — Select design elements, menu buttons and icons. Window selection available by dragging.

◆ **Right mouse button (RMB)** — Open pop-up menus.

◆ **Shift plus right mouse button (SHIFT+RMB)** — Pan, zoom control.
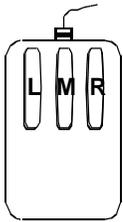
Three-button mouse:

◆ **Left mouse button (LMB)** — Select design elements, menu buttons and icons. Window selection available by dragging.

◆ **Right mouse button (RMB)** — Open pop-up menus.

◆ **Middle mouse button (MMB)** — Pan, zoom control.

Summary

Allegro supports either a two-button mouse or a three-button mouse. However, it is much easier to use a three-button mouse. Using a three-button mouse eliminates the need to hold down the Control key while using the right mouse button to pan, zoom in and zoom out.

More Information

Left Mouse Button

or..

Use this button to select graphic elements in a design (such as lines, pads, and text). The selected feature is highlighted. Must be used in conjunction with an active command.

To select a group of items, you create a selection rectangle. To do so, first you click the left mouse button to pick a corner for the rectangle, then you hold the left mouse button and drag your mouse, creating a rectangle. All applicable items within the rectangle are selected.

Use this button to select commands from menus or icons.

Some forms contain entry fields with a list of built-in options. To display and select these options, use the left mouse button in the data field (for example, the Options tab).

Right Mouse Button

or

Displays a pop-up menu containing options associated with the current command. This mouse button is also used with the control key (**CTRL**) to execute Allegro "strokes."

Middle Mouse Button

or.. ◄Shift
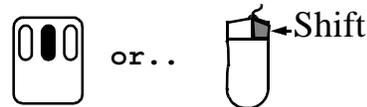
Press and hold the middle button while moving the mouse in the direction you want to pan. If you click the middle mouse button, the system will either zoom in or zoom out, based upon the direction you move your cursor. If you move from top left to bottom right, the display will zoom out. If you move from bottom right to top left, the display will zoom in. In both cases, you will see a rectangle that depicts the new zoom area.

Controlling the Window Display

View > Zoom … menu options

| View	Add	Display	Setup	Plac
Zoom By Points			F8	
Zoom Fit			F9	
Zoom In			F10	
Zoom Out			F11	
Zoom World				
Zoom Center				
Zoom Previous				
Color View Save				
Color View Restore Last				
Refresh				
Customization				►
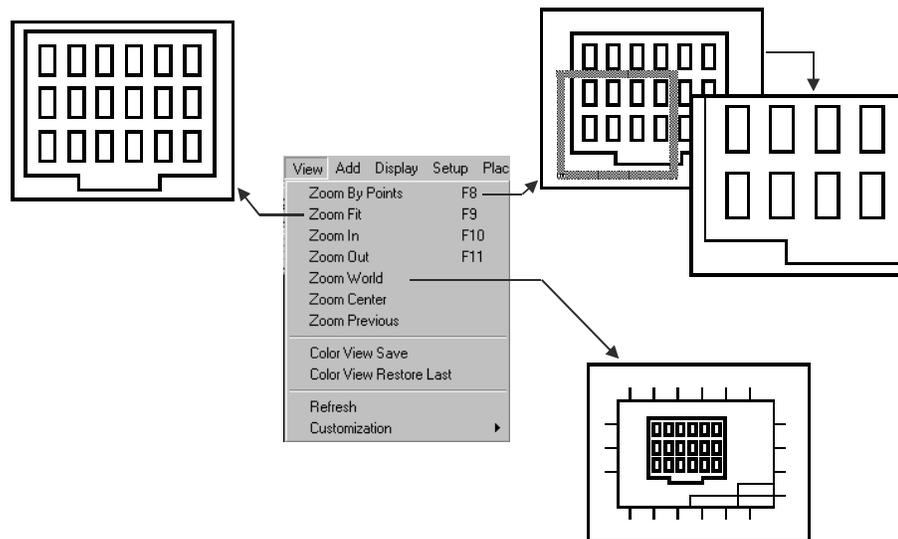
More Information

There are several commands available to change what is displayed in your current work area or the Design window. By choosing the View pull-down menu in the menu bar, you have the following options:

- ◆ **Zoom by Points** specifies a new display area by letting you pick two diagonally opposed points. After you pick the first point, a frame stretches from the first point to the cursor. Picking a second point defines the size of the new work area.

- ◆ **Zoom Fit** creates a view that includes, but is no larger than, the board.

- ◆ **Zoom In** magnifies or zooms in to a smaller area of the drawing that remains centered about the same point.

- ◆ **Zoom Out** increases the displayed area of the drawing. This shows more data in your Design window and makes objects become smaller.

- ◆ **Zoom World** displays the entire extents of the drawing in the work area.

- ◆ **Zoom Center** redisplays the drawing area with the center being a point that you select.

- ◆ **Zoom Previous** displays the previous viewing area.

- ◆ **Color View Save** allows you to save the current visibility settings.

- ◆ **Color View Restore last** restores the previous color view.

- ◆ **Refresh** simply performs a redraw of the current display area.

Navigating in the World View Window

Whole design ——————————————▶

Current display window ———————————▶

Board outline ——————————————▶

Cmd: hilight
x, y: 2695, 2430

Right mouse button popup ——————————————▶

Done
Oops
Cancel

Move Display
Resize Display
Find Next
Find Previous
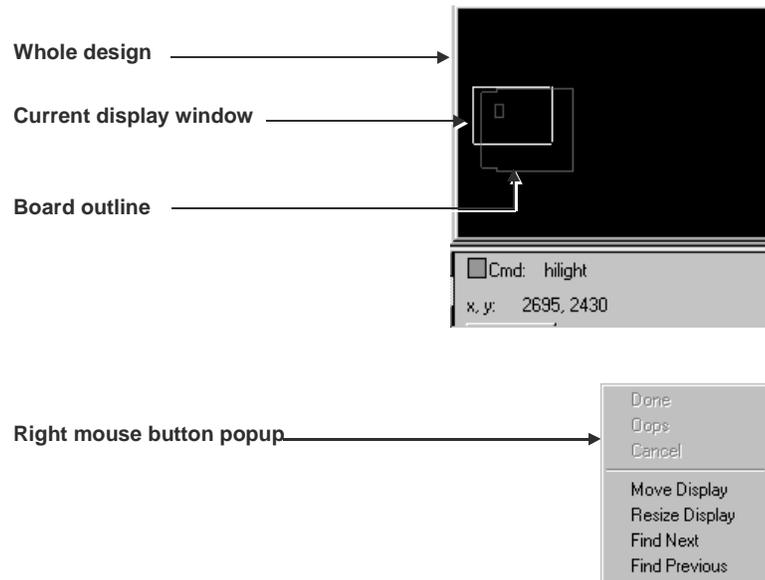
Summary

The World View window is located at the bottom of the Control Panel. It gives you quick and convenient access to the panning and zooming commands. The World View window has a representation of the board outline and also indicates the portion of the board where you are currently zoomed in.

More Information

To display the World View window pop-up menu, first you left click and then right-click right in the World View window. The pop-up menu appears.

◆ The **Move Display** option moves the display to the location you specify in the World View window. You can accomplish this by clicking and holding the middle mouse button and moving the cursor in the World View window.

◆ The **Resize Display** option changes the work area display size. You can also accomplish this by clicking and holding the left mouse button and dragging the cursor in the World View window.

◆ The **Find Next** option centers the work area view on the next highlighted object. You can also accomplish this by clicking with the left mouse button in the World View window.

◆ The **Find Previous** option centers the display on a highlighted object that is previous in the list.

Zoom Control Using the Middle Mouse Button

Circle represents the original selection point made by the middle mouse button select.

Arrows represent the direction in which the mouse is moved.

Zoom Prev

Zoom by Points   **Zoom by Points**

Zoom Cancel   **Zoom Fit**

Zoom Out   **Zoom Out**

Zoom Out
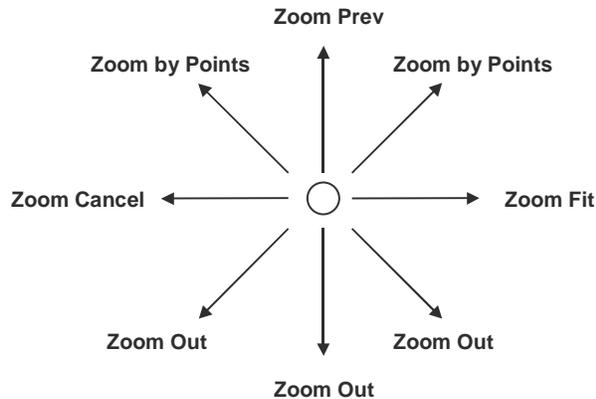
If little-to-no mouse movement is made, and a second middle mouse button select is made, a Zoom Center command will be executed.

More Information

The middle mouse button can also be used to zoom in and out of your display. You first start by selecting a point inside your current work area. You do NOT want to hold the middle mouse button as you would when you want to perform a dynamic pan. Based upon the direction you move your mouse, the new area can be zoomed in (as notated by Zoom by Points) or can be zoomed out (as notated by Zoom Out). Also, you can perform a zoom fit (as notated by Zoom Fit) or a Zoom Previous (notated by Zoom Prev). If you start the zoom and then want to cancel the zoom, move your mouse in the direction notated by Zoom Cancel.

If you select close to the same point twice, the selected point will become the new center of your work area (the Zoom Center command).

Default Aliases for Function and Control Keys

Key	Command	Key	Command
F1	Help	SF1	Add Connect
F2	Done	SF2	Grid
F3	Oops	SF3	Hilite Pick
F4	Cancel	SF4	Dehilite All
F5	Show Element	SF5	Redisplay
F6	Property Nets	SF6	Slide
F7	Edit Vertex	SF7	Move
F8	Zoom Points	SF8	(available)
F9	Zoom Fit	SF9	Write temp
F10	Zoom In	SF10	(available)
F11	Zoom Out	SF11	(available)
F12	(available)	SF12	(available)

More Information

The function keys on your keyboard are also aliased to Allegro commands. The table shows the default function key aliases. For example, to invoke the Zoom Fit command, you could either select **View > Zoom Fit** from the menu bar or simply hit the F9 key on your keyboard. To invoke the Move command, you could either select **Edit > Move** from the menu bar, or use the Shift and F7 keys on your keyboard.

Running Commands with Strokes

Strokes are predefined patterns of mouse movements. The Allegro tool interprets stroke patterns and activates commands.

Stroke	Equivalent command	Key combinations
C	Copy	CTRL+C
M	Move	SHIFT+F7
Z	Zoom In	F10
U	Oops (Undo)	F3
W	Zoom World	—
∧	Delete	—

More Information

Some Allegro commands such as Zoom, Move, and Copy are aliased to mouse *strokes*. A mouse stroke is a predefined mouse movement pattern that can be recognized by the Allegro Editor and used to invoke an Allegro command.

To draw a stroke you must hold down the control (CTRL) key on the keyboard, along with the right mouse button. If you move the mouse in one of the predefined patterns, Allegro invokes the associated command. When you use strokes to run certain commands, the following conditions apply:

◆   The Zoom World stroke can be drawn anywhere on the design.

◆   The Zoom In stroke zooms in to the area in which you draw the **Z**.

◆   The Move, Copy, and Delete strokes select the object under the first point of the stroke.

Controlling the Toolbars

**View > Customization > Toolbar**
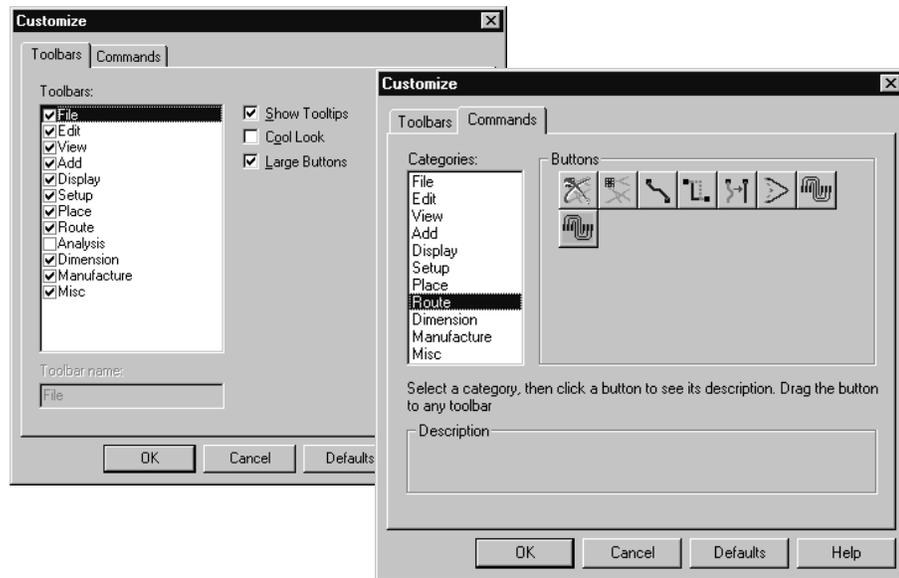
More Information

You can customize the toolbar by selecting **View > Customization > Toolbar** from the menu bar. Under the Toolbars tab you can add or remove groups of icons from the toolbar. You can also enable or disable display of Tooltips and Large Buttons or set a Cool Look.

Under the Commands tab you can control which icons are displayed in each of the toolbar groups. The toolbar settings are stored in an Allegro initialization file and are read each time you invoke Allegro. They are not stored in the Allegro database.

Drawing Parameters

Setup > Drawing Size
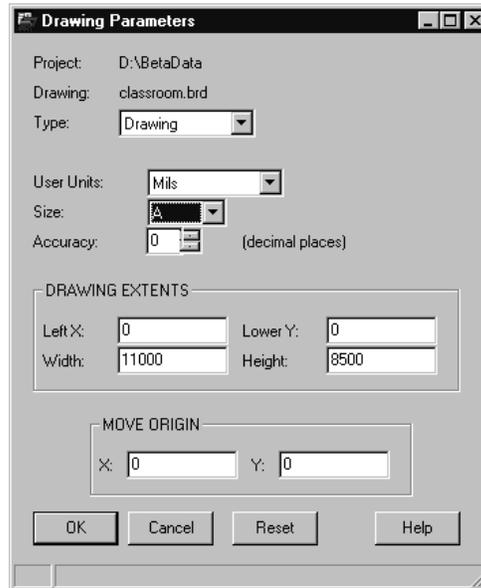
More Information

Virtually all design activity (symbol and layout creation) occurs within the context of a "drawing." To access the Drawing Parameters form, select **Setup—Drawing Size** from the top menu bar.

User Units specifies the unit of measure used during the design process. The options are Mils (default), Inches, Microns, Millimeters, or Centimeters.

Size specifies the size of the drawing area required. The standard sheet sizes are: **A** (11x8.5), **B** (17x11), **C** (22x17), **D** (34x22), or **Other** (user-specified).

Accuracy sets the accuracy of the drawing database. This value (ranging from 0 to 2) denotes the number of decimal places that can be used when defining feature sizes (pad sizes, grid sizes, line widths, and so on), or when entering x, y coordinates at the Allegro command line. If the user unit is mils, an accuracy of zero means sub-mil values are either rounded up, or not accepted at all. Accuracy settings should be compatible across all design processes to avoid rounding off problems.

Drawing Extents shows the height and width of the drawing, and the location of the lower left corner with respect to the drawing origin (located in the lower left corner by default).

Allegro Layout System   1-25

Move Origin relocates the drawing origin (datum 0,0). The x, y coordinates for the new origin are transferred into the Drawing Extents section. (Changes are indicated in the Left X field and the Lower Y field in the Drawing Extents form.)

Note

You can change the above items at any time during the design process.

Drawing Options: Display and DRC
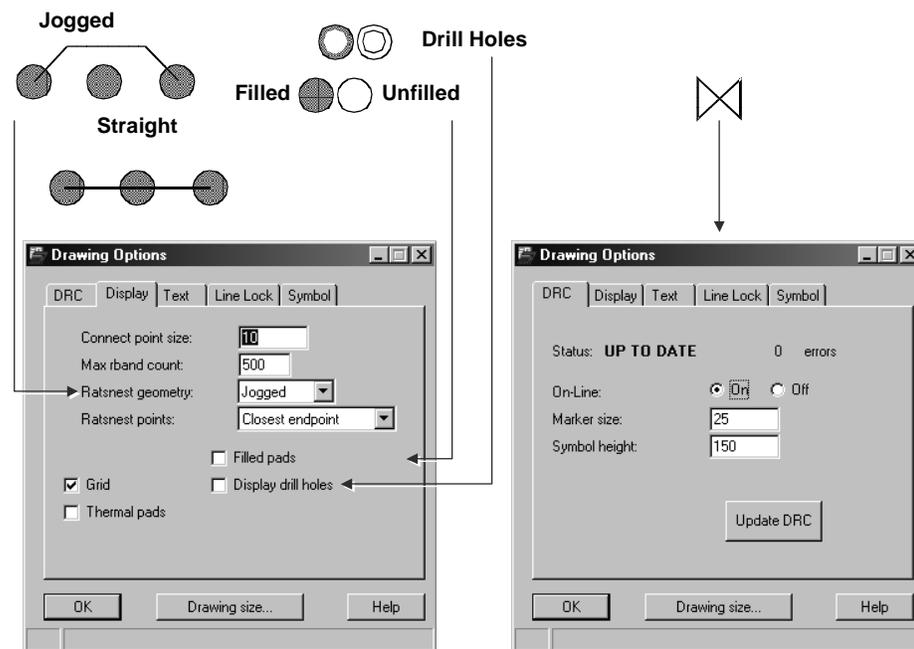
More Information

This menu displays current settings for various design operations. It is divided into five categories: Display, DRC, Line Lock, Text, and Symbol. The default settings are shown.

The Display Section:

Max Rband Count is the maximum number of rubber bands displayed when placing or moving a component.

Ratsnest Geometry determines shape of ratsnest lines. Options are Jogged or Straight.

Filled Pads indicates whether pins and vias are filled or unfilled.

Thermal Pads displays the Thermal Relief Flash symbol or anti-pad size for negative planes.

**Display Drill Holes** displays the drill hole along with the pad.

The DRC Section:

>**Status** indicates whether or not DRC markers are up to date.
>
>**Online** options are On or Off to let you toggle the online DRC error checking.
>
>**Marker Size** determines the size, in user units, of the DRC "bow tie."
>
>**Symbol Height** indicates the *default* height of all package symbols. To override this default value, specify the height in the package symbol definition.

Drawing Options: Line Lock and Symbol
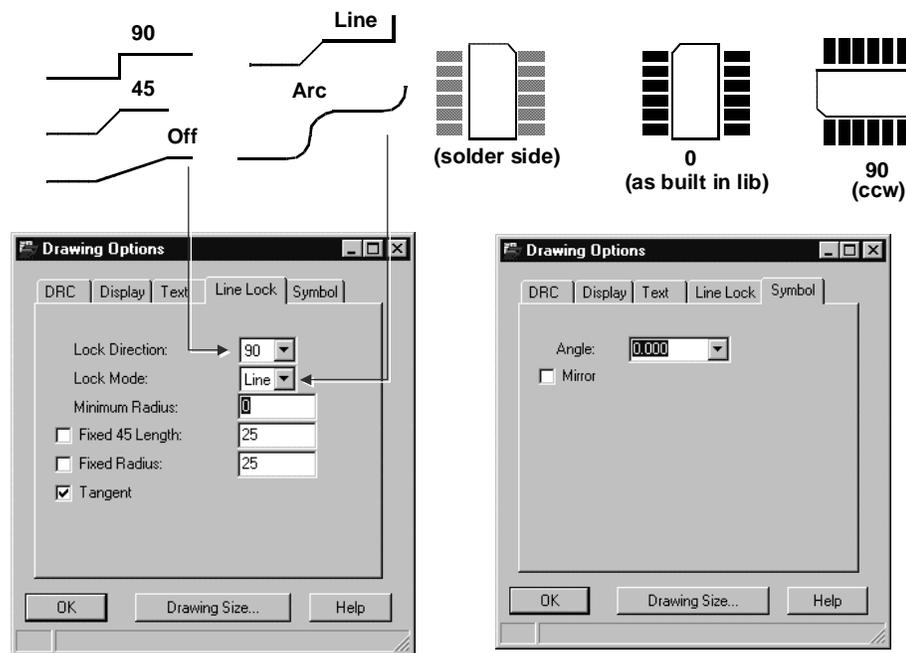
More InformationNotes

The Line Lock Section:

>**Lock Direction** lets you specify whether orthogonal, diagonal, or any-angle lines can be added. The available values are 45, 90, and Off.
>
>**Lock Mode** specifies whether new lines will be added as straight segments or arcs.
>
>**Minimum Radius** determines the minimum radius allowed for an arc.
>
>**Fixed 45 Length** specifies the length, in user units, of 45-degree segments.
>
>**Fixed Radius** specifies the radius, in user units, of arcs.

**Tangent** causes an added line to lock on to the tangent of an arc or circle.

The Symbol Section:

Angle specifies the initial rotation of package symbols during manual placement.

Mirror - during manual placement, the Allegro tool assumes the active side is the top (default). Toggle this button ON to change that default setting to the bottom (or solder) side.

User Preferences

Setup > User Preferences

Can be effective:
- **Immediately**
- **Restart**
- **Next Command and so on**

Brief description of variable
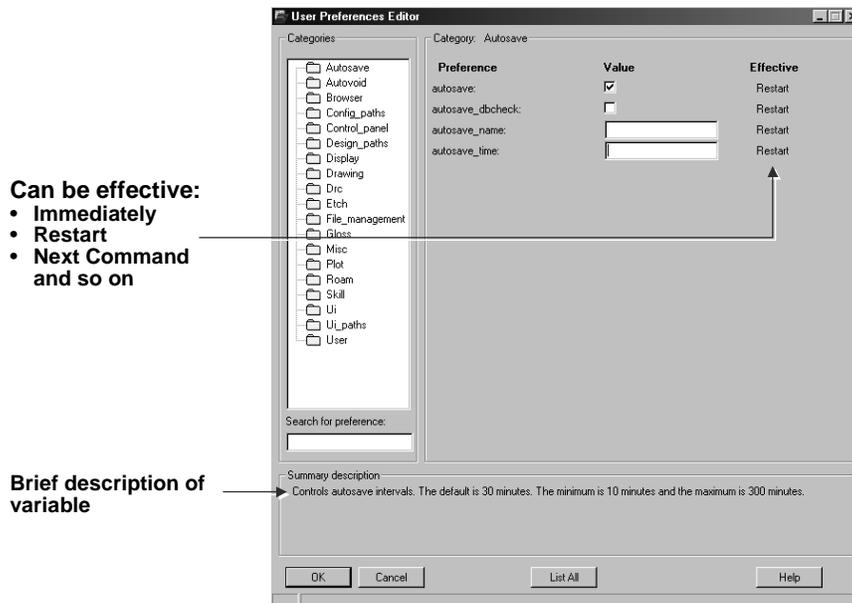
Summary

The User Preferences Editor allows you to set or unset the Allegro preferences, also known as the Allegro environmental variables. All changes are written to the end of the user's "env" file. This section of the env file should NEVER be modified manually. If the env file does not exist, it will be created upon successful completion of this command.

More Information

The major sections of the User Preferences Editor are as follows:

Categories

All preferences that can be set are grouped together based upon like functionality. All available categories are listed on the left side of the form. Select the category name in this section of the form to enable the setting of the preferences.

Category: <category name>

When you select a category from the left side, all the preferences in that category are listed in the Category section, located on the right side of the form. Note that certain variables can only be set or unset, while other variables require values to be entered. This section contains the Preference name, the current Value, and the Effective period.

The Effective period can have several values, including Next Command or Restart. Next Command specifies that the preference will take effect after the OK button has been selected. Restart specifies the preference will not take effect until Allegro has been terminated and restarted again.

Summary description

This section of the form displays a description of the preference selected.

Lab

◆ Lab: Navigating the Allegro User Interface
- Manipulating mouse buttons
- Choosing options from a pop-up menu
- Panning your view
- Applying the View command and zoom options
- Working in the World View window
- Using strokes
- Customizing your view and toolset by changing menus and toolbars
- Setting drawing options

More Information

The following lab will teach you how to use the mouse, pan, zoom and use the World View window to change your display area, use strokes, work with menus, and set the drawing options for Allegro.

Lab 1-2:   Navigating the Allegro User Interface

Objective: Learn how to use mouse buttons, navigate within the Allegro Editor window to manage your view, and customize some of the features of the user interface.

Note

All mouse commands in this course assume that you are using a three-button mouse. If you have a two-button mouse, you can hold the **SHIFT** key and use the right mouse button (**SHIFT**+**RMB**) for any commands specified as the middle-mouse button.

Using a Pop-Up Menu and View Panning

1. Choose the **Route > Slide** option from the top menu by using the left mouse button (LMB).

2. Move your cursor into the work area window and right click.

   A pop-up menu appears.

   There are different pop-up menus associated with different tools. Pop-up menus are very much context specific.

3. Select the **Cancel** option in the pop-up menu to exit the Route Slide command.

4. Place the cursor in the work area. Press (and hold) the middle mouse button down and slide the mouse to the left, right, up, and down.

Note

If you have a two-button mouse, you can press (and hold) the SHIFT key while you hold the right mouse button down and slide the mouse.

Notice how the design shifts in the direction of your cursor movement. This is *panning*. Also notice how the view changes in the World View window at the bottom right of the Allegro Editor window.
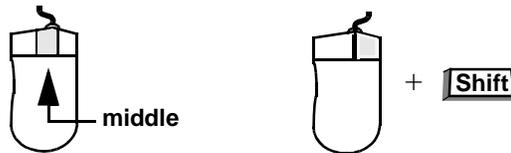
Using the View Command and Zoom Options

In this part of the lab, you will use the View command from the top menu.

1. Select **View > Zoom By Points** from the top menu.

   The Allegro message area prompts you to pick the first corner of a new view window.

2. Click to place the first corner of the new window.

   As you move your cursor, a rectangle with inscribed diagonals representing the new window, is formed.

3. Click again to fix the size of the new window.

   Your work area zooms to display only the area you just outlined within the rectangle.

   You can also click this icon to use the Zoom by Points command:

4. Select the **View > Zoom World** menu item.

   This command fits the entire extents of the drawing to your work area. There is no icon for this zoom option.

5. Select the **View > Zoom Fit** menu item. This command fits the layout to the work area.

   You can also click this icon to use the Zoom Fit command:

6. Select the **View > Zoom In** menu item.

   The view in the work area zooms in.

   You can also click this icon to use the Zoom In command:

7. Select the **View > Zoom Out** menu item.

The view in the work area zooms out.

You can also click this icon to use the Zoom Out command:

Using the Middle Mouse Button to Zoom In and Out

The middle mouse button can also be used to zoom in and out of your display.

1. Place the cursor in the bottom right portion of the work area. Press but do NOT hold the middle mouse button in the work area.

Note

If you have a two-button mouse, you can press the SHIFT key while you select with the right mouse button.

2. Move your cursor towards the top left portion of the work area.

Notice as you move your cursor that a rectangle is drawn. This represents what will be the new display area.

3. Select again with the middle mouse button (or the left mouse button).

The area that was contained within the white rectangle now becomes your new display area.

4. Select again with the middle mouse button somewhere towards the middle of the display area. Remember not to hold down the middle mouse button.

5. Move your cursor SLOWLY towards the bottom right.

As you move your cursor, two white rectangles are drawn. The inside rectangle represents the original display area. The outside rectangle represents a zoom out magnification. The further the outside rectangle is away from the inside rectangle, the greater the zoom out. As you move your mouse, you will see your work area temporarily redisplay. This temporary redisplay represents what will be the new work area.

6. Select again with the middle mouse button (or the left mouse button).

Your work area is redrawn to match the current zoom.

Using the World View Window

In the lower part of the Control Panel is the World View window. It displays a board outline, as shown in the figure. The white rectangle defines your view relative to the board outline.
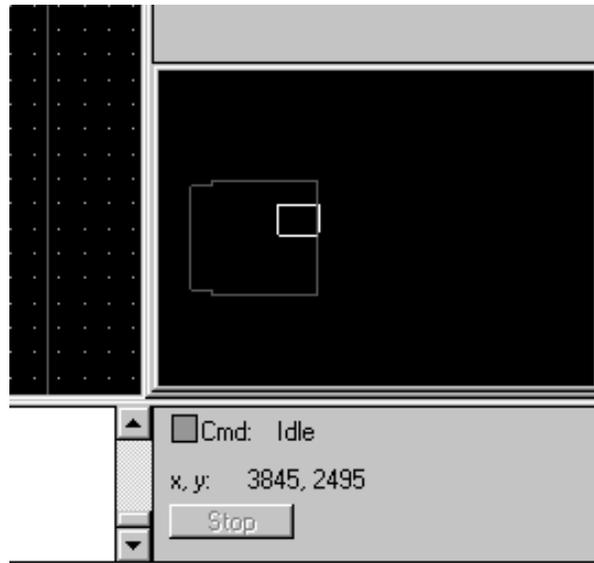
To see how the World View window works, perform the following commands in this window:

1. Place your cursor into the World View window and click left.

This "initializes" the World View window.

2. Right click in the World View window.

A pop-up menu appears.

3. Choose the **Resize Display** option.

The Allegro message in the Console window prompts you to click in the World View window to enter the first point of a rectangle (similar to the Zoom By Points command).

4. Left click in the World View window.

As you move your cursor, a white rectangle representing a new window forms.

5. Click again to complete the sizing of the outline for a new window.

The work area zooms to display just the area within the white rectangle you specified.

6. Repeat the **Resize Display** command and create a small rectangle within the board outline.

The work area zooms to display that portion of the design you have outlined.

Note

If you have a three-button mouse, there is a quicker way to resize the white rectangle in the World View window. Place your cursor in the World View window, and click and hold the left mouse button. As you move your cursor, a white rectangle representing the new window is formed. Release the left mouse button to designate the size of the new window.

7. Right click in the World View window, and select the **Move Display** option from the pop-up menu.

   The Allegro message area prompts you to pick in the World View window to reposition the white rectangle, currently attached to your cursor.

8. Click in the World View window to reposition the white rectangle somewhere else on the design.

   The work area zooms to display just the area within the white rectangle that you have specified.

Note

If you have a three-button mouse, there is a quicker way to move the white rectangle in the World View window. Place your cursor in the World View window, and click and hold the middle mouse button. The white rectangle snaps to your cursor location, and the content of the work area changes accordingly when you release the middle mouse button.

9. Using the middle mouse button (or SHIFT+LMB), drag the white rectangle to a new location, then release the middle mouse button.

   The work area zooms to display that portion of the design you specified.

Using Strokes

Allegro allows you to use *strokes*, or specific cursor movements, to perform common commands. You can try these strokes on your own now:

1. Place your cursor in the work area, then press (and hold) the CTRL key on the keyboard while you press (and hold) the right mouse button. This action is indicated like this: CTRL+RMB.

2. Draw the letter **W** with the cursor.

This **W** stroke has been aliased to a command that zooms to fit the entire layout drawing on the screen.

3. Use the same CTRL+RMB keystroke combination to draw the letter **Z** across an area of the board.

This **Z** stroke has been aliased to a command that zooms in to an area of the design. The extents of the zoom area are defined by the diagonal line connecting the upper left tip to the lower right tip of the **Z**.

Customizing Your View and Toolset

1. From the top menu bar, choose **View > Customization > Display**.

The Display Option dialog box appears.
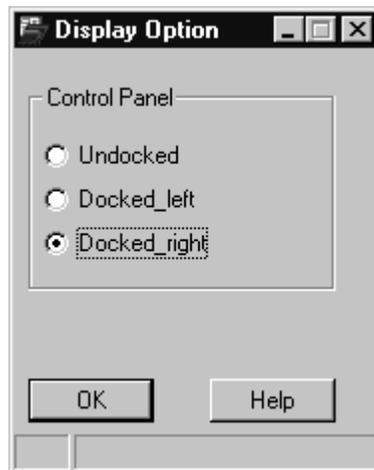
2. Experiment with the docking options that determine where the Control panel appears, then click **OK** to close this dialog box.

3. Select the **View > Customization > Toolbar** menu item.

The Customize dialog box appears. Experiment by turning the various toolbars on and off.
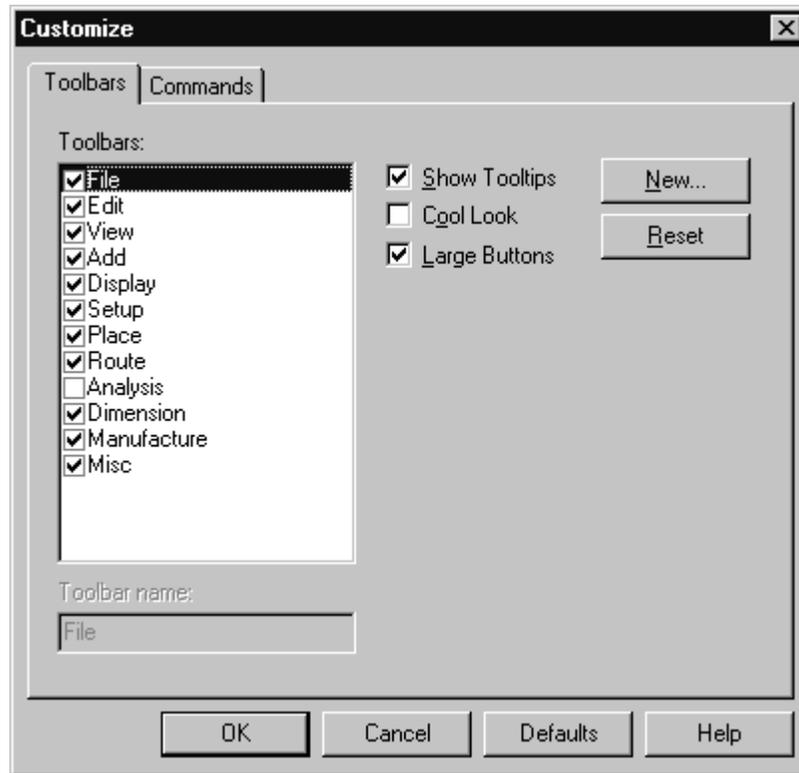
4. Click the **Commands** tab to bring it forward.

5. Click the **Route** category to display available route-related icons, as shown in the following figure:

Allegro Layout System   May 27, 2002
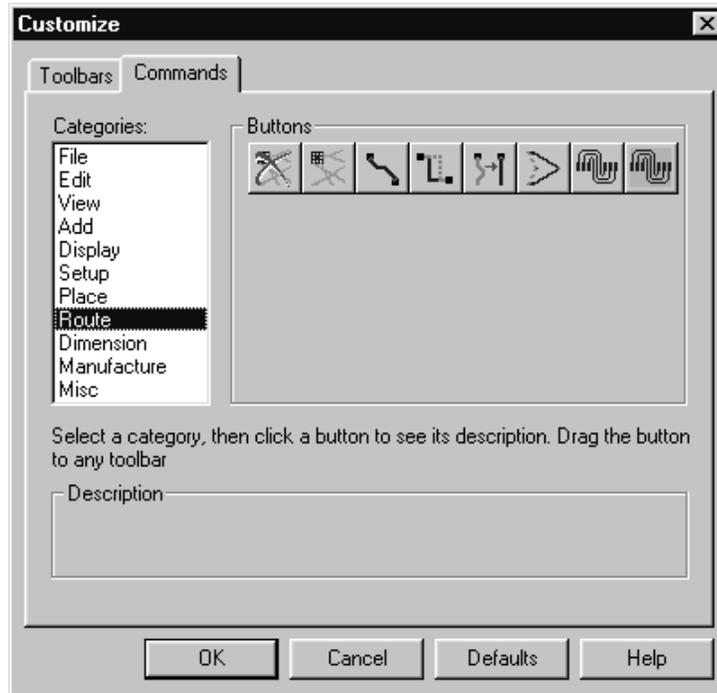
Notice that there are two SPECCTRA router-related icons. The last icon does not appear in your Allegro Editor window.

■   The first SPECCTRA icon will open the SPECCTRA autoroute parameter form, which allows you to use the SPECCTRA autorouter without having to leave the Allegro Editor.

■   The second SPECCTRA icon opens the SPECCTRA GUI.

6.   Add the second SPECCTRA icon by clicking and dragging the icon from the Commands tab to the toolbar area of the Allegro window. Place it next to the current SPECCTRA icon.

7.   Click **OK** to close the Customize dialog box.

8.   Reset the options in the Display Option dialog box and the Customize dialog box to their defaults.

Note

For purposes of this class, it is important to have your Allegro work match the figures shown in the labs.

Choosing Drawing Options

1.   Zoom into the area around the **U7** component in the upper left part of the board, and view the pads.

2.   Choose **Setup > Drawing Options** from the top menu.

The Drawing Options dialog box appears. Notice the five tabs near the top of this dialog box.

3. Click the **Display** tab to bring it forward.

4. Enable the **Grid**, **Filled Pads** and **Display drill holes** options, as shown in the figure, then click **OK**.
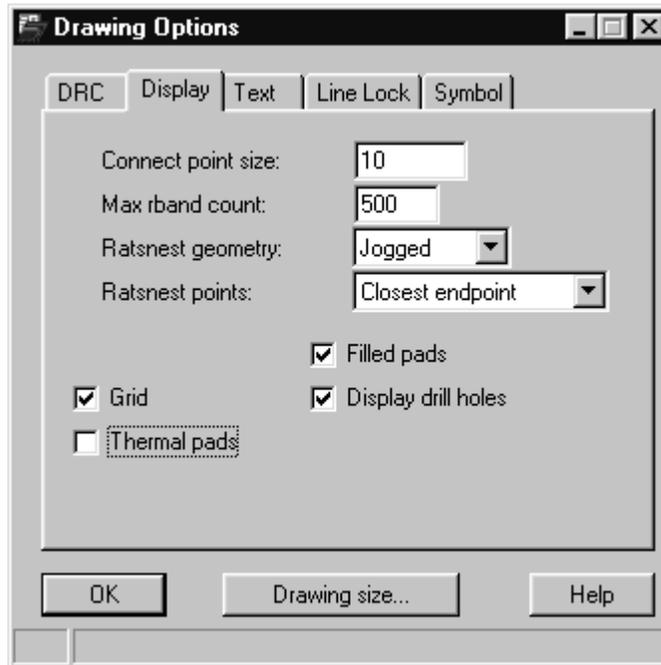
The drawing now shows the U7 pin pads filled in, grid points, and the drill holes.

5. After viewing the changes on the U7 component, reset the Display options in the Drawing Options dialog box to their previous disabled (unchecked) states and click **OK**.

Changing the Cursor Display with User Preferences

1. Choose the **Setup > User Preferences** menu item.

    The User Preferences Editor displays.

2. Select the **UI** folder in the Categories box.

3. Next to the pcb_cursor preference option, click the drop-down list and select **Infinite**.

    Notice the Summary Description area states that this variable is used to change or set the cursor type, and the Effective field states that this change will take effect immediately.

4. Click **OK** to save the change and close the dialog box.

Notice the cursor has changed to a cross-hair and now spans the height and width of your window.

5. Reverse your choices to change the cursor back to a cross.

🛑 **End of Lab**

2

Lesson 2: Managing the Allegro Work Environment

Learning Objectives

- Control the color and visibility of objects.
- Create and use scripts.
- Apply the Find Filter (in the Control Panel) to select objects.
- Locate board database objects and report information about them.

Summary

In this section you will be introduced to the Allegro PCB Layout System. You will explore the Allegro graphical user interface and explore the various programs that comprise the Allegro PCB Layout System. You will also view Allegro classes and subclasses, work with setting colors and visibility of objects, and learn how to use the **Display > Element** command to query design objects.

Groups, Classes and Subclasses

GROUPS	CLASSES	SUBCLASSES
Geometry	Board Geometry	OUTLINE, PLATING_BAR, ASSEMBLY_NOTES, TOOLING_CORNERS, DIMENSION, PLACE_GRID_TOP, PLACE_GRID_ BOTTOM, TOP_ROOM, BOTTOM_ROOM, BOTH_ROOMS, SWITCH_AREA_TOP, SWITCH_AREA_ BOTTOM, SILKSCREEN_TOP, SILKSCREEN_BOTTOM, ASSEMBLY_DETAIL, SOLDERMASK_TOP, SOLDERMASK_BOTTOM, OFF_GRID_AREA, CONSTRAINT_AREA
	Package Geometry	ASSEMBLY_TOP, ASSEMBLY_ BOTTOM, PLACE_BOUND_TOP, PLACE_ BOUND _ BOTTOM, PIN_NUMBER, PAD_STACK_NAME, SILKSCREEN_TOP, SILKSCREEN_BOTTOM, BODY_CENTER, SOLDERMASK_TOP, SOLDERMASK_BOTTOM, DISPLAY_TOP, DISPLAY_ BOTTOM
Manufacturing	Manufacturing	PHOTOPLOT_OUTLINE, NO_GLOSS_ALL, NO_GLOSS_TOP, NO_GLOSS_BOTTOM, NO_GLOSS_INTERNAL, NCDRILL_LEGEND, NCDRILL_FIGURE, PROBE_TOP, PROBE_BOTTOM, AUTOSILK_TOP, AUTOSILK_ BOTTOM, NO_PROBE_TOP, NO_PROBE_BOTTOM
	Drawing Format	OUTLINE, TITLE_BLOCK, TITLE_DATA, REVISION_BLOCK, REVISION_DATA

Summary

A design file is a composite of a number of drawing layers. The drawing elements of each of these layers can be selectively colored and turned on or off as visible or invisible layers.

Allegro organizes drawing layers into a hierarchy of groups, classes and subclasses. Each layer has its own color and visibility settings. Groups are classes that have been combined together to aid you in controlling the color and visibility.

More Groups, Classes and Subclasses

GROUPS	CLASSES	SUBCLASSES
Stack-up	Pin Via DRC Etch Anti-Etch	TOP, BOTTOM, SOLDERMASK_TOP, SOLDERMASK_BOTTOM, PASTEMASK_TOP, PASTEMASK_BOTTOM, FILMMASKTOP, FILMMASKBOTTOM, THROUGH_ALL, PACKAGE_TOP, PACKAGE_BOTTOM
Components	Comp Value Dev Type Ref Des Tolerance User Part	ASSEMBLY_TOP, ASSEMBLY_BOTTOM, SILKSCREEN_TOP, SILKSCREEN_BOTTOM, DISPLAY_TOP, DISPLAY_BOTTOM
Areas	Route KO Via KO Package KO Package KI Route KI	TOP, BOTTOM, THROUGH ALL
Display	Grids Ratsnests Temp Highlight Perm Highlight Background	*Subclasses not applicable*

More Information

All graphical items are stored in what is basically a two-level database scheme. The top level is called a class. There are 20 classes defined inside the Allegro database. You cannot delete or add classes.

Under each class there are many subclasses. These subclasses are the second level of the database. Subclasses are often referred to as layers in the design. You cannot delete predefined subclasses, although you can add and delete your own user-defined subclasses. For example, when you want to create the outline for your printed circuit board, you draw it on a class called Board Geometry, with a subclass called Outline.

All of the board routing will appear on the subclasses under the class called Etch. You need to create a subclass for each layer of the printed circuit board. Thus, if you have a six-layer printed circuit board, you need to have six subclasses under the class called Etch.

Note that under the Etch class there is a subclass called Top and a subclass called Bottom. These names cannot be changed, nor can these two subclasses ever be deleted.

Options Window of the Control Panel

| Edit > Change	Route > Connect	Add > Text
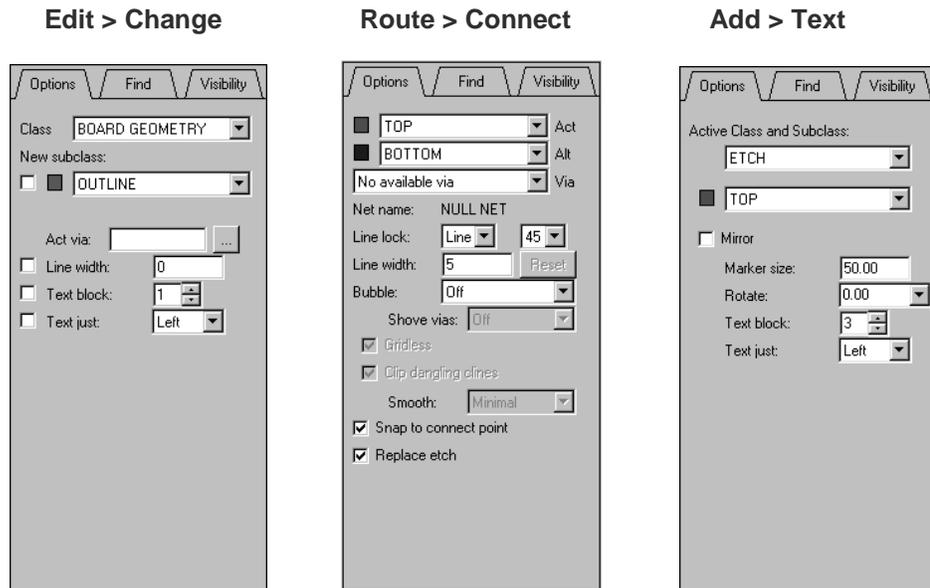
Summary

The Options folder tab of the Control Panel contains parameters that are used to control the current interactive command. You will notice that the parameters change from command to command.

The parameters and values you set in the Options window take effect immediately. They override definitions for the same parameters and values that may exist elsewhere in the Allegro software. For example, in the **Add > Text** command, the Allegro tool looks to the Drawing Options dialog box, which was set using the **Setup > Drawing Options** command for the rotation and text values. If you place a different value in the Options window, however, the tool ignores the information in the Drawing Options dialog box.

Controlling Color and Visibility
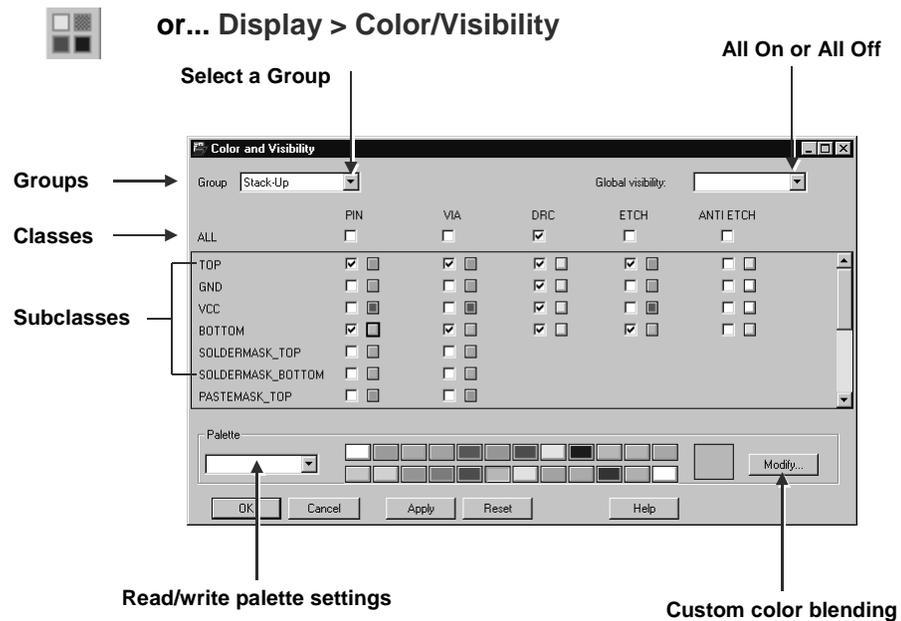

More Information

You display the Color Visibility dialog box by selecting the **Display > Color/Visibility** option from the top menu or by selecting the **Color** icon. You use this form to turn on or off the visibility for layers, as well as to set colors for layers.

To turn on or off the visibility of a specific subclass, you simply click the box to the left of the subclass. A check in this box indicates that the subclass is currently visible. If there is no check in that box, that subclass is currently invisible. To change the color of a subclass, first you select the desired color from the bottom portion of the Palette dialog box, and then you select the color icon to the right of the desired subclass.

At the top right of this dialog box you see the Global Visibility pull-down menu. With this menu you can make all subclasses visible or invisible in the design at one time. Remember that in order to turn a subclass off or on, you must first select the appropriate group in the top left pull-down menu labeled Group.

Information about colors assigned to individual layers, and which layers are visible and invisible, are all stored in the Allegro database. There is no ASCII file that is used to store the color information.

Controlling Etch Visibility

Include Plane Layers

Color View

Conductor layer controls

Plane layer controls

Individual layer controls

Individual element control
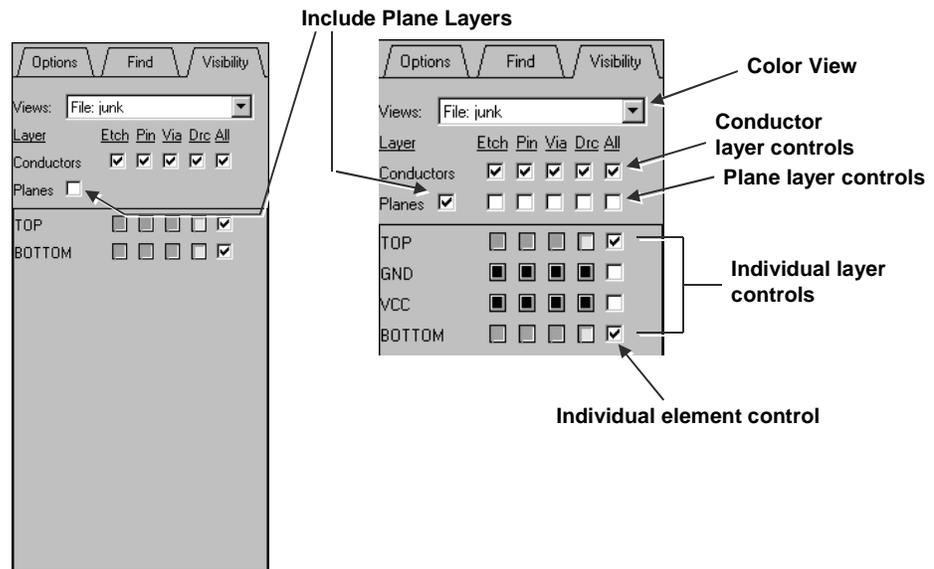
More Information

The Control Panel Visibility tab is a quick way to turn on or off layers or elements contained in a design. You can separately control the etch routing layers from the plane layers, as well as Etch, Pins, Vias and DRCS.

Conductor Controls

The Conductor check boxes let you individually turn on or off all etch, pin, via or DRCs for all layers defined as conductor. By selecting the All check box, you can turn on and off all etch, pins, vias and DRCs for all conductor layers.

Plane Controls

The Planes check boxes let you individually turn on or off all etch, pin, via or DRCs for all layers defined as plane. By selecting the All check box, you can turn on or off all etch, pins, vias or DRCs for all plane layers. If you check the Include Planes Box, you will see all the plane layers listed in this visibility form.

Individual Layer Control

By selecting the check box under the All column in the individual layer row, you can turn on or off all etch, pins, vias or DRCs for that layer.

Individual Element Control

You can turn on or off a single element (etch, pin, and so forth) by selecting the element.

Graphics Dimming or Shadow Mode
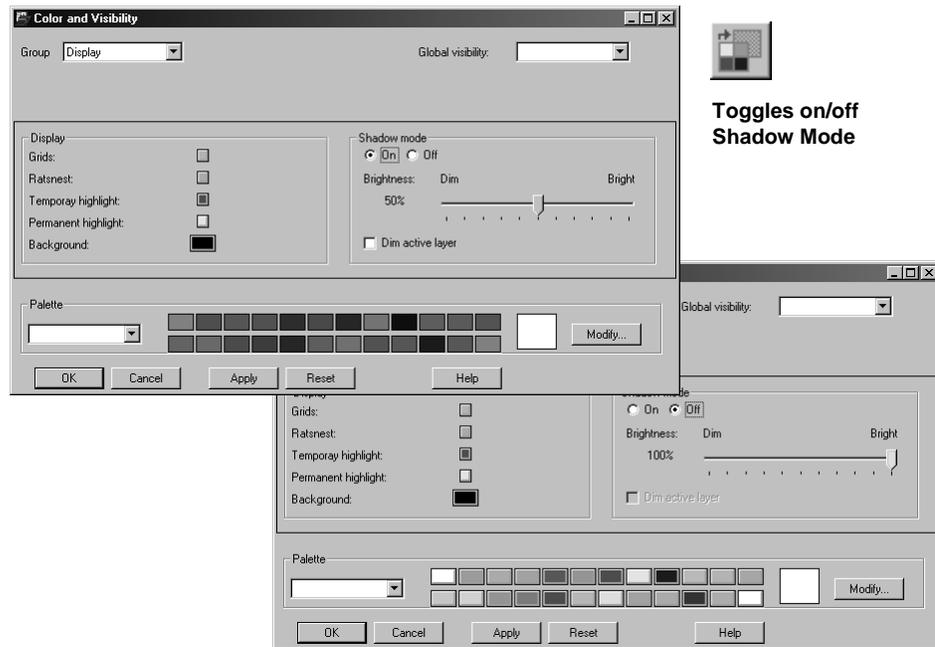
**Toggles on/off
Shadow Mode**

More Information

The Graphics Dimming or Shadow Mode option gives you the ability to provide distinct levels of visibility that are based on the importance of the object. The main control for shadowing is located in the Color and Visibility window under the Display group. With Shadow Mode turned on, the brightness slide bar controls the color intensity of the non-important objects. The higher the brightness percentage, the less difference in color between the important and the non-important objects. While you are using the brightness slide bar, the color palette boxes will reflect the shadow version of each color. You use the **Shadow Toggle** icon to turn on and turn off the shadowing feature.

Objects of importance are defined as follows:

- Items that have been highlighted using the highlight command

- Items that are highlighted by the current active command

- The current Active layer as defined in the Options Folder tab

The default is to have Shadow Mode disabled. When Shadow Mode is first enabled, the default brightness is 40 percent.

Scripts

Step 1 -Start the Script
File > Script
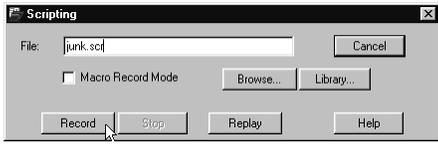
Resulting Script

Step 2 - Execute the commands
View > Zoom By Points

```
Pick 1st Corner Of New Window.
last pick: 101.7, 96.2
Pick To Complete Window.
last pick: 503.0, 389.3
Command >
```
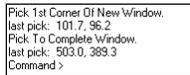
Step 3 - Stop the Script
File > Script

```
# Allegro script
#        file: junk.scr
#        start time: Tue Mar 27 16:27:24 2001
version 14.0

setwindow pcb

zoom points
pick 101.7 96.2
pick 503.0 389.3

#        stop time: Tue Mar 27 16:28:14 2001
```
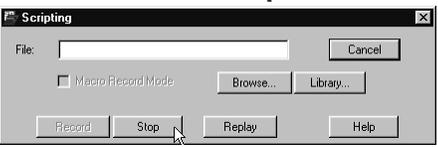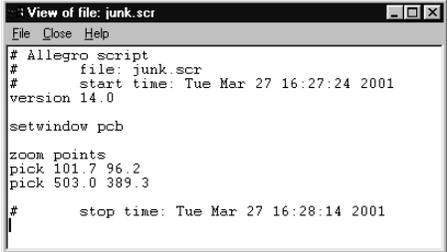
More Information

With scripts, you can have the Allegro Editor save all your menu selections and mouse picks in a text file. You initiate such script recording by clicking **Record**. Allegro will save all your commands in a text file until you stop the recording. You can then replay the file in the same design or a different design to quickly replay and execute repetitive operations.

Macros are like scripts in that they let you perform repetitive actions, such as complex geometric operations, on a drawing. The difference, however, is that scripts record from absolute coordinates while macros record from relative coordinate positions in a drawing. To start recording a macro, you enable the Macro Record Mode check box.

Lab

◆ Lab: Script Files and Controlling Visibility and Color
  - Defining groups, classes and subclasses
  - Starting a script file recorder
  - Controlling visibility
  - Setting colors
  - Stopping the script file recorder
  - Testing the script file (*colors.scr*)

More Information

The following lab will familiarize you with the Allegro database structure of Groups, Classes and Subclasses, and teach you how to use the script recording feature, as well as how to control setting colors and visibility.

Lab 2-1:   Script Files and Controlling Visibility and Color

Objective: Learn how to use a script file to control color and visibility of graphical elements.

In this lab, you will change the default visibility and color assignments on each new layer to suit your personal preferences. Changing layer visibility and assigning colors is a procedure you will want to use over and over again. You can use script files to capture repetitive procedures. From the time you enter *recording* mode until the time you stop the recorder, all your activities are captured into the script file.

Starting a Script File Recorder

1. Select **File > Script** from the top menu.

   The Scripting dialog box appears.

2. Place the cursor in the File text field and type the following:

   colors

Note

DO NOT press the ENTER key.
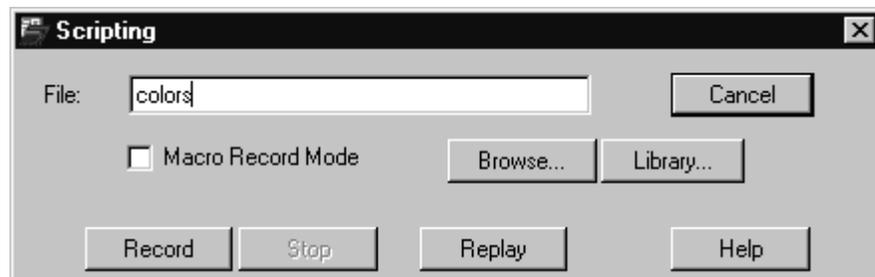
3. Click **Record**.

   The Scripting dialog box disappears and you are ready to begin recording. Everything you do from this point forward will be entered into the script file *colors.scr*. You will be instructed later when to stop the recording.

Controlling Visibility

First you can set the visibility and color assignments for the design.

1. Click the **Color** icon.

   The Color and Visibility dialog box appears.

2. Near the top right of the Color and Visibility dialog box, click on the **Global Visibility** drop-down list and select **All Invisible**.

3. When an alert message appears asking if you want to change all classes to invisible, click **Yes**.

This action resets all the colors to OFF, so you can begin setting them to whichever colors you like.

**4.** In the Group drop-down list, select **Components**, as shown.

5. Under the REF DES class name, enable the visibility box for the subclass ASSEMBLY_TOP. A check mark in the box indicates the subclass is turned ON.

6. Select **Geometry** from the Group drop-down list.

The Geometry groups are named BOARD GEOMETRY and PACKAGE GEOMETRY.

7. Under the BOARD GEOMETRY group enable the visibility for the **OUTLINE** subclass.

8. Under the PACKAGE GEOMETRY group, enable the visibility for **ASSEMBLY_TOP**.

9. Select **Stack-Up** from the Group drop-down list.

10. Enable visibility for subclasses in this group, as shown in the figure, then click **Apply**.

We will use the Palette drop-down list in the next section.
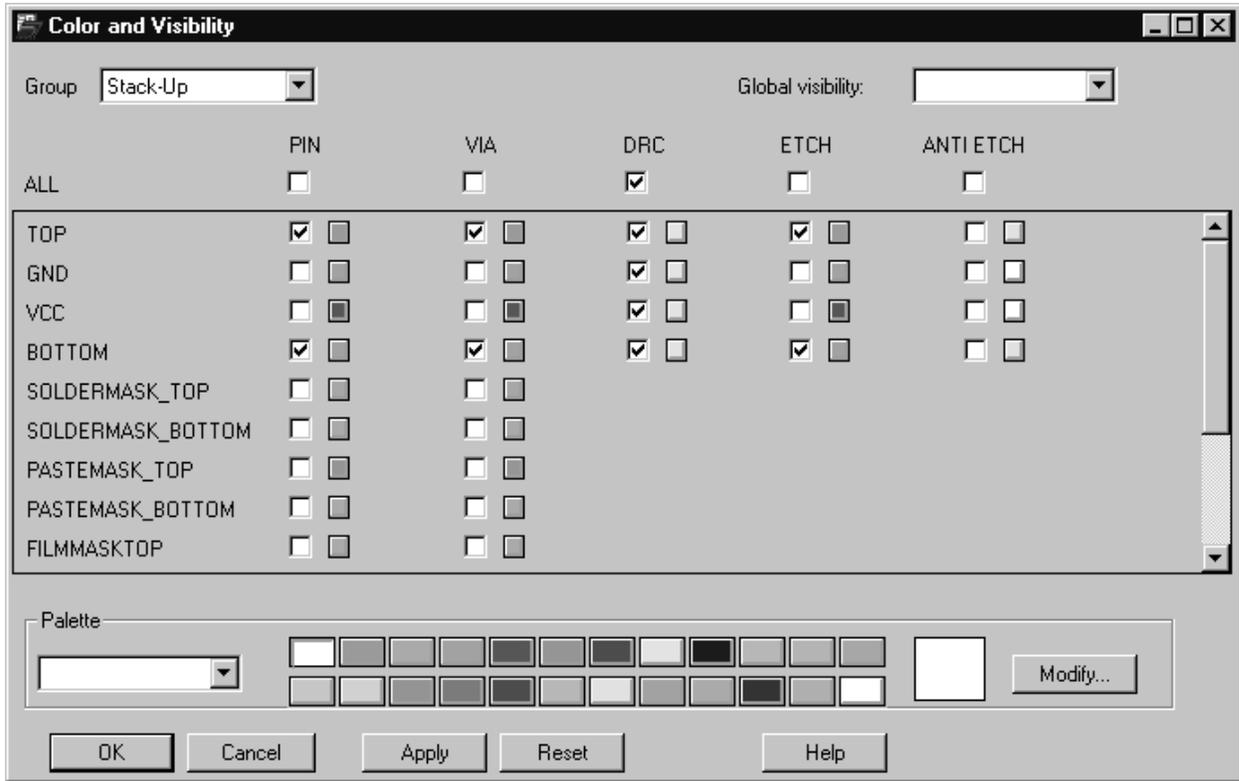
Controlling Colors

To change the colors of some of the subclasses in the Stack-Up group, follow these steps.

1. Click a color button in the **Palette** section of the Color and Visibility form, then select the subclass color button next to **Bottom** for ETCH, PIN and VIA.
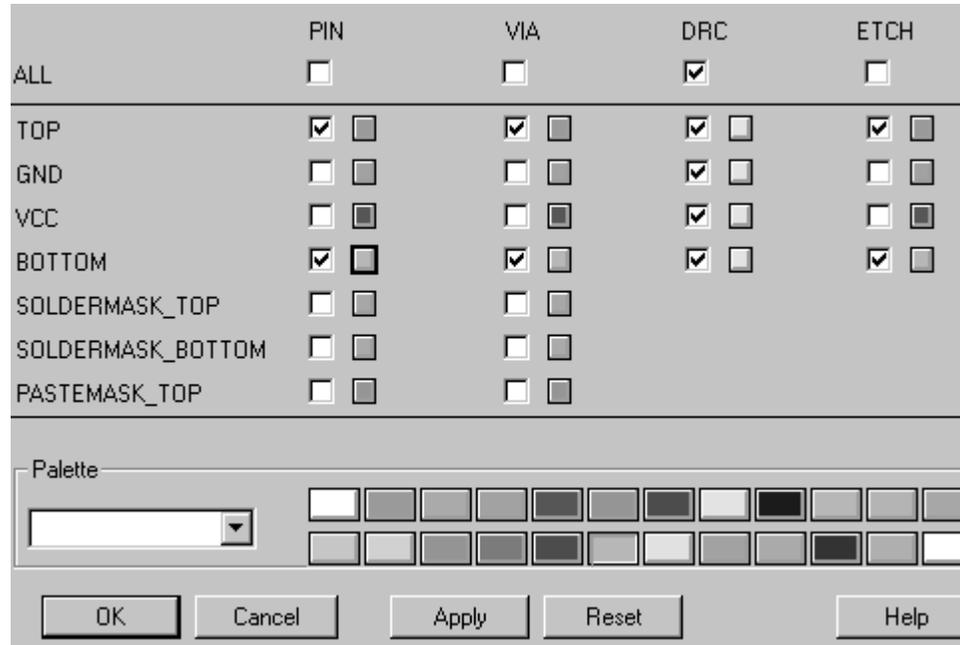
2. Click **OK** to apply and close the Color and Visibility menu.

Stopping the Script File Recorder

Notice the word *Recording* in the Status window (lower right corner of the work area window). You are still in record mode.

1. Select **File >Script** from the top menu.

The Scripting dialog box appears.

2. Click **Stop** to stop the script file from recording.

All the visibility and color assignments you made have been captured in the *colors.scr* file.

3. Click **Cancel** to close the Scripting dialog box.

4. View the *colors.scr* ASCII file by selecting **File > File Viewer**. The file should be located in your *play* working directory. Be sure to change the file type in the browser menu from *(*.log)* to *All Files (*.*)* so your *colors.scr* file will display.

5. Close the *colors.scr* file when you're done viewing it.

Testing the Script File (colors.scr)

1. Click the **Color** icon.

The Color and Visibility dialog box appears.

2. Near the top right of the form in the Global Visibility drop-down list, select **All Invisible**.

3. When a warning appears asking if you want to change all classes to invisible, click **Yes**.

4. Click **OK** to close the Color and Visibility dialog box.

    Because the visibility for all classes is turned off, nothing is displayed in the work area.

5. At the Allegro command line, enter the following:

    replay colors

    This command replays the script file you created, and sets the visibility and color assignments automatically.

Use the Shadow Mode Option

1. Click the **Color** icon.

    The Color and Visibility dialog box appears.

2. In the Group drop-down list, select **Display**.

3. Select **On** for the Shadow Mode option.

4. Select and drag the Brightness slide bar.

    Notice as you move the slide bar in either direction, the colors in the color palette change, giving you the opportunity to see how the changes will actually appear.

5. Click **OK** to apply and close the Color and Visibility menu.

    Notice how the color of the current Active Class and Subclass as defined in the Options folder tab is displayed at the normal color, while all others are drawn at the dimmed color.

6. Change the Active Class in the Options folder tab to **Board Geometry** and the Active Subclass to **Outline**.

    Notice now that the board outline is drawn at the normal color and everything else is displayed at the dimmed color. Select the Shadow Mode toggle icon to turn off shadow mode.


 End of Lab

The Selectable Objects List

◆ You use the Design Object Find Filter section of the Find folder tab is used when selecting data base elements with the mouse.

◆ The "list" is searched, starting from the top left (Groups) and proceeding to bottom right (Rat Ts)

◆ The first "type" that is found with a check will be used for the selection.

Challenge: Given the settings to the right, when the Delete command is executed, what will be selected for deletion in the following two scenarios (note the cursor location)?
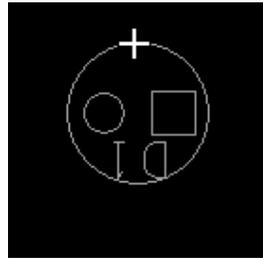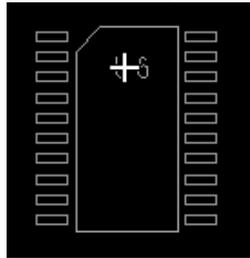
Summary

The Find tab is more commonly referred to as the Find Filter. This is one of the more important forms used in Allegro. It is critical that you pay attention to and understand the settings.

The top section of this form contains the Design Object Find Filter box. This section determines what types of objects in the design are to be acted upon when you select elements with the mouse.

When more than one item is checked, the system prioritizes selection by going from left to right and top to bottom and finding the first checked item. In *both* instances of the examples shown, the entire part would be deleted. This is because the Symbols item would be the first check box found in the Find Filter.

using the All On and All Off buttons are quick ways to turn on or off all the items in the Design Object Find Filter box.

Using the Find by Name Section

Use the Find by Name section of the Find Folder tab to:

- Highlight a net name.
- Locate a part placed in the design by its ref. des.

1 Use the pull-down field to set which type of a name you will enter.

2a Enter the name in the blank (**>**) field.

2b Use the **More** button to display a scrollable list of all elements matching the desired "type."

NOTE: The check boxes selected in the Design Object Find Filter have no affect when using the Find by Name section, with the exception of the **Property** pull-down field.
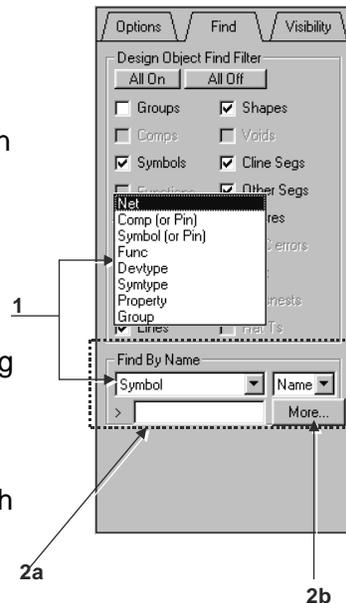
Summary

The bottom section of the Find Filter contains the Find by Name box. You use the Find by Name section to select elements by a name rather than graphically.

For example, if you wanted to highlight the net called GND, you would execute the **Highlight** command, go down to the Find by Name section, click the down arrow and select Net. Then in the blank field immediately below the Net pull-down field, enter GND, and press ENTER. The net named GND would then be highlighted.

The More button in the lower right corner of the Find by Name section opens a scrolling window that lets you choose from a list of all available net names, component names, properties, and so forth. It should be noted that when you use the Find by Name section, the check boxes in the Design Object Find Filter section are ignored, unless the Property pull-down option is used.

Using Find by Property
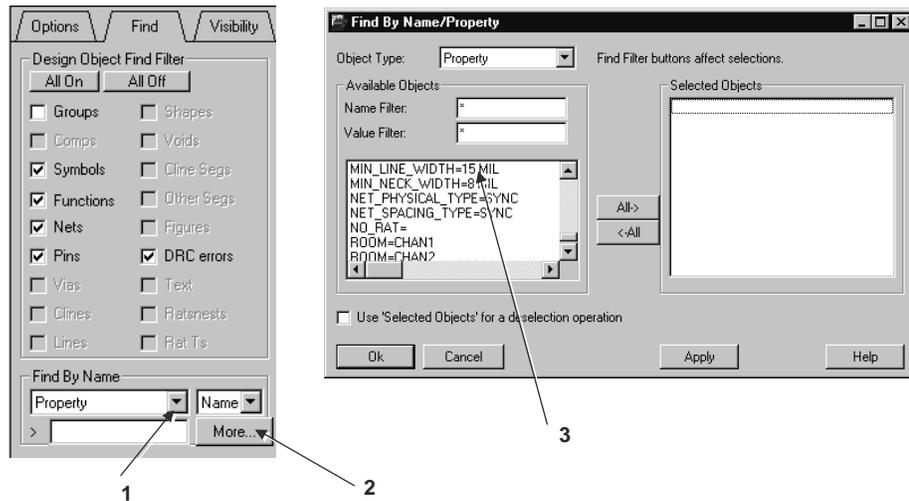
Use the Find by Property option to select database elements with a common property such as "FIXED", "MIN_LINE_WIDTH", and so forth.

More Information

As previously noted, the Property option under the Find by Name box uses the Design Object Find Filter section. When you select the Property option and click the More button, all properties are gathered that are attached to the checked items. A scroll list is generated specifying all the unique properties that were found.

Remember that the Find Filter is only accessible *after* a command has been issued, such as **Highlight**, **Delete**, **Move** and so forth.

Highlighting Elements

Display > Highlight

…or

Common sequence for highlighting elements with the mouse is:

1   Start the command.

2   Activate the Find Folder tab.

3   Click the **All Off** button.

4   Toggle on desired elements.

5   Select the elements in the design window to highlight.
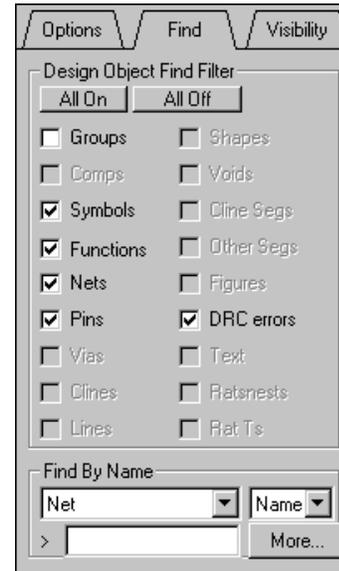
More Information

The Highlight command is used to display a database element in a certain color. The type of database element highlighted is based upon the Find Filter.

You have a choice of 24 different colors to choose from in the Options Folder tab. Once highlighted, the elements remain highlighted until they are dehighlighted using the **Dehighlight** command.

Lab

◆ Lab: Highlighting and using the Find Filter
   ■ Using the Selectable Objects list
   ■ Using the Find By Name section
   ■ Finding items by property
   ■ Highlighting objects in a design

More Information

The following lab will teach you how to select elements in the Allegro database by graphically selecting items, selecting items by their names, and selecting items by their properties. You will also learn how to use the **Highlight** and **DeHighlight** commands.

Lab 2-2:   Highlighting and Using the Find Filter

Objective: Learn how to use the Find Filter as a selection aid and how to highlight items.

Using the Selectable Objects List

In this lab, you will use the Selectable Objects list to select a particular type of object with the left mouse button. You can toggle different objects either ON or OFF to prevent inadvertently selecting something you don't want to edit.

1. Zoom in on component **U3** (the middle IC on the left side of the design).

2. Click the **Find** tab in the control panel to bring the Find Filter to the front of the display.

3. Select **Edit > Move** from the top menu bar.

4. In the Find Filter, click **All On**.

   This ensures that check boxes of all appropriate objects are toggled on, as shown in the figure.
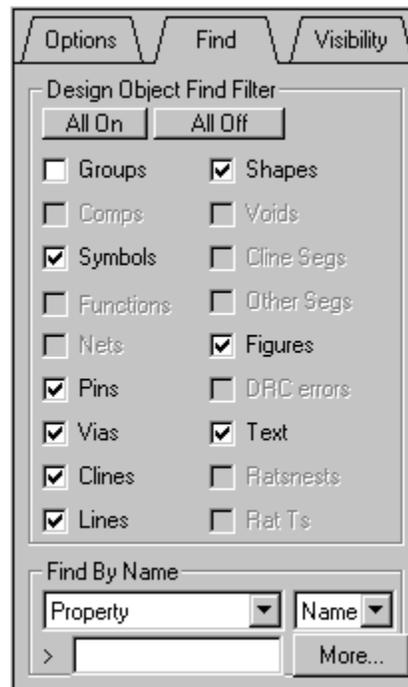
5. Click on the reference designator (text characters) **U3**.

Part U3 snaps to your cursor. In the selectable objects section of the Find Filter, Symbols is checked, or toggled ON. The reference designator you selected is seen as *part of* the package symbol. Because Symbols is higher in the selection hierarchy than the reference designator Text, Allegro selects the item at the higher level.

6. With the cursor in the work area, right click.

   A pop-up menu appears with options for the active, **Move** command.

7. Select **Oops** from the pop-up menu.

   Part U3 snaps back to its original location.

8. In the Find Filter, click **All Off**, then enable the **Text** check box.

   All items in the Find Filter should be unchecked except for Text.

9. Select the reference designator text for **U3** again.

   This time, part U3 does not snap to the cursor. Instead, only the reference designator text snaps to the cursor.

   Because of the change you made in selectable objects, the reference designator you selected is treated as a text object and the symbol is not selected.

10. Right click and choose **Cancel** from the pop-up menu.

    Text U3 snaps back to its original location.

Using the Find By Name Section

The Find By Name section contains a data entry field and two field description boxes. Here's how to use these options.

1. Perform a **Zoom Fit** command, then choose **Edit > Move** from the top menu.

2. If needed, change the setting in the Find By Name field to **Symbol (or Pin)** as shown, and enter **U7** in the **>** field.

3. Hit the **Enter** or **Return** key.

Part U7 snaps to your cursor and the display is redrawn to be zoomed around this part. Whatever you enter in the Find By Name field is selected for manipulation by the active command—in this case, Move.

4. Right click and choose **Cancel** from the pop-up menu.

Part U7 snaps back to its original location as you exit the active command.

Finding Items by Property

You can find objects by specifying the properties attached to them. To do so, you use the Property field under the Find By Name box in conjunction with the **Highlight** command.

When you click the More button, the Properties dialog box displays a list of properties to help you select the object you want to edit or act upon. This list of properties is affected by the button settings in the selectable objects section. To get a complete listing of available properties, you must make sure all the buttons in the selectable objects section are toggled ON.

1. Choose **Display > Highlight** from the top menu bar.

2. Click the **Find** tab in the Control Panel to bring the Find Filter to the front of the display.

3. Under the Find by Name field, select **Property** from the drop-down list if it is not already selected.


4. Click **All On**.

   This ensures that all relevant check boxes are toggled ON, limited to Symbols, Functions, Nets, Pins, and DRC errors.

5. Click **More...** to display a browser menu of properties that exist in your design.

   The Find By Name/Property dialog box appears, as shown in the figure, containing a scrollable list of available properties.
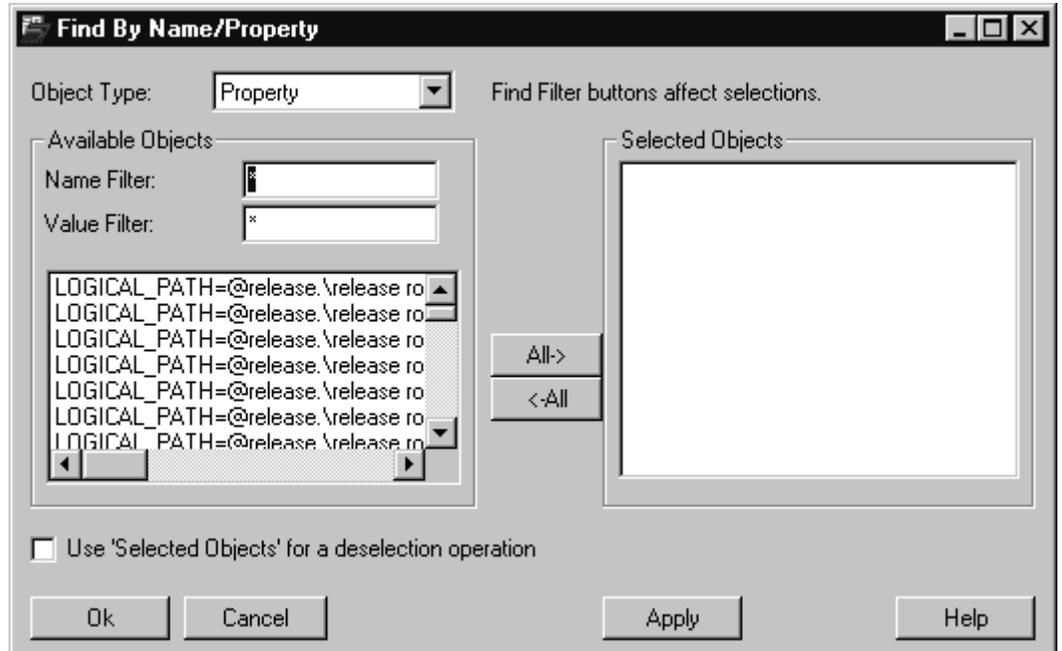
6. Scroll down and select the **MIN_LINE_WIDTH=15** property and click **Apply**.

You have just highlighted your special voltage nets. All nets with an assigned MIN_LINE_WIDTH property of 15 are highlighted in the work area. The nets V12N, GND_EARTH, AGND and V+12 in this design have a MIN_LINE_WIDTH property attached to them.

7. Click **Cancel** to close the Find By Name/Property dialog box.

8. With the cursor in the work area, right click and choose **Cancel** from the pop-up menu.

The **Highlight** command is no longer active.

Highlighting Objects in a Design

In this part of the lab, you will use the **Highlight** command to locate objects you want to highlight.

You can highlight an object whose location is unknown (so you can see where it is placed or how it has been routed). Highlighting is particularly useful on very large, densely populated designs.

1. Zoom in to the area around the **U3** part, located at the left side of the design near the center.

2. Click the **Highlight** icon or choose **Display > Highlight** from the top menu.

3. Click the **Options** tab in the Control Panel to bring the Options to the front of the display.

The Options form changes to display available colors, and the current active permanent highlight color is displayed.
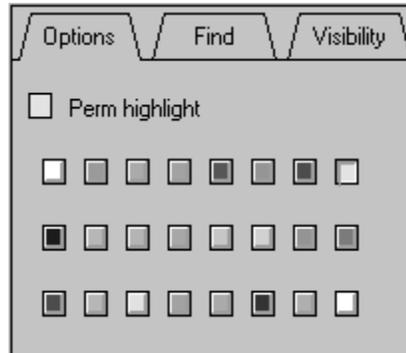
4. Click on the red color button to designate red as the active color for permanent highlighting.

5. Click the **Find** tab to bring the Find Filter menu forward in the Control Panel.

6. Change the setting in the Find by Name field to **Symbol (or Pin)** as shown and type **U3** in the **>** field.

7. Hit the **Enter** or **Return** key.

U3 becomes highlighted. You can also see the highlighted part in the World View window.

8. Click the **Dehighlight** icon or select **Display >Dehighlight** from the top menu.

9. If the Find Filter is covered by the Options form, then click the **Find** tab to bring forward the Find Filter.

10. Enter ***** in the > field under Find by Name in the Find filter.

11. Hit the **Enter** or **Return** key.

You have just removed all the permanent highlights that were in your design.

12. Right click in the Allegro work area and choose **Done** from the pop-up menu.

Note

You can use highlights for objects other than components. Use them for critical nets, pins, properties or anything the Find Filter is capable of finding.

STOP End of Lab

Using the Show Element Command

Display > Element

…or   ⓘ

Common sequence for using
Show Element with the mouse is:

1   Start the command.

2   Activate the Find folder tab.

3   Click the **All Off** button.

4   Toggle on desired elements.

5   Select the elements in the
design window.

```
┌─Options─┐/─Find─\┌─Visibility─┐
│ Design Object Find Filter───────────┐
│   All On    │    All Off    │
│  □ Groups        □ Shapes         │
│  □ Comps         □ Voids          │
│  ☑ Symbols       □ Cline Segs     │
│  ☑ Functions     □ Other Segs     │
│  ☑ Nets          □ Figures        │
│  ☑ Pins          ☑ DRC errors     │
│  □ Vias          □ Text           │
│  □ Clines        □ Ratsnests      │
│  □ Lines         □ Rat Ts         │
│ Find By Name────────────────────┐
│  Net           ▼    Name ▼       │
│  >  [          ]    More...      │
└──────────────────────────────────┘
```
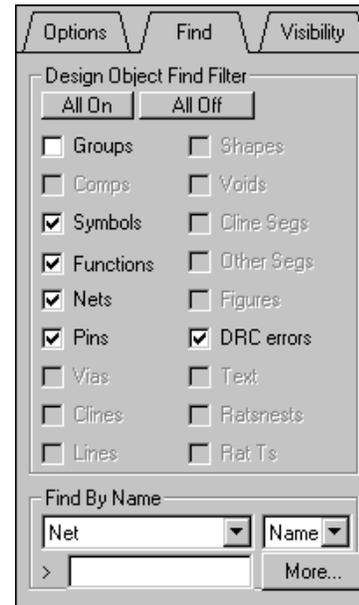
More Information

You can use the **Show Element** command, also referred to as the **Display Element** command, to ascertain information about an item in the design. Remember that the Find Filter is used to determine what type of information will be displayed. Based upon the Find Filter settings, you can determine a net name, a component's reference designator, which padstack a pin uses, and so forth.

Using the Display Measure Command

Display > Measure

```
Measure
File  Close  Help

        SYMBOL PIN U2.1 @ (575.0, 2075.0)
        SYMBOL PIN U2.2 @ (575.0, 1975.0)

Dist = 100.0000.   Total Dist = 100.0000.
Manhattan Dist = 100.0000.   Dx = 0.0000.   Dy = 100.0
Air Gap = 38.0000.   On Subclass:  TOP
```

☐ Nets   ☐ Figures
☑ Pins   ☐ DRC errors
☐ Vias   ☐ Text

Options / Find / Visibility

Active Class and Subclass:

ETCH

☐ TOP
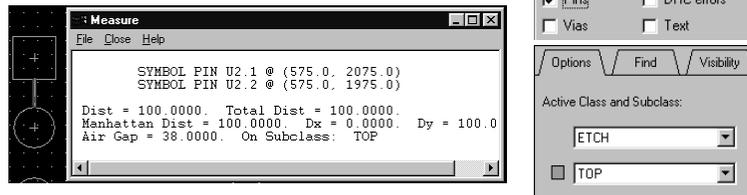
Verify the settings in both the Find Folder tab and the Options Folder tab

Bottom Pin

```
Measure
File  Close  Help

        SYMBOL PIN U2.1 @ (575.0, 2075.0)
        SYMBOL PIN C4.2 @ (635.0, 2200.0)

Dist = 138.6542.   Total Dist = 138.6542.
Manhattan Dist = 185.0000.   Dx = 60.0000.   Dy = 125.0000.
No air gap -- both elements are not defined on  TOP.
Common subclasses for air gap are
BOTTOM
```

☐ Nets   ☐ Figures
☑ Pins   ☐ DRC errors
☐ Vias   ☐ Text

Options / Find / Visibility

Active Class and Subclass:

ETCH

☐ TOP
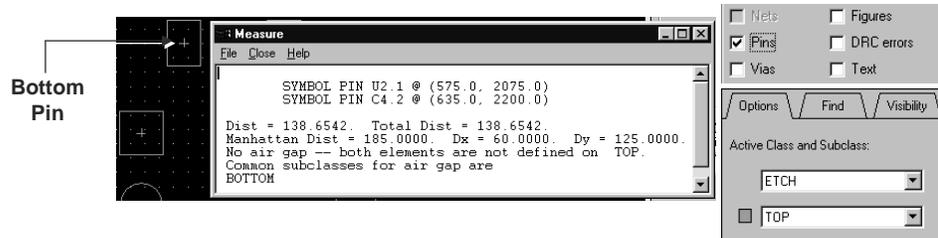
If the class and subcclass settings are incorrect, the **Display Measure** command may not return the desired results.

More Information

You use the **Display > Measure** command to determine the distance between two points. After the two points have been selected, a window is displayed detailing information about the distance between the two elements. Information displayed includes total distance, manhattan distance, the delta X and delta Y, and the air gap. The air gap will only be displayed if the two selected elements reside on the same class and subclass. Again, it is important to remember that the Find Filter settings determine which database elements will be selected by this command. If the selection point contains no items that match the Find Filter settings, then the closest grid point will be used for determining the distance.

Lab

◆ Lab: Using the Find Filter with the Show Element Command

  ■ Using the Find Filter with the **Display > Element** Command

  ■ Using the Find Filter with the **Display > Measure** Command

More Information

The following labs will teach you how to use the **Display > Element** and the **Display > Measure** commands.

Lab 2-3:   Using the Find Filter with the Show Element Command

Objective: Learn how to display information about objects in a design.

The **Show** command displays helpful information about selected objects. You can use this command to evaluate net names, reference designators and pin numbers, line widths, wire lengths, package types, padstack names, measured distances, assigned properties, DRC errors, and more.

Remember, the Find Filter controls what is selected, and therefore the data that is reported to you.

Using the Show > Element Command

1. Zoom in to a view area around the **U2** component, which is a long DIP component located just left of the board center, and to the right of the three SOICs at the left side of the design.

2. Click the **Show Element** icon.

> ### Note
>
> The Show Element command can also be accessed from the **Display > Element** menu or by pressing the **F5** key.

3. Click the **Find** tab in the Control Panel to bring the Find Filter to the front of the display.

4. Click **All On**.

    This ensures that the check boxes for all objects are toggled ON. Only the Group field remains unchecked.

5. Select one of the pins on the U2 component that contains etch connected to the pin.

    The Show Element report appears.

6. If your Show Element report window is covering the Find Filter, move it so you can also see the Find Filter.

    At the top of the Show Element form is a description of the type of object that is selected, <COMPONENT INSTANCE>. The data in this report corresponds to a description of the component instance of the Comps items in the Find Filter because the Comps category is higher in the selection hierarchy than pins or etch.

7. In the Find Filter, disable the check box next to **Comps**.

8. Select the same pin on the same component again.

This time the Show Element form refreshes to display SYMBOL information for this component package.

This report focuses on the characteristics of the physical package symbol, and corresponds to the Symbols entry in the Find Filter. Symbols is now the priority item in the Find Filter. If more than one item in the Find Filter is turned ON, then the priority goes to the highest active item in the list.

9. In the Find Filter, disable **Symbols** and select the same pin again.

The Show Element form refreshes to display FUNCTION INSTANCE information for this package. This information corresponds to the Functions entry in the Find Filter. (The pin you selected is seen as part of a function or gate within this package.)

10. In the Find Filter, disable **Functions** and select the same pin again.

The Show Element form refreshes to display NET information for this pin. This information corresponds to the Nets entry in the Find Filter.

Notice the information about etch length and any attached properties.

11. In the Find Filter, disable **Nets** and select the same pin again.

The Show Element form refreshes to display CONNECT PIN information. This information corresponds to the Pins entry in the Find Filter.

Notice the padstack information.

12. In the Find Filter, disable **Pins** and select the same pin again.

The Show Element form refreshes to display CONNECT LINE information for the connection to the pin. This information corresponds to the Clines (etch) entry in the Find Filter.

13. Right-click in the work area window and choose **Cancel** from the pop-up menu.

Selecting the same object generates different information, depending upon the settings in the Find Filter. It is not just *which* item you select, but also the *selection priority* in the Find Filter that matters.

When choosing the **Display > Element** menu item, disable all the objects in the Find Filter. Then enable only the object(s) that will generate the information you want to see.

Using the Display > Measure Command

1. Click the **Options** tab in the Control Panel to bring the Options form forward.

2. Set the Active Class to **ETCH** and the Subclass to **TOP**, as shown.
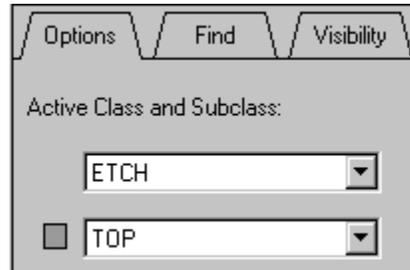
3. Choose **Display > Measure** from the top menu bar.

The Allegro message area prompts you to:

```
Make two picks for calculator by selecting two adjacent
conductor lines.
```

4. Select two objects that you wish to measure the distance between. Remember to check the settings in the Find Filter.

The Measure report appears, showing information about the objects (if any) selected, the manhattan distance, and air gap information. An example of the measure output is shown below. Yours will probably not match this display exactly.


```
    HORIZONTAL LINE SEGMENT @ (2135.00, 3827.00)  (Width = 5.00)
    SYMBOL PIN U15.3 @ (2125.00, 3750.00)

Dist =              77.6466     Total Dist = 77.6466
Manhattan Dist =  87.0000     Dx = 10.0000  Dy = 77.0000
Air Gap =           34.5000   On Subclass:   TOP
```
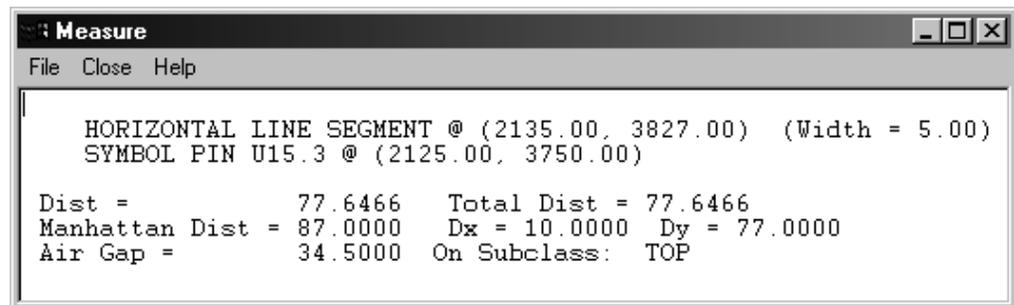
5. To exit from the **Display > Measure** command, right click and choose **Done** from the pop-up menu.

6. Choose the **File > Exit** menu item.

An Exit window appears, asking if you want to save any of the changes made to your current design.

7. Click **No**.

The Allegro window closes.

🛑 **End of Lab**

Lesson 3:   Padstacks

Learning Objectives

◆ Create a flash symbol used for thermal reliefs.

◆ Use the Padstack Designer (or Padstack Editor) to create padstacks for a number of typical pins and device types:

Create a padstack for a through-hole pin.

Create a padstack for pin 1 of a through-hole pin.

Create a padstack for a surface-mounted device.

Summary

In this section you will create Allegro padstacks that will be used to model pins in Allegro footprint symbols and vias on the printed circuit board. You will also learn how to create Flash Symbols that are used to model Thermal Reliefs when designing negative planes.

Anatomy of a Padstack

Through-Hole Padstack

Surface-Mount Padstack

mask

top

inner

anti - pad

thermal relief

inner

bottom

mask

drill size

paste

mask

top

More Information

You define the pad size and shape for all etch and non-etch layers in the Padstack Editor. Default routing layers are BEGIN layer, DEFAULT INTERNAL, and END layer. The DEFAULT INTERNAL padstack definition is used by default when you add more layers in your design. When the padstack is placed in the footprint, the BEGIN layer is mapped to the TOP layer, and the END layer is mapped to the BOTTOM layer.

You can define other internal padstacks with wildcards. In such a case, if a layer is added to the design and the layer name is "matched", this wildcard padstack is used instead of the DEFAULT INTERNAL padstack. For example, if you add a layer to your padstack named "SIG*", and you add a layer into your design named "SIGNAL1", the padstack definition of "SIG*" will be used instead of the padstack definition of "DEFAULT INTERNAL."

Non-etch layers include SOLDERMASK_TOP, SOLDERMASK_BOTTOM (for soldermask artwork) and PASTEMASK_TOP, PASTEMASK_BOTTOM (for solder paste artwork). An extra layer pair named FILMMASK_TOP and FILMMASK_BOTTOM is available for use in whatever means you wish. These two layers are optional and do not have to be used or defined.

Note

If you require sub-mil values to describe padstacks, set the accuracy of your package symbol drawings to a minimum of the same sub-mil value as the padstack, to avoid rounding of padstack features.

Padstack Details

◆ **Regular Pad: A positive pad with a regular shape (circle, square, rectangle, oblong). Flashed on positive layers only.**

regular

◆ **Thermal Relief, Positive: Used to connect pins to a positive copper area; a combination of the regular pad, anti-pad geometry, and tie bars.**

◆ **Thermal Relief, Negative: A flash used to connect pins to a negative copper area.**

TR_80_60

◆ **Anti-Pad: Used to disconnect pins from a surrounding copper area.**

anti - pad

◆ **Shape: Irregularly shaped (custom) pad created with the Symbol Editor.**
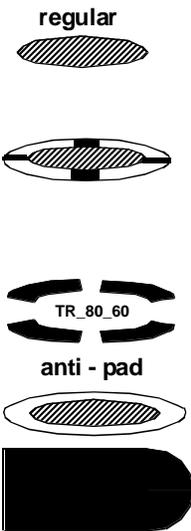
More Information

When you are defining your padstack, you must remember that you are defining a "generic" pad. The pad may be used on a routing layer OR it may be used on a plane layer. For planes, based upon your design environment, the pad may be used on a negative plane or on a positive plane.

Therefore, it is usually best to define all of the regular, thermal and anti-pad definitions for the Begin Layer, Default Internal and End Layer when creating the initial padstack. For each of these definitions, you must define the shape as circle, square rectangle, oblong or shape. Shape is used for any definition that is not a circle, a square, a rectangle or an oblong. A Shape padstack must be manually created using the Symbol Editor.

What is a Thermal Relief?

◆ A thermal relief is a special pattern used where connections are made to an embedded plane that allows heat to concentrate near a pin or via during the soldering process. Usually a "spoked-wheel" pattern.

◆ Allegro supports both a "positive plane" thermal relief and a "negative plane" thermal relief

■ Positive Plane Thermal Relief:
- A combination of the "positive pad", void areas and line draws. The void areas and line draws are defined in the "Shape Parameters" form which will be described later

■ Negative Plane Thermal Relief:
- Defined by a Flash Symbol

Negative Plane Thermal Relief   Positive Plane Thermal Relief
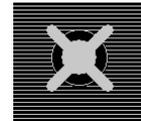
More Information

A thermal relief pad is used to connect a pad to a copper area. This usually occurs on plane layers. However, the thermal relief definition is also used to connect a pad to a copper area created on a routing layer, such as an external shield.

The decision to use either positive planes or negative planes is entirely up to you. Allegro supports either of these technologies. The pictures shown define how Allegro represents a thermal relief pad on a negative and a positive plane.

Flash Symbols

◆ Flash symbols are only required if you are using negative planes.

◆ You create flash symbols in the Allegro Symbol Editor.
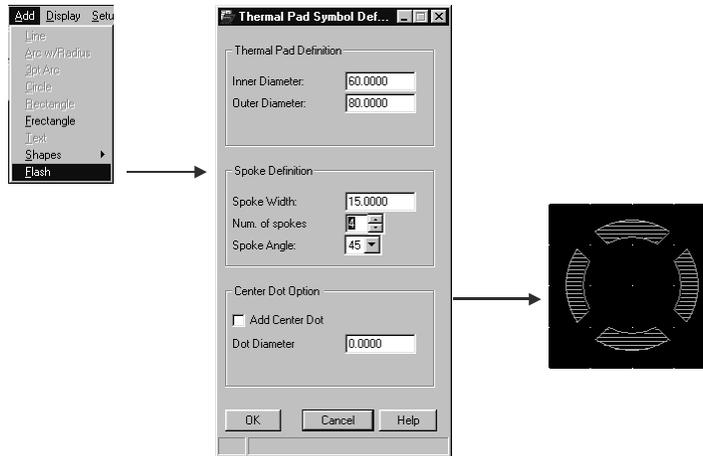
Summary

Again, it is important to remember that you only need to define a flash symbol if you are going to create a negative plane in your design. If you plan to use ONLY positive planes in Allegro, you do not need to create flash symbols.

More Information

You can use the **Add > Flash** command to aid you in creating the negative thermal relief flash. You specify the inner and outer diameter sizes, the spoke width, the number of spokes, and the spoke angle. The center dot section can be used to create a filled circle that will graphically locate the center point of the flash.

A thermal relief is created as a series of filled shapes located on the class Etch, subclass Top. You do not have to use the **Add > Flash** command when creating your thermal relief. You can manually draw any number, size and shape of filled shapes. Be sure to create all graphics on the class Etch, subclass Top.

Lab

◆ Lab: Creating a Flash Symbol
  ■ Start in the Symbol Edit mode.
  ■ Set drawing parameters.
  ■ Create a thermal relief pattern.
  ■ Save the symbol to disk.

More Information

The following lab will teach you how to create a flash symbol for use with a negative plane.

Lab 3-1: Creating a Flash Symbol

Objective: Learn to create flash symbols used for thermal reliefs.

This lab shows you how to create a flash symbol. The flash symbol you create here will be used in the padstacks you create in subsequent labs. Flash symbols are only required if you are going to use negative planes.

Starting in Symbol Edit Mode

1. Start the Allegro Editor.

    The Allegro Editor appears.

   ### Note

    You learned how to start the Editor in the previous labs.

2. Select **File > New**.

    The New Drawing dialog box appears.

3. Type the following name in the Drawing Name field:

    tr_80_60

4. Select **Flash Symbol** from the scrolling list of Drawing Types, as shown below:
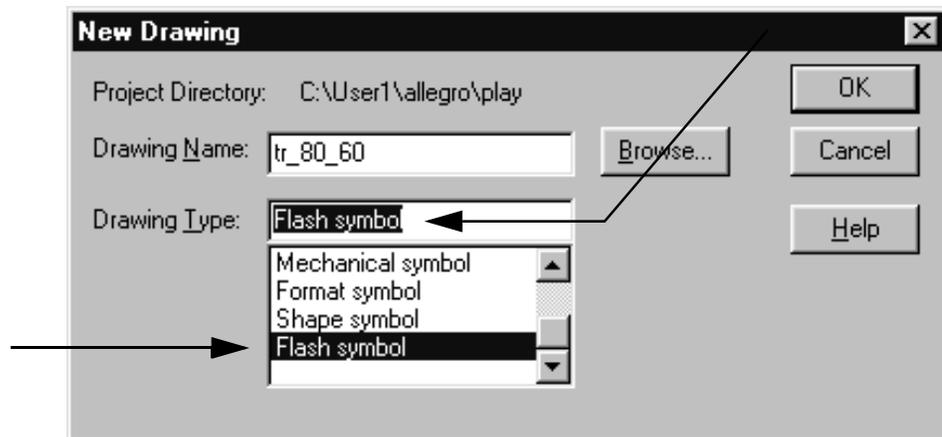
5. Click **OK** to close the New Drawing dialog box.

Setting the Drawing Parameters

Use the Drawing Parameters form to set the drawing size, units, and accuracy. Also use this form to move the drawing origin from the lower left corner to a point inside the drawing area.

Note

The origin of this flash symbol should be the center of the thermal relief flash. In this manner, it will align with the center of the padstack.

1. Select **Setup > Drawing Size**.

2. Locate the Size section in the Drawing Parameters form. Change the size to **A**. This will help you see the graphics while adding data to the symbol.

   The drawing extents will match the extents of the previous drawing (*cds_routed.brd*). The lower left value of (-2200.00,-2400.00) will be sufficient.

3. Click **OK**.

   The Drawing Parameters form closes.

   A default grid setting of 100 mils is displayed.

Creating the Thermal Relief

The Flash Editor has built-in routines to create most of your normal thermal relief flashes. You can also create your own thermal reliefs by adding a series of filled shapes on the Etch class, Top subclass.

1. Select **Add > Flash** from the top menu.

   The Thermal Pad Symbol Definition form is displayed.

2. Fill out the form as follows:

Inner Diameter:	60
Outer Diameter:	80
Spoke Width:	15
Num. of Spokes:	4
Spoke Angle:	45

3. Select **OK** to close the form and create the thermal relief.

4. Select **View > Zoom Fit** to zoom in around just the newly created thermal relief.

Saving the Symbol to Disk

⚠ Caution

The first time the Allegro designer is opened, the default Allegro work directory becomes the active workspace. This directory is defined during software installation. It is therefore important to navigate to the proper directory when saving files.

1. Select **File > Create Symbol** from the top menu.
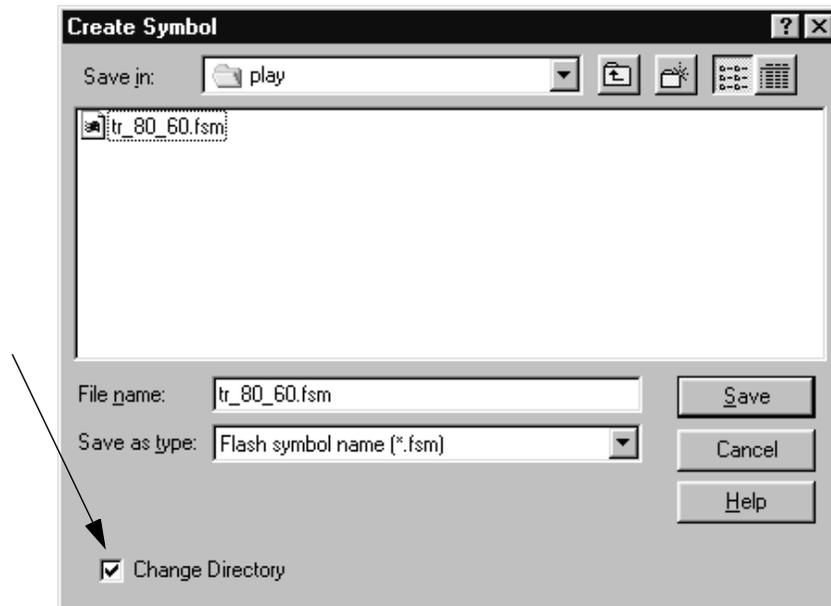
A create symbol form appears, showing the name of the flash symbol as 'tr_80_60'.

2. Navigate if necessary to the directory *<course inst dir>/allegro/play*.

3. Check the **Change Directory** box.

4. Click on **Save** to accept the current "tr_80_60" name.

   The Allegro message area confirms symbol *tr_80_60.fsm* has been created on disk. This file is used when creating your padstacks.

5. Select **File > Save** from the top menu.

   The Allegro message area confirms *tr_80_60.dra* has been saved to disk.

6. Select **File > Exit** from the top menu to exit Allegro.

What Does the Padstack Designer Do?

◆ The Padstack Designer lets you create or edit library padstacks:

- Define the parameters of your padstacks
- Create blind and buried via padstacks
- Add padstack layers
- Copy padstack layers
- Delete layers in a padstack

◆ A library padstack defines pad data for all layers.

◆ Padstacks must be defined before you create package symbols.

Summary

You MUST create padstacks before they can be used. Therefore, you need to proceed with this step before you can create your package symbols, which are the physical footprints.

More Information

You define the pad size and shape for all etch and non-etch layers in the Padstack Editor. Default routing layers are BEGIN layer, DEFAULT INTERNAL, and END layer. The DEFAULT INTERNAL padstack definition is used by default when you add more layers in your design. When the padstack is placed in the footprint, the BEGIN layer is mapped to the TOP layer, and the END layer is mapped to the BOTTOM layer.

You can define other internal padstacks with wildcards. In such a case, if a layer is added to the design and the layer name is "matched", this wildcard padstack is used instead of the DEFAULT INTERNAL padstack. For example, if you add a layer to your padstack named "SIG*", and you add a layer into your design named "SIGNAL1", the padstack definition of "SIG*" will be used instead of the padstack definition of "DEFAULT INTERNAL."

Non-etch layers include SOLDERMASK_TOP, SOLDERMASK_BOTTOM (for soldermask artwork) and PASTEMASK_TOP, PASTEMASK_BOTTOM (for solder paste artwork). An extra layer pair named FILMMASK_TOP and FILMMASK_BOTTOM is available for use in whatever means you wish. These two layers are optional and do not have to be used or defined.

Padstack Designer - Parameters
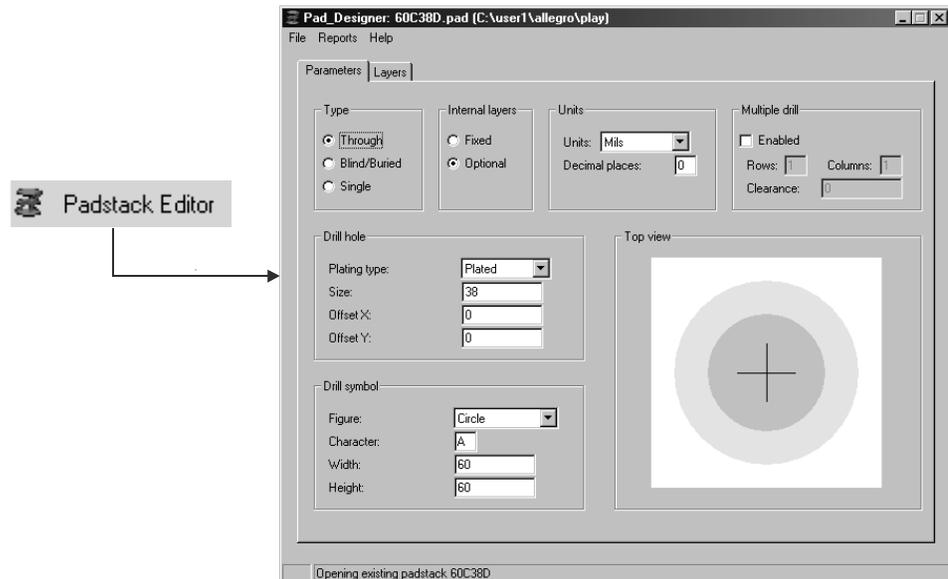
More Information

◆ **Type:** Options are:

> **Through** is a padstack between all layers.
>
> **Blind/Buried** is a padstack spanning consecutive surface and/or internal layers.
>
> **Single** is a surface mount-padstack on top or bottom layers only.

◆ **Internal Layers**: specifies whether you can suppress unconnected internal pads during Gerber generation. Options are:

> **Fixed**: You do not have the option to suppress internal pads.
>
> **Optional**: You can suppress internal pads.

◆ **Units:** Mils, Inches, Millimeters, Centimeters, or Microns. Default is Mils.

◆ **Decimal Places:** specifies number of digits after the decimal. Default is 0.

◆ **Drill Hole** and **Drill Symbol**: Options are:

> **Plating Type**: Options are Plated (default), Nonplated or Optional.
>
> **Size**: A user-defined integer representing the drill size of the hole.
>
> **Offset x/y**: Ability to offset the drill hole from the center of the padstack.
>
> **Figure**: Marks each hole size with a geometric shape such as Circle, Square.
>
> **Character**: Optional character, such as A-Z or 0-9.

Width: User-defined width of the figure.

Height: User-defined height of the figure.

Padstack Designer - Layers

Select Row to modify
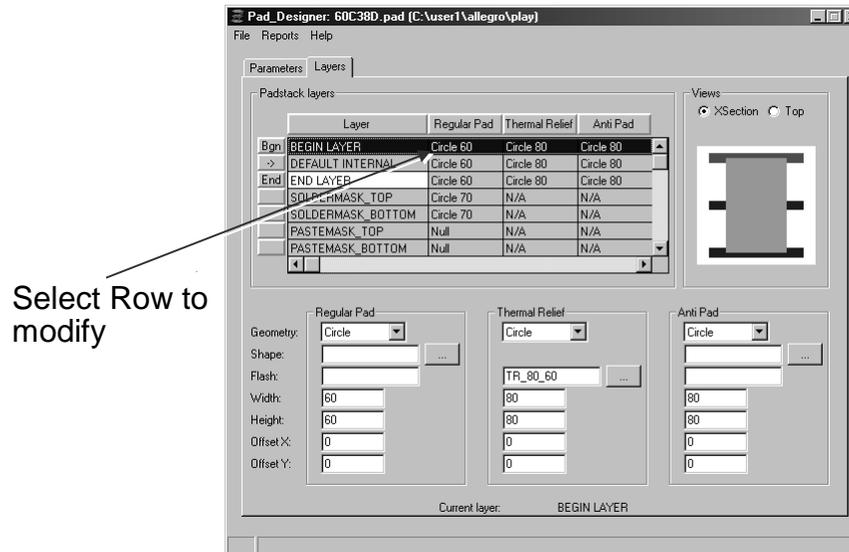
More Information

You select the Layers folder tab in the Pad Designer to view and edit the layer definitions for a padstack. The Begin layer defines the pad that will be used on the top layer of the printed circuit board, while the End layer defines the pad that will be used on the bottom layer of the printed circuit board. The Default Internal layer defines the pad that will be used for all internal layers of the board.

Select a layer in the Padstack Layers section to display the pad information for the layer in the fields at the bottom of the Pad Designer form, so that you can edit them. For through-hole padstacks, you need to define a regular pad, thermal pad, and anti-pad for the top layer, the bottom layer, and the default internal layer. Regular pads, thermal pads, and anti-pads are described later. For surface-mount pads you only need to define a regular pad for the top layer.

The Padstack Designer also lets you enter soldermask pads that will determine the size of the soldermask opening for the padstack on the printed circuit board. You will need a soldermask top and soldermask bottom for through-hole padstacks, and only a soldermask top for single or surface-mount padstacks. A single or surface-mount padstack may also require a solderpaste top pad to allow for the application of solderpaste before the surface-mount components are attached to the printed circuit board in the assembly process.

Defining Pad Shapes/Sizes

regular   **thermal relief**   **anti - pad**
TR_80_60
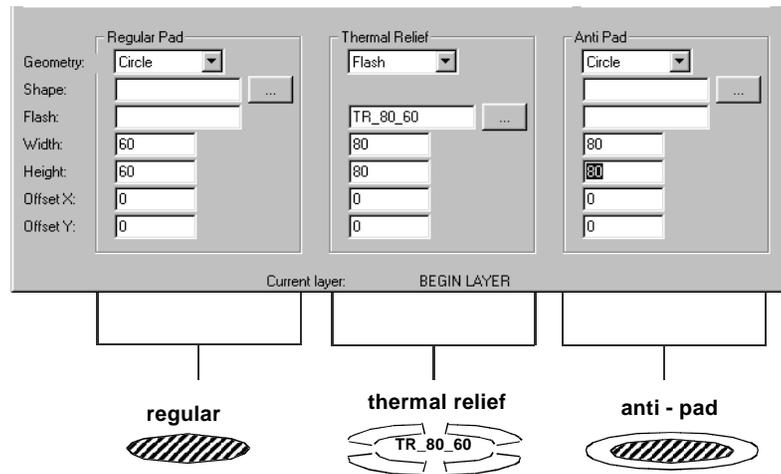
More Information

For each copper layer of the padstack you can define a regular pad, an anti-pad, and a thermal pad. In the printed circuit board design, Allegro uses the regular pad definition for a padstack when the padstack does not pass though a copper plane on a layer. For a negative plane, if the padstack passes through a plane and the pin or via using the padstack needs to be connected to the plane, then the thermal definition is used. If the padstack passes through a plane and the pin or via using the padstack does not need to be connected to the plane, then the anti-pad definition is used.

For each type of pad definition you can enter a standard geometry of circle, square, oblong, or rectangle, with a corresponding width and height. If a non-standard geometry is required, then the Geometry field should be set to Shape. You then need to enter the name of the shape in the Shape field of the pad definition. When this shape is used, Allegro looks for a shape file whose name matches the string in the Shape field. The shape file is created in the Allegro Symbol Editor and saved in a library with a *.ssm* extension.

The Flash field of the Thermal Relief column is used for negative planes. Planes will be discussed in detail in a later module. The name entered here should be a flash symbol defined as part of the library. This would be the same flash you created earlier.

Each pad definition can also have an x and y offset, which will offset the pad relative to the placement of the pin or the via.

Adding/Deleting/Copying Layers

Select with right mouse button here
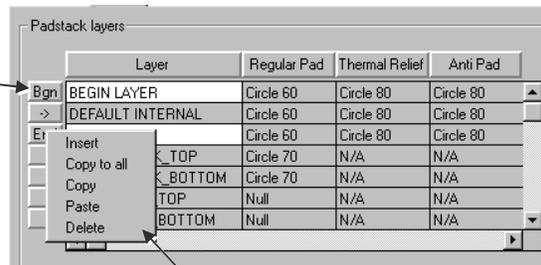
Right Mouse Button pop-up

Summary

You can create pad definitions on specific layer names using the **Add**, **Delete**, **Copy**, **Paste** and **Copy to All** commands. In general, you will only need to define the top, bottom, and default internal layers. The default internal layer definition will be used on any layer of the board that is not defined in the padstack. If you use a padstack with a specific layer defined, and that layer does not exist in the board, then the information for the layer will be ignored.

More Information

By selecting with the right mouse button on the Bgn, "->", or End buttons, you invoke a pop-up menu that has the following options:

**Insert** lets you add a new layer in the padstack.

Copy to All invokes a form where you can copy any or all the Regular/ Thermal Relief/Anti-Pad shapes and sizes to any or all of the Regular, Soldermask, Pastemask or Filmmask layers.

Copy takes a snapshot of the layer and copies the Regular/Thermal Relief/Anti-Pad shapes and sizes into a copy/paste buffer.

Paste takes the previous copy buffer and pastes the Regular/Thermal Relief/Anti-Pad shapes and sizes into the current layer.

Delete removes the current layer from the padstack. You cannot delete BEGIN LAYER, DEFAULT INTERNAL, or END LAYER.

Saving the Padstack
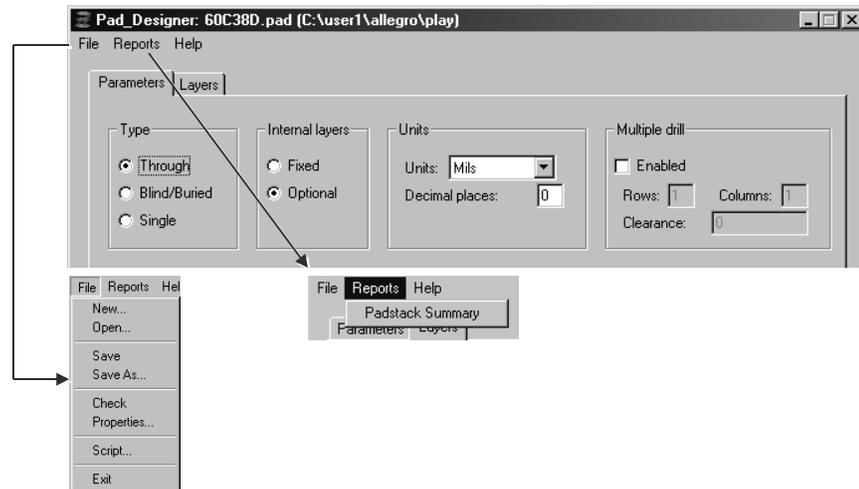
Summary

After editing a padstack or creating a new padstack, you must save it in a padstack library. You must navigate to a padstack library and then enter a name for the padstack in the Name field of the file browser. A padstack library is simply a directory where you will store common types of padstacks. The file will be saved with a *.pad* extension. Allegro will find padstacks based on directories listed in the PADPATH variable that is set in the Allegro environment file. If the same file name is used in multiple padstack libraries listed in the PADPATH variable, Allegro uses the first padstack found.

More Information

The File pull-down menu has the following options:

New lets you begin editing a new padstack. It clears previous settings.

Open lets you edit an existing padstack, or start a new padstack. (Pad layer definitions will reset to Not Defined if this is a new padstack.)

Save lets you save the padstack to disk without closing the form.

Save As lets you save the padstack to disk as a new file name without closing the form.

Check checks the padstack and issues warnings if errors are found (no save).

Script lets you create (record and stop) or replay a script file.

Exit closes the Padstack Designer. If the padstack has not yet been saved, you are prompted as to whether you want to save and exit, save and not exit, or cancel the exit command.

The Reports pull-down menu lets you generate a Padstack Summary report. This report documents all pad sizes and shapes on all layers. This file can be saved to disk using the **File > Save As** pull-down menu in the Padstack Summary report window.

Labs

◆ Lab: Creating Padstacks for a Through-Hole Pin Device
  ■ Create a padstack for a through-hole pin.
  ■ Create a padstack for pin 1of a through-hole pin.
◆ Lab: Creating a Padstack for a Surface-Mounted Device
  ■ Create a padstack for a surface-mounted device.

More Information

The following labs will teach you how to:

■ Create through-hole padstacks.
■ Create surface-mount padstacks.

Lab 3-2:   Creating Padstacks for a Through-Hole Pin Device

Objective: Create padstacks for a through-hole pin.

You will continue working in the *play* directory during this lab to create a padstack named 60c38d. This is a 60-mil-diameter circular pad with a 38-mil plated hole.

In the second part of the lab you will create a padstack named 60s38d. This is a 60-mil square pad, with a 38-mil plated hole. The definition for the previous padstack is very similar to the features needed for this next padstack.

Starting the Padstack Editor

WindowsNT

1. To start the Padstack Editor from WindowsNT, select **Start > Programs > Cadence PSD 14.2 > Allegro Utilities > Padstack Editor**.

    The Pad_Designer form is displayed.

2. Continue with the next section.

UNIX

1. To start the Padstack Editor from UNIX, enter the following command in a UNIX shell window:

    pad_designer &

    The Padstack Designer form is displayed.

2. Continue with the next section.

Creating the Padstack in the Correct Directory

The **first** time Pad Designer is run by a user, the current working directory will be set to a location defined by the software installation. The following steps will be used to create the padstacks in the correct working directory. After this, all padstacks will be saved in the correct working directory.

1. Select **File > New** from the Pad Designer main menu.

    A file browser window opens.

2. Navigate to the *<course inst dir>/allegro/play* directory.

3. In the File Name field, type the name for this padstack:

    60c38d

4. Click the **Change Directory** box.

This causes the *play* directory to become your current working directory. The browser window should look like this:
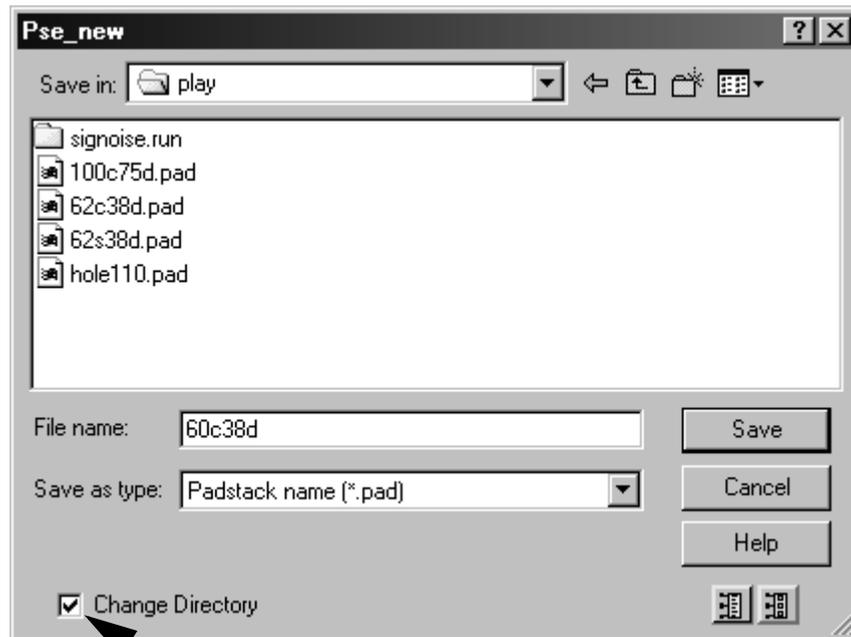
**This causes your working directory
to become <course inst dir>/allegro/play.**

5. Select **Save** to define the new padstack name and set the current working directory.

Describing the NCDRILL Requirements

1. Fill out the **Drill Hole** section of the form as follows:

Plating Type: Plated

Size: 38

Offset X: 0

Offset Y: 0

2. Fill out the **Drill Symbol** section of the form as follows:

Figure: Circle

Character: A

Width: 60

Height: 60
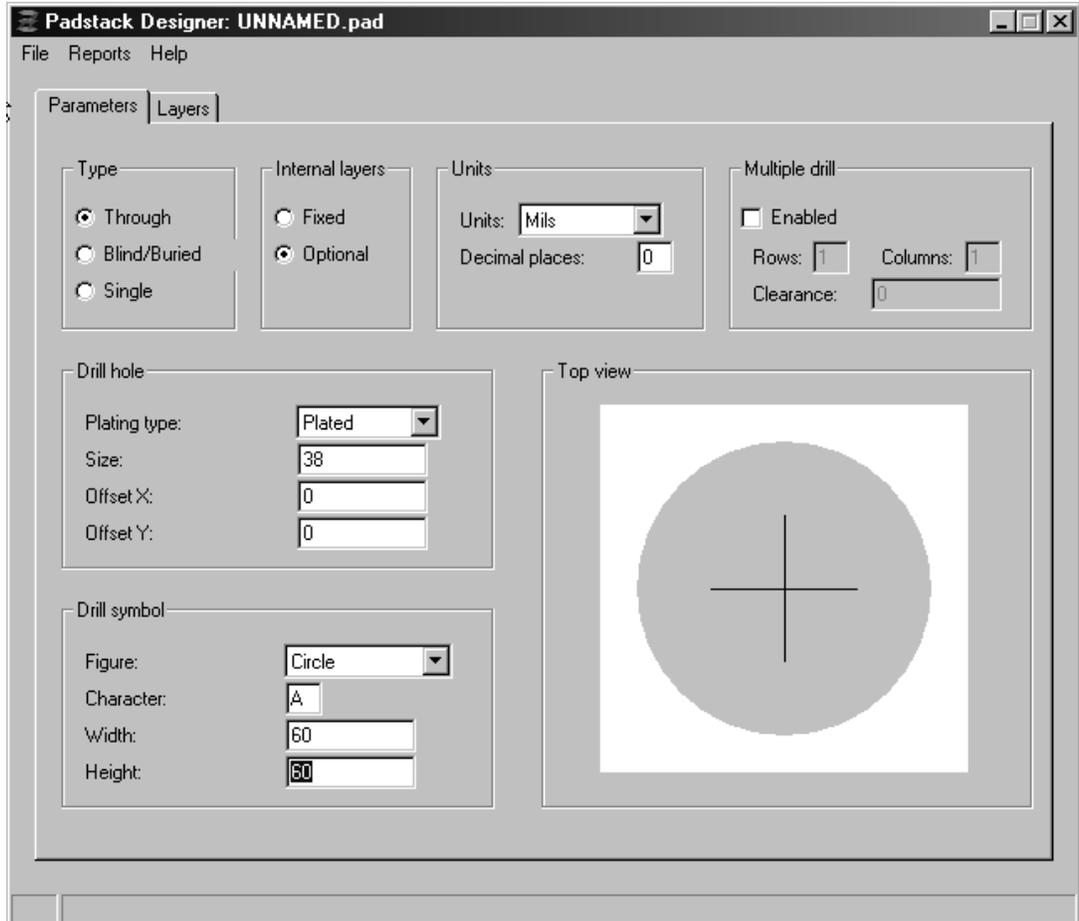
Describing the BEGIN LAYER Pad

1. Select the **Layers** tab in the Padstack Designer form to bring the layer definition section to the top of the form.

2. Select the **Regular Pad** column of the BEGIN LAYER row, as shown below:

The bottom portion of the form displays the current definitions for the BEGIN LAYER pad. Notice that all values are Null. Also, the CURRENT LAYER section now specifies BEGIN LAYER.

3. Fill out the following values for the BEGIN LAYER row:

Note

In the Thermal-Relief section, when you enter the flash name, the Geometry option will automatically be set to "Flash". You must re-set the Geometry option to Circle before you can modify the Width and the Height fields.

REGULAR-PAD

Geometry:	Circle
Width:	60
Height:	60

THERMAL-RELIEF

Geometry:	Circle
Flash:	TR_80_60
Width:	80
Height:	80

ANTI-PAD

| Geometry:	Circle
Width:	80
Height:	80

The BEGIN LAYER pad is now defined.

Describing the DEFAULT INTERNAL and END LAYER Pads

Because the DEFAULT INTERNAL and END LAYER pads are the same size and shape as the BEGIN LAYER, you will use the **Copy** command to save time.

1. To copy the BEGIN LAYER pad definition, select the **Bgn** button with the right mouse button, as shown below:
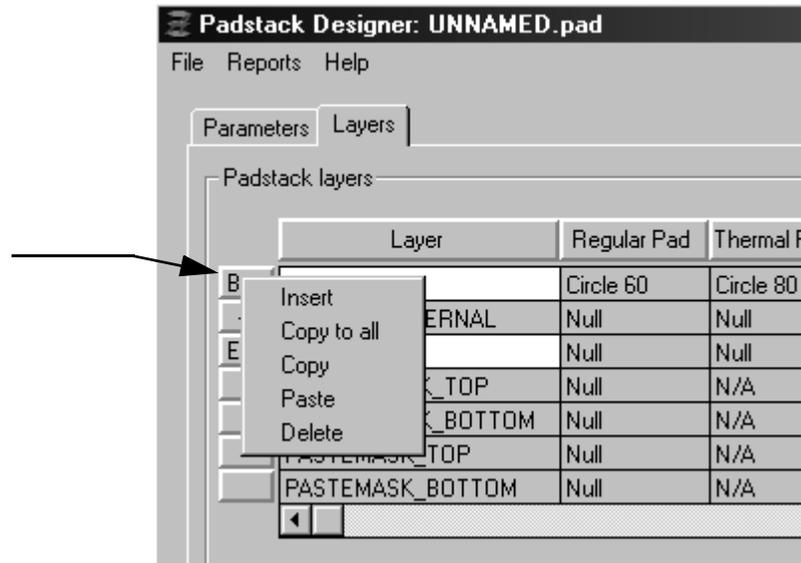
A pop-up menu is displayed.

2. Select **Copy to all** from the pop-up menu.

The Copy to All pop-up menu is displayed. Make any changes required to match the form as shown below:
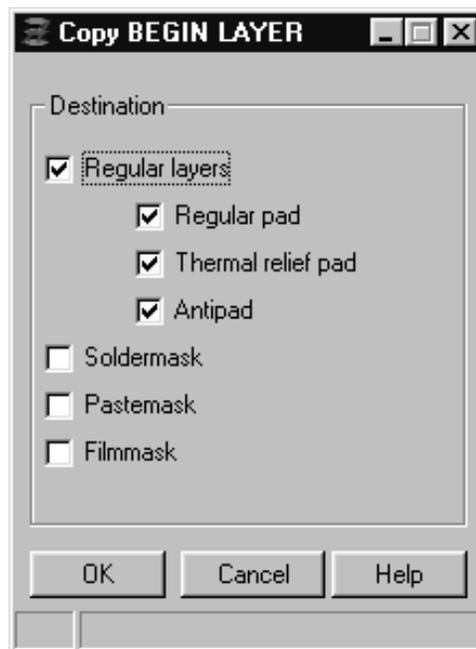
3. Select **OK**.

The Begin Layer pad is copied to the Default Internal Layer and the End Layer.

Next, define the soldermask requirements.

Describing the SOLDERMASK Pads

1. Select the **Regular Pad** column of the SOLDERMASK_TOP row.

   The bottom portion of the form displays the current definitions for the SOLDERMASK_TOP pad.

2. Fill out the following values for the SOLDERMASK_TOP Regular Pad in the bottom section of the form:

   Geometry: Circle

   Width: 70

   Height: 70

   You will now copy the top soldermask definition to the bottom soldermask.

3. With the right mouse button, select the button to the left of SOLDERMASK_TOP.

4. Select **Copy** from the pop-up menu.

   The message area states "Copying from: SOLDERMASK_TOP" (at the extreme bottom of the Padstack Designer form).

5. With the right mouse button, select the button to the left of SOLDERMASK_BOTTOM.

   A pop-up menu is displayed.

6. Select **Paste** in the pop-up menu.

   The message area states "Pasting to: SOLDERMASK_BOTTOM" (at the extreme bottom of the Padstack Designer form).

7. Select **File > Save** from the top menu of the Padstack Designer form.

   The padstack file (*60c38d.pad*) is saved to disk.

Note

It is important that you save ALL padstacks you create in this module in the *play* directory. It is good design practice to use a padstack name that is descriptive. "60c38d" refers to a 60-mil circular pad with a 38-mil drilled hole.

Note

DO NOT close the Padstack Editor at this point because you will use many of your current settings to create your next padstack.

Describing the BEGIN LAYER and END LAYER Pads for Pin 1

Because of the similarities between this padstack and the last, all you need to do is change the Geometry field of the BEGIN LAYER and END LAYER pads. The internal pad remains unchanged.

1. Select the **Layers** tab to bring it to the top of the form, if it is not currently on the top.

2. Select the **Regular Pad** column of the BEGIN LAYER row.

   The bottom portion of the form displays the current definitions for the BEGIN LAYER pad.

3. Click the scroll button in the Geometry field and select **Square** for REGULAR-PAD, THERMAL-RELIEF and ANTI-PAD.

   The BEGIN LAYER pad is now a square.

4. To copy the BEGIN LAYER pad definition, use the right mouse button to select the **Bgn** button to the left of BEGIN LAYER.

   A pop-up menu is displayed.

5. Select **Copy** in the pop-up menu.

   The message area states "Copying from: BEGIN LAYER" (at the extreme bottom of the Padstack Designer form).

6. With the right mouse button, select the **End** button to the left of END LAYER.

   A pop-up menu is displayed.

7. Select **Paste** from the pop-up menu.

   The message area states "Pasting to: END LAYER" (at the extreme bottom of the Padstack Designer form).

Describing the SOLDERMASK Pads

Because of the similarities between this padstack and the last, all you need to change is the geometry of the top and bottom soldermask pads.

1. To change the top soldermask to square, select the **Regular Pad** column of the SOLDERMASK_TOP row.

   The bottom portion of the form displays the current definitions for the SOLDERMASK_TOP pad.

2. Click the scroll button in the Geometry field of the Regular Pad and select **Square**.

3. To change the bottom soldermask to square, select the **Regular Pad** column of the SOLDERMASK_BOTTOM row.

The bottom portion of the form displays the current definitions for the SOLDERMASK_BOTTOM pad.

4. Click the scroll button in the Geometry field of the Regular Pad and select **Square**.

Saving the Padstack to Disk

1. Select **File > Save As** from the top menu of the Padstack Designer form.

A file browser window opens.

2. In the File Name field, type the name for this padstack:

60s38d

3. Click **Save** to save the file and close the browser menu.

The padstack file (*60s38d.pad*) is saved to disk.

There is no need to close the Padstack Editor until you have completed all your pad editing work.

STOP **End of Lab**

Lab 3-3:   Creating a Padstack for a Surface-Mounted Device

Objective: Create a padstack for a surface-mounted device.

In this lab, you will create a padstack named 76x24smd. This is a 76- by 24-mil rectangular pad with no drilled hole (for surface mount devices). It is assumed that the Padstack Editor menu is still open. To reopen it, use the steps you learned in Lab 2-1.

Naming the Padstack

Since the padstack you are now about to create has no similar features to the previous padstack, use the following technique to remove all the information currently in the Padstack Designer form, and create a new padstack.

1. Select **File > New** from the top menu of the Padstack Designer form.

2. In the File Name field, enter:

   76x24smd

3. Click **Save** to close the browser menu.

4. Select the **Parameters** tab to bring it to the top of the form, if it is not currently on the top.

5. Set the padstack Type to **Single**.

Describing the BEGIN LAYER Pad

1. Select the **Layers** tab to bring this section to the top of the form.

   Notice that DEFAULT INTERNAL and END LAYER no longer appear. They are not needed for single-layer padstacks.

2. Select the **Regular Pad** column of the BEGIN LAYER row.

   The bottom portion of the form displays the current definitions for the BEGIN LAYER pad. Notice that all values are Null. Also, the CURRENT LAYER section now specifies BEGIN LAYER.

3. Fill out the following values for the BEGIN LAYER pad in the bottom section of the form:

   REGULAR-PAD

Geometry:	Rectangle
Width:	76
Height:	24

THERMAL-RELIEF

Geometry:	Rectangle
Width:	96
Height:	44

ANTI-PAD

Geometry:	Rectangle
Width:	96
Height:	44

Note

Thermal relief and anti-pad definitions are needed on surface-mount pads only if you plan to use copper-filled areas on the external layers of the design. If you are not going to have copper areas on the external layers, you do not need to define thermal relief and anti-pad values for your surface-mount padstacks.

Describing the SOLDERMASK Pad

1. To define the top soldermask, select the **Regular Pad** column of the SOLDERMASK_TOP row.

   The bottom portion of the form displays the current definitions for the SOLDERMASK_TOP pad.

2. Fill out the Regular Pad section as follows:

Geometry:	Rectangle
Width:	86
Height:	34

Describing the PASTEMASK Pad

Because this is a surface-mount padstack, you will need to define a *pastemask_top* pad. You do this by copying the BEGIN LAYER pad.

1. To copy the BEGIN LAYER pad definition, use the right mouse button to select the **Bgn** button to the left of BEGIN LAYER.

   A pop-up menu is displayed.

2. Select **Copy** from the pop-up menu.

   The message area states "Copying from: BEGIN LAYER" (at the extreme bottom of the Padstack Designer form).

3. With the right mouse button, select the button to the left of PASTEMASK_TOP.

A pop-up menu is displayed.

4. Select **Paste** from the pop-up menu.

The message area states "Pasting to: PASTEMASK_TOP" (at the extreme bottom of the Padstack Designer form). Even though the BEGIN LAYER pad had definitions for thermal relief and anti-pad, these are not applicable to a solder paste layer, so those definitions are not copied. Only the Regular Pad definition is copied.

Note

No SOLDERMASK_BOTTOM or PASTEMASK_BOTTOM pad definitions are required. If a part is placed on the bottom side of the board, the system automatically "moves" all definitions from the TOP layer to the BOTTOM layer.

For surface-mount padstacks, you only require the BEGIN LAYER, SOLDERMASK_TOP and PASTEMASK_TOP pad layers. All others should read "Null".

Saving the Padstack to Disk

1. Select **File > Save** from the top menu of the Padstack Designer form.

The padstack file (*76x24smd.pad*) is saved to disk.

2. Select **File > Exit** from the top menu of the Padstack Designer form.

The Padstack Designer closes.

STOP **End of Lab**

4

Lesson 4:   Component Symbols

Learning Objectives

◆ Use the Package Symbol wizard to create a package symbol.

◆ Use the Symbol Editor to create a surface-mount package.

Summary

In this section you will create Allegro footprint symbols that model the components that are placed on the printed circuit board. You will learn how to use the Symbol wizard to create footprints and also how to manually create footprints.

Package Symbol Wizard

Use the Package Symbol wizard to create a footprint:

◆ Select the type of footprint to be created.

◆ Select "Template" to be used.

◆ Define units.

◆ Define number of pins and part dimensions.

◆ Select padstacks to be used.

◆ Define origin of footprint.

More Information

The Package Symbol Wizard can create may different styles of footprints including DIP's, SOIC's, PLCC's, QFP's and so on. You can define information such as design units, number of pins, pin spacing, padstacks to use, and so forth.

After running the Package Symbol Wizard, you can edit and modify any of the items created by using the standard Allegro user interface.

Lab

◆ Lab: Creating a DIP16 Package Using the Package Symbol Wizard

  ▪ Use the Package Symbol wizard to create a DIP16 symbol.

More Information

The following lab will allow you to familiarize yourself with the process of creating a DIP package using the Package Symbol Wizard. The wizard can create several different styles of footprints including DIP's, SOIC's, PLCC's, QFP's and so on.

Lab 4-1:   Creating a DIP16 Package Using the Package Symbol Wizard

Objective: Learn to use the Package Symbol Wizard to create a through-hole package symbol.

This lab shows you how to create a package symbol for a 16-pin, dual in-line package (DIP) using the Package Symbol Wizard. You will use the through-hole padstacks you defined earlier.

Naming the Symbol

1. Start the Allegro Editor.

   The Allegro Editor appears.

   ### 🖎 Note

   You learned how to start the editor in the previous labs.

2. Select **File > New** from the top menu.

   The New Drawing dialog box appears.

3. Type the following name in the Drawing Name field:

   dip16

4. Select **Package symbol** (**wizard**) from the scrolling list of drawing types, as shown below:
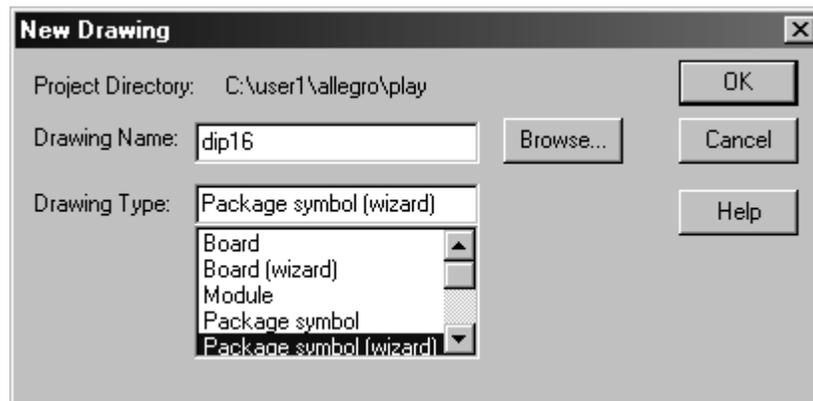
5. Click **OK** to close the New Drawing dialog box.

   The Package Symbol Wizard form is displayed. This form is used to specify the type of Package Symbol Wizard to be used.

Using the Package Symbol Wizard

1. Select **DIP** as the type of Package Symbol Wizard to be used (if this option is not currently selected).

2. Select **Next>** to use the DIP wizard and continue to the next form.

    The Template form is displayed.

    This form is used to specify the drawing template to be used when creating the symbol. The drawing template "seeds" such items as color of classes and subclasses, units of the drawing, accuracy of the drawing, and so forth.

3. Select **Default Cadence supplied Template** if this option is not currently selected.

4. Select **Load Template** to load the default template.

5. Select **Next>** to continue to the next form.

    The General Parameters form is displayed.

    This form is used to specify some of the drawing parameters, as well as the reference designator labels. The values for Units and Accuracy are obtained from the drawing template specified in the previous form.

6. Set the values of Units to **Mils** and Accuracy to **2** for both *Units used to enter dimensions in this wizard* and *Units used to create package symbol*, if these values are not currently set.

7. Set the Reference Designator Prefix to **U*** if this value is not currently set.

8. Select **Next>** to continue to the next form.

    The DIP Parameters form is displayed.

    This form is used to specify DIP-specific parameters. This includes items such as pin-to-pin spacing, spacing between columns, and the overall package dimensions used to create the assembly and silkscreen outlines.

9. Modify the form as required, to match the following values:

Number of Pins(N):	16
Lead Pitch(e):	100
Spacing between two terminal rows (e1):	300
Package Width(E):	220
Package Length(D):	785

10. Select **Next>** to continue to the next form.

    The Padstacks form is displayed.

    This form is used to specify the padstacks to be used for the pins. You can specify a different padstack for pin 1 from the rest of the pins.

11. Select the **"..."** button next to the empty field for Default Padstack to Use for Symbol Pins.

A Package Symbol Wizard padstack browser appears.

Select the padstack **60c38d** (case is unimportant).

12. Select **OK** to use the 60-mil round pad you created earlier, and close the Padstack browser form.

13. Select the "**...**" button next to the field for **Padstack to Use for Pin 1**.

A Package Symbol Wizard padstack browser appears. Select the padstack **60S38d** (case is unimportant).

14. Select **OK** to use the 60-mil square pad you created earlier and close the padstack browser form.

15. Select **Next>** to continue to the next form.

The Symbol Compilation form is displayed.

This form is used to specify the location of (0,0) relative to the rest of the pins, as well as whether to compile the symbol or not.

16. Select **Pin 1 of symbol** as the location of the symbol origin (if this option is not currently selected).

17. Select **Create a compiled symbol** for whether or not the Package Symbol Wizard should generate a compiled symbol (if this option is not currently selected).

18. Select **Next>** to continue to the next form.

The Summary form is displayed.

This form is used to verify that the correct files are to be created. This is also your last chance to go "backwards" through any previous form to change any data or specifications.

19. After verifying that the files *dip16.dra* and *dip16.psm* will be created, select **Finish** to complete the Package Symbol Wizard and create the dip16 symbol.

The dip16 drawing (*dip16.dra*) and symbol (*dip16.psm*) are created and the footprint is opened in the Symbol Editor. At this point you can make any changes that you require. If you do make changes, be sure to create the symbol and save the drawing.

STOP **End of Lab**

Drawing Parameters Form

User Units specifies the unit of measure used during the design process.

Size specifies the size of the drawing area required.

Accuracy sets the accuracy of the drawing database.

Drawing Extents shows the height and width of the drawing, and the location of the lower left corner with respect to the drawing origin (located in the lower left corner by default).

Move Origin relocates the drawing origin (datum 0,0). The X, Y coordinates for the new origin are then listed into the Drawing Extents section.

More Information

Select the appropriate drawing parameters:

> **Project** is the current directory path name.

> **Drawing** specifies the name of the package symbol you are creating.

> **Type** can be Package (*.psm*), Mechanical (*.bsm*), Format (*.osm*), Flash (*.fsm*), or Shape (*.ssm*).

> **User Units** can be Mils, Inches, Millimeters, Centimeters, or Microns. The default is Mils.

> **Size** can be A, B, C, D or Other (A1, A2, A3, A4 for metric units). The default is A.

> **Accuracy** is the number of decimal places. Range is 0 - 2; the default is 1.

Click **OK**.

Drawing Origin

◆ Drawing origin (0,0) is located in the lower left corner by default.

◆ To set a package symbol origin, you must relocate the origin to a point somewhere on the symbol (for example, pin 1 or the body center).

◆ You may want to move the drawing origin before placing the pins of the device. If not, you can move the origin any time during the creation process by selecting **Setup > Drawing Size**.

More Information

When you start a new symbol drawing, the origin (0,0) is located in the lower left corner by default. This origin must be relocated to a point somewhere on the symbol (for example, pin 1 or the body center), and will be used as the package symbol origin.

You may find it convenient to move the drawing origin before placing the pins of the device. If not, you can move the origin any time during the creation process by selecting **Setup > Drawing Size**.

Moving the Drawing Origin
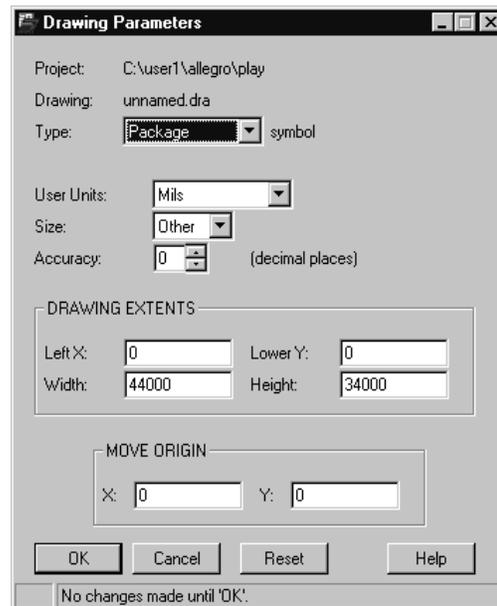
Setup > Drawing Size
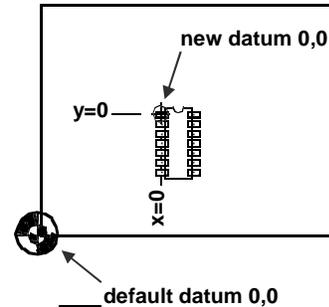
More Information

There are two methods you can use to move the origin of the footprint. First you can use the Move Origin section. You enter the amount that you want to move the origin based upon the current origin. In this example, since you want to move the origin from the default location to the new location, you would enter positive X and positive Y values.

Note

When you enter a value in the Move Origin section, use the **Tab** key to have the value take effect. When you hit the **Tab** key, the Move Origin field will reset to 0 and the Left X or Lower Y field of the Drawing Extents section will be updated.

You can also use the Drawing Extents section to move the origin of the footprint. When using this section, you enter in the new value of the bottom left or upper right of the drawing area. Again, using the current example, you would enter in negative numbers for the Left X and Lower Y fields. Use the **Tab** key to proceed to the next field.

Allegro Symbol Types
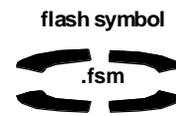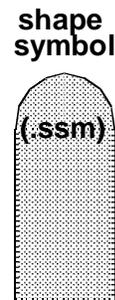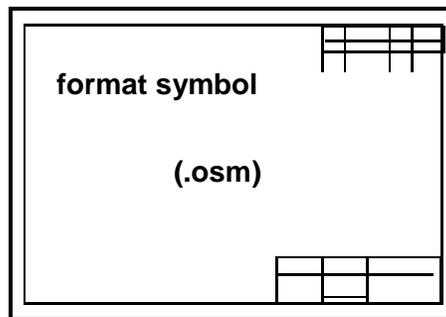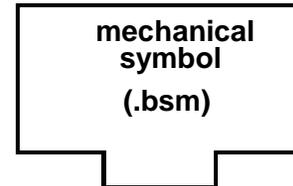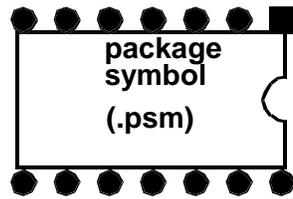
More Information

The Allegro Symbol Edit mode lets you create the following symbols:

◆ Package Symbol (*.psm*)

   Used for footprints such as dip14, soic14....

◆ Mechanical Symbol (*.bsm*)

   A generic card outline, mounting hole

◆ Format Symbol (*.osm*)

   A-D size page format, company logo, assembly/fab notes, cross section diagram, and so on.

◆ Shape Symbol (*.ssm*)

   Creates a filled polygon (*shape*) used for custom pads.

◆ Flash Symbol (*.fsm*)

   A symbol used to represent a thermal relief connection on a negative plane.

Example: a 14-pin DIP Package
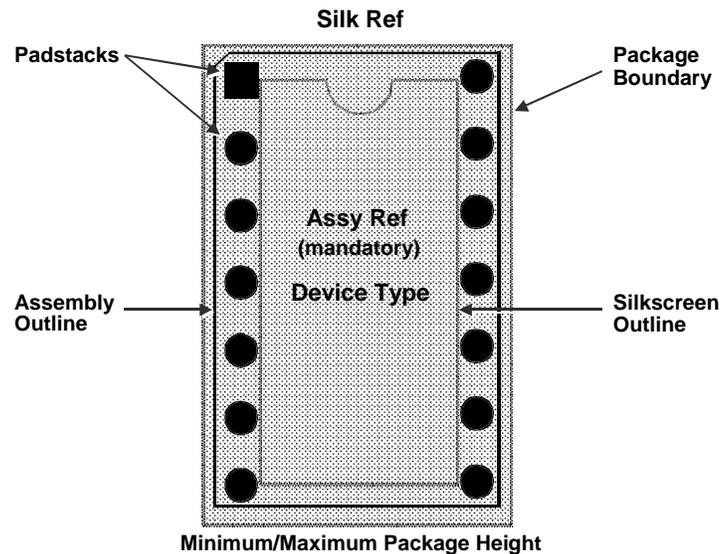
More Information

A typical dip package contains pins (padstacks), an assembly and silkscreen outline, and placeholder labels for assembly/silkscreen reference designators and device types.

To create an Allegro package symbol:

◆ Add pins (padstacks).

◆ Draw component outlines for assembly and silkscreen layers.

◆ Add the placeholder labels for assembly and silkscreen designators (at least one is mandatory).

◆ Define constraint areas (routing and via keepouts, package boundary and height information).

◆ Assign Minimum Package Height or Maximum Package Height, or both, using the **Setup > Areas > Package Height** command.

◆ Create a symbol file (*.psm*). This is a binary file, used during placement only. It cannot be read by the Allegro Symbol Editor. Use **File > Create Symbol** to generate this file.

◆ Save the drawing file (*.dra*). This is a graphics file; it can be used for editing purposes only. Use **File > Save** to generate this file.

Note

It is important to keep the symbol (*.psm*) and drawing (*.dra*) files synchronized by saving the drawing file each time you create the symbol file.

Adding Pins

Layout > Pins
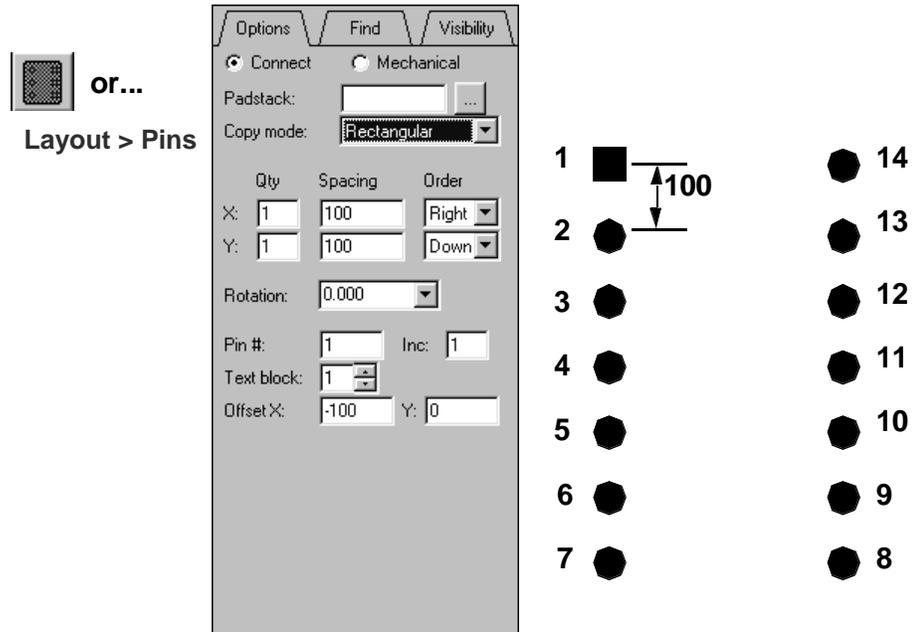
Summary

Allegro will search the padstack directories defined by your PADPATH variable for the padstack you specify. This variable is defined in the "env" file. If the padstack or any part of the padstack (such as a flash symbol) cannot be found, an error will be reported.

More Information

Padstack: Enter the padstack name (not case sensitive—looks for lowercase file on disk) or use the Padstack browser.

X: the number of pin columns to be added.

Y: the number of pin rows to be added. For multiple rows and columns, the array expands in the X, or column, direction first (horizontally), followed by Y, or rows, second (vertically).

Spacing: used to specify pin-to-pin spacing within the column(s) and row(s).

Left/Right: (toggle field) used to specify direction of column expansion (from start point).

Up/Down: (toggle field) used to specify direction of row expansion (from start point).

**Rotation**: can be 0, 45, 90, 135, 180, 225, 270, 315, or user-defined angle. The default is 0.

Pin #: shows the next pin to be added. Alphanumeric pin names are okay (not case sensitive). Last character of pin name is incremented first (A1->A2, 1A->1B, 1AZ->1BA).

Inc: specifies pin number increment. The default is 1.

Text Block: Each pin you add includes a visible pin number. This parameter determines the size of the pin number (text). Enter text block number 1-16. See the **Define > Text** command for more information.

Offset X/Y: offsets the pin number text with respect to the pin center. The default is -100, 0 (left of pin center).

Drawing Component Outlines

Add > 3pt Arc

Add > ...

| Line |
| Arc w/Radius |
| 3pt Arc |
| Circle |
| Rectangle |
| Frectangle |
| Text |
| Shapes ▶ |
| Flash |
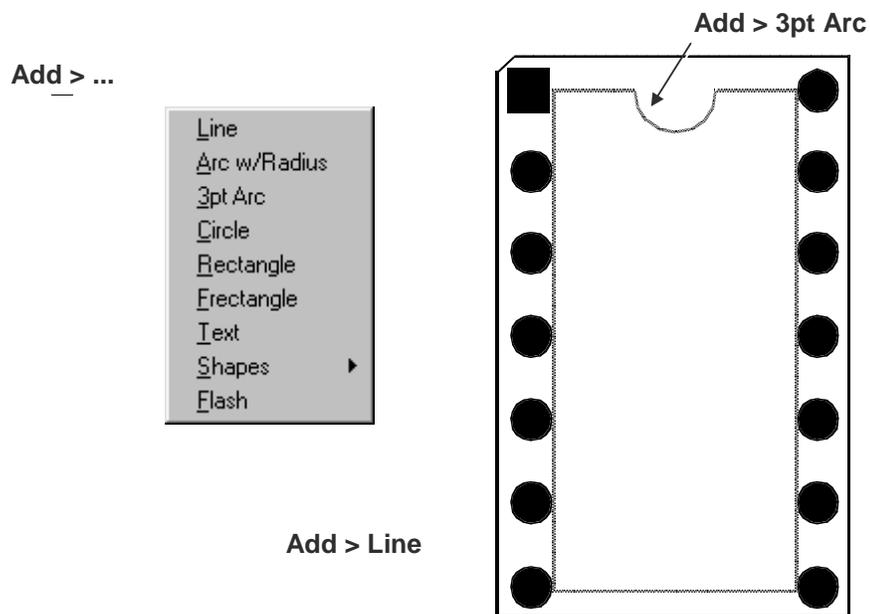
Add > Line

More Information

You create the Assembly Outline of your symbol using the **Add Line** command. Set the class and subclass in the Options form to PACKAGE_GEOMETRY and ASSEMBLY_TOP, and define the outline of the component using lines and arcs.

You create the silkscreen for the component in the same fashion, by adding lines and arcs, but the silkscreen outlines will be added on the SILKSCREEN_TOP and SILKSCREEN_BOTTOM subclasses. Be sure to set the Line Width field to an appropriate value when adding lines and arcs on the silkscreen subclasses. The line width will define the line width of the silkscreen line on the actual printed circuit board.

Adding Labels
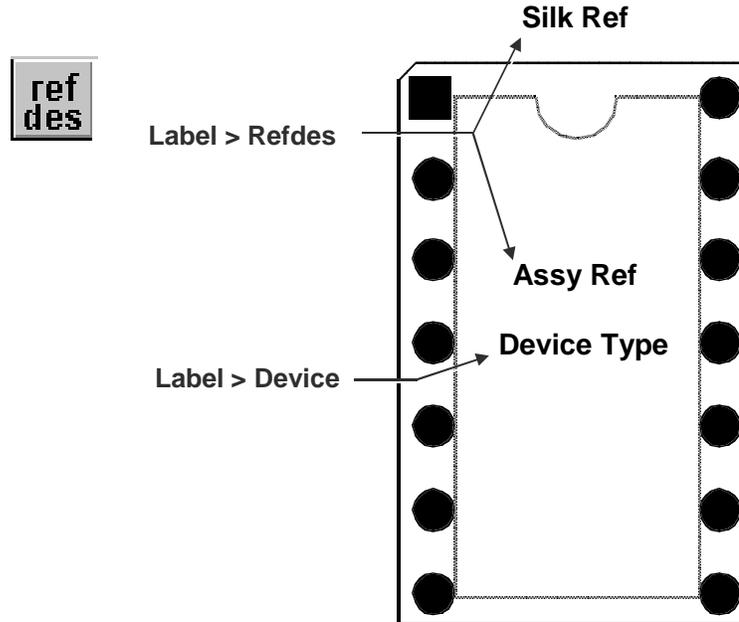
More Information

Labels are placeholders for component data such as assembly/silkscreen reference designators and device types. The location of the label determines where the data is displayed. You must define at least one label in order to successfully create a footprint.

When adding a label, use the Options form to specify the text block size. This controls the size of the displayed data (for example, assembly refdes).

What you type can be used by automatic renaming later. Up to (but not including) the last character of the reference designator name you use will be retained by the automatic rename feature, if you wish.

Use the Options form to specify the drawing layer (class/subclass) for your text label. Depending on which command you select, the Options form will default to an appropriate class/subclass setting. If you are creating silkscreen text labels, you will need to toggle the Subclass field to Silkscreen_Top.

Defining Area Constraints

Setup > Areas

Silk Ref

Assy Ref

Device Type

.050   .150
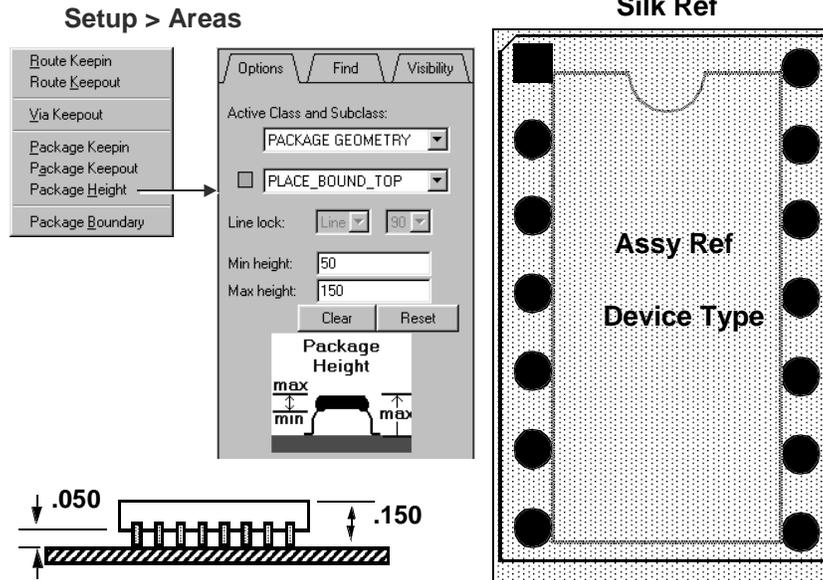
More Information

To define areas, use the pull-down menu from the **Setup > Areas** command.

> **Route Keepout** is a user-defined polygon that prohibits conductors.

> **Via Keepout** is a user-defined polygon defining an area that prohibits vias.

> **Package Boundary** defines a two-dimensional area that is used to check for package overlap. It is a filled polygon. If none exists, one is automatically created for you with the Create Symbol command.

> **Package Height** defines the package height (z dimension) information that is attached to the package boundary. The height is a range: bottom of package (Min Height), top of package (Max Height). If only one value is specified, it assumes the package starts from the board surface, and extends to the given Max Height. You can also use this command to create the package boundary.

Use the Options form to specify the drawing layer (class/subclass) for your constraints. Depending upon which command you select, the Options Class/Subclass fields show certain default settings.

Saving Symbol Files

Saving the *.psm* file

- This file is the binary equivalent of your drawing file, and is the file used during placement to represent a component's physical layout.
- The Create Symbol command automatically checks the drawing for common errors. This step is also known as "compiling" the symbol.

Saving the *.dra* file

- The binary package symbol file (*.psm*) cannot be viewed or edited, but you can open the drawing file (*.dra*). Therefore, the drawing file must also be saved to disk, and kept in the library directory in the event you need to make a revision.

More Information

Saving the *.psm* File

Once your drawing is complete, you must make a package symbol file (*.psm*). This file is the binary equivalent of your drawing file, and is the file used during placement to represent a component during physical layout.

The **Create Symbol** command automatically checks the drawing for common errors. For example, it checks to make sure you have at least one refdes label. It also checks for package boundaries. If your package symbol has no package boundary defined, this command automatically creates one either by using the Package Geometry/Assembly_top graphics or by surrounding all the device pins with a rectangle (tangent to the pin edges), whichever is larger. This step is also known as "compiling" the symbol.

Saving the *.dra* File

The Allegro Editor can only read a *.dra* file. It does not read the *.psm* file. Therefore, it is important to save this version of the footprint along with the compiled symbol (*.psm*)

Note

Save both the *.psm* and the *.dra* files. You can extract these files from an archived design, but you should keep both files available during the current project.

Labs

◆ Lab: Creating a DIP14 Package Symbol
  ■ Add pins
  ■ Add the silkscreen/assembly outlines
  ■ Add the Refererence Designator labels
  ■ Add Package Height
  ■ Save the footprint
◆ Lab: Creating an SOIC 16 with the Symbol Editor (optional lab)

More Information

In the following labs, you will create from scratch footprints for a

■   Through-hole part

■   Surface-mount part.

Lab 4-2:   Creating a DIP14 Package Symbol

Objective: Learn to create package symbols.

This lab shows you how to create a package symbol for a 14-pin dual inline package (DIP). You will use the padstacks you created to represent the pins of the device.

Starting in Symbol Edit Mode

1. Select **File > New**.

   The New Drawing dialog box appears.

2. Type the following name in the Drawing Name field:

   dip14

3. Select **Package Symbol** from the scrolling list of drawing types, as shown below:
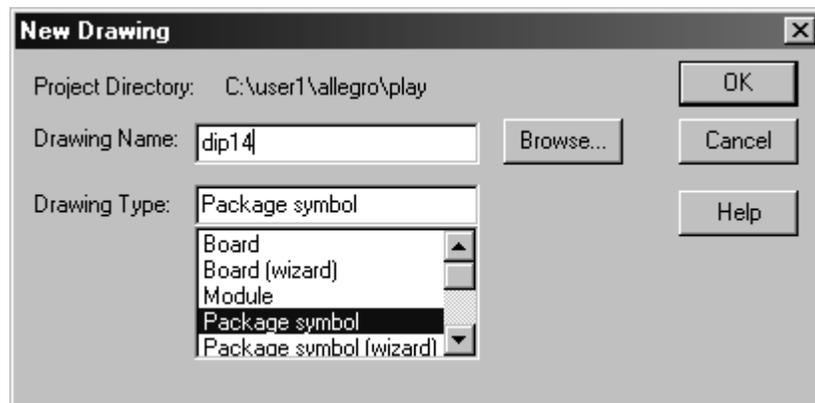
4. Click **OK** to close the New Drawing dialog box.

Setting the Drawing Parameters

Use the Drawing Parameters form to set the drawing size, units, and accuracy. Also use this form to move the drawing origin from the lower left corner to a point inside the drawing area.

Note

The origin of this package symbol drawing will become the package origin when you are in the component placement phase of your design.

1. Select **Setup > Drawing Size**.

   All of the parameters should match the previous "dip16" package symbol.

2. Modify the form as required to match the following values:

Type:	Package
User Units:	Mils
Size:	A
Accuracy:	2
Left X:	5000
Lower Y:	5000

3. Click **OK**.

The Drawing Parameters form closes. The drawing origin is now near the center of the work area.

Adding Pins

The first pin you will place is pin 1. This is typically a square pin. The rest of the device pins will be round.

1. Click the **Add Pin** icon from the top menu.

The Options form displays fields for adding pins.

2. In the Options form, click in the Padstack field and enter:

60s38d

You will use this padstack to represent pin 1 of this device.

3. Press the **Tab** key to enter the padstack name.

The Allegro message area states:

```
Using '60S38D.pad'
```

This means that the Allegro program was able to locate the padstack you specified in the Options form. The padstack is now attached to your cursor.

4. To place pin 1, click the Allegro command line to activate it, then enter the following command:

x 0 0

The padstack for pin 1 is placed at the drawing origin (0,0) near the center of your work area.

5. Zoom in to the area around pin 1.

6. In the Options form, double click in the Padstack field and enter:

60c38d

This is the padstack that you will use to represent the remaining pins of this device.

7. Press **Tab**.

The Allegro message area states:

```
Using '60C38D.pad'
```

This means that the Allegro program was able to locate the padstack you specified in the Options form. The padstack is now attached to your cursor.

8. To add pins 2 through 7 in a column (under pin 1), double click in the Qty field for the **Y** direction, and enter:

6

	Qty	Spacing	Order
x:	1	100.0	Righ ▾
y:	6	100.0	Down ▾

9. Press **Tab**.

The Options form is now ready to place an array of 6 pins (1 column and 6 rows). The spacing between the rows is 100 mils. The first pin of the array will be pin 2 (see Pin #), followed by pin 3, and so on, in a *downward* direction (Down).

The Allegro tool is waiting for a location for the array of pins.

10. At the Allegro command line, enter:

x 0 -100

🗒 **Note**

The cursor must be in the Allegro window to enter data at the command line.

Since pin 1 is located at the drawing origin (0,0), the starting point for the array is (0, -100).

The array of 6 pins is placed, starting with pin 2, and progressing in a downward fashion.

11. To add another column of pins (8 through 14), double click in the Quantity field of the**Y** direction, and enter:

7

The Options form is now ready to place an array of 7 pins (1 column and 7 rows). The spacing between the rows is still 100 mils. The first pin of the array will be pin 8 (see Pin #), followed by pin 9 and so on, but the direction needs to be in an *upward* fashion.

12. To change the direction that the array expands, locate the **Order** box to the right of the Spacing fields (currently set to Down). Click the scroll button and change the order to **Up**.

The Allegro program is waiting for a location for the array of pins.

13. Click on the Allegro command line and enter:

x 300 -600

Since pin 1 is located at the drawing origin (0,0), the starting point for the array is (300, -600).

The array of 7 pins is placed, starting with pin 8, and progressing in an upward fashion.

Notice the pin numbers for pins 8 through 14 (to the left of their respective pins).

14. To make the pin numbers appear on the right side for pins 8 through 14, place the cursor in the work area and click right to select **Oops** from the pop-up menu. (Use the **Oops** command to undo a step when you make an error.)

Pins 8 through 14 are removed.

15. In the Options form, double click left in the **Offset x:** field and type:

100

You have changed the text position from -100 to a positive 100.

16. Press the **Tab** key to enter the new data from the Options form.

The Allegro tool is waiting for a location for the array of pins.

17. Click the Allegro command line and enter the location of pin 8.

x 300 -600

Notice the pin numbers for pins 8 through 14 (now on the right side of their respective pins).

18. Click right and select **Done** from the pop-up menu.

Adding an Assembly Outline

To make the assembly graphics easier to draw, reduce the grid size in the work area (currently set to 100 mils).

1. Select **Setup > Grids** from the top menu.

The Grids Display form appears.

2. Locate the Non-Etch section at the top of the form. This is where you will make the grid spacing changes.

3. Double click in the Spacing: x: field and enter:

25

4. Double click in the Spacing: y: field and enter:

25

5. Click **OK** at the bottom of the form.

The work area now displays a 25-mil grid.

6. Click **Add > Line** from the top menu.

Notice the Options form states that the active class and subclass are PACKAGE GEOMETRY and ASSEMBLY_TOP. You add assembly graphics to this layer of the symbol drawing.

A typical assembly outline is a rectangle that surrounds all the pins of the device and contains some kind of "notch" showing part orientation.

7. Click to specify the corners of the rectangle.

As you move the cursor, you see the attached line. If you want to add a notch on the corner showing pin 1, be sure the line lock is set to **45**.

8. When your assembly outline is complete, click right and select **Next** from the pop-up menu.

Since you need to create the Silkscreen as a series of lines, you do not need to exit the **Add Line** command.

Adding a Silkscreen Outline

For the purposes of this lab, assume a typical silkscreen outline is a polygon that exists between the two columns of device pins. Notice that the Options form states that the active class and subclass are PACKAGE GEOMETRY and ASSEMBLY_TOP. You do not want to add silkscreen graphics to this layer of the symbol drawing.

1. In the Options form, click the scroll button to show the available subclasses and change ASSEMBLY_TOP to **SILKSCREEN_TOP**.

2. Click to specify the corners of the rectangle.

    A typical silkscreen outline is a polygon drawn inside the pads that has an orientation arc at one end. You may want to use the **Add > 3pt Arc** command.

3. To exit the **Add Line** command, click right and select **Done** from the pop-up menu.

Setting Colors

By default, all objects in a new drawing are set to the same color. To help differentiate between the assembly and silkscreen outlines, assign each of them a different color.

1. Click the **Color** icon.

    The Color and Visibility form appears.

2. Set the Group field to **Geometry**.

    Next you will change the ASSEMBLY_TOP subclass to green.

3. Click a color (green) in the Palette area of the menu, and assign it to the ASSEMBLY_TOP subclass, under the PACKAGE_GEOMETRY class.

4. Click another color (white), and assign it to the SILKSCREEN_TOP subclass.

5. Click on **OK** in the Color and Visibility form.

    The menu closes, and the symbol drawing displays the new color assignments.

Adding Labels

Use labels to display logical information about a device (reference designator, device type, value and tolerance data if applicable). The label is simply a location placeholder.

1. Select **Layout > Labels > RefDes** from the top menu.

   You can also use the **refdes** icon to add labels.

   Notice the Options form states that the active class and subclass are REF DES and ASSEMBLY_TOP. You want to add text to this layer.

   The Allegro message area prompts you to:

   ```
   Pick text location
   ```

2. Click under the device (inside the assembly outline).

   The Allegro message area prompts you to:

   ```
   Enter text string.
   ```

3. Enter:

   U*

   When entering a designator text string, remember these three important characteristics:

   > Location

   > Orientation

   > Text Size

   Control these characteristics using the Rotate and Text Block fields in the Options form.

4. Click right and select **Done** from the pop-up menu.

5. Select **Layout > Labels > Device** from the top menu.

6. Click under the device (near the refdes label).

7. Enter:

   devtype

8. Click right and select **Done** from the pop-up menu.

   This is where the reference designator and device type will appear during board layout. This data will appear in the orientation and size represented by these placeholder labels. The actual text used for this string is insignificant and will be replaced when logic data is imported.

You now have reference designator and device type labels for the assembly layer. You should add a reference designator label for the silkscreen layer also.

9. Select **Layout > Labels > RefDes** from the top menu.

   Notice that the Options form shows that the active class and subclass are REFDES and ASSEMBLY_TOP. You do not want to add the text to this layer of the symbol drawing.

10. In the Options form, change the subclass to **SILKSCREEN_TOP**.

    Notice the prompt on the Allegro command line that says:

    ```
    Pick text location.
    ```

11. Click above the device outline so that the silkscreen text will be in a visible location *after* the components are installed.

12. Enter:

    U*

13. Click right and select **Done** from the pop-up menu.

    This is where the silkscreen reference designator will appear. The Allegro software's automatic silkscreen optimization may move this location slightly, but you have designated a starting point for this text.

Creating a Package Boundary

The DRC program uses the package boundary to make sure a package does not overlap another package or any other objects that can cause a problem (package keepout areas, and so forth).

If you do not create the package boundary, it will be created for you when you use the **Make Sym** command.

1. Select **Setup > Areas > Package Boundary** from the top menu.

2. Set the Class and Subclass fields in the Options form to **PACKAGE GEOMETRY** and **PLACE_BOUND_TOP** if necessary.

3. Click to draw a polygon representing the area required for placement. Most commonly, this is an outline that is outside all of the pins.

   When you close the polygon, it is automatically filled solid.

Defining the Package Height

The DRC program uses package height to make sure a package does not violate a height-restricted area of the board.

It is not necessary to define the package height for every device. The Allegro tool uses the Drawing Options form to define a default package height for all symbols. To override this default package height, you need to create a package boundary, then attach a height value to the boundary.

1. Select **Setup > Areas > Package Height** from the top menu.

2. Set the Class and Subclass fields in the Options form to **PACKAGE GEOMETRY** and **PLACE_BOUND_TOP** if necessary.

   Notice the prompt in the Allegro message area that says:

   ```
   Select or add package shape.
   ```

3. Click on the package boundary you just created (filled polygon).

   The package boundary is highlighted. The Allegro message area prompts:

   ```
   Enter package PACKAGE GEOMETRY/PLACE_BOUND_TOP height.
   ```

4. In the Max height: field of the Options folder tab, enter:

   180

   The package height is 180 mils.

5. To exit the **Package Height** command, click right in the Allegro workspace and select **Done** from the pop-up menu.

   The package boundary is a 2-D polygon. When height data is attached to this polygon, the DRC program evaluates the package boundary as if it were three dimensional.

   This package now contains explicit height information that will override the default height specification contained in the Drawing Status form.

Saving the Symbol to Disk

1. Select **File > Create Symbol** from the top menu.

   A create symbol form appears, showing the name of the package symbol as '*dip14*'.
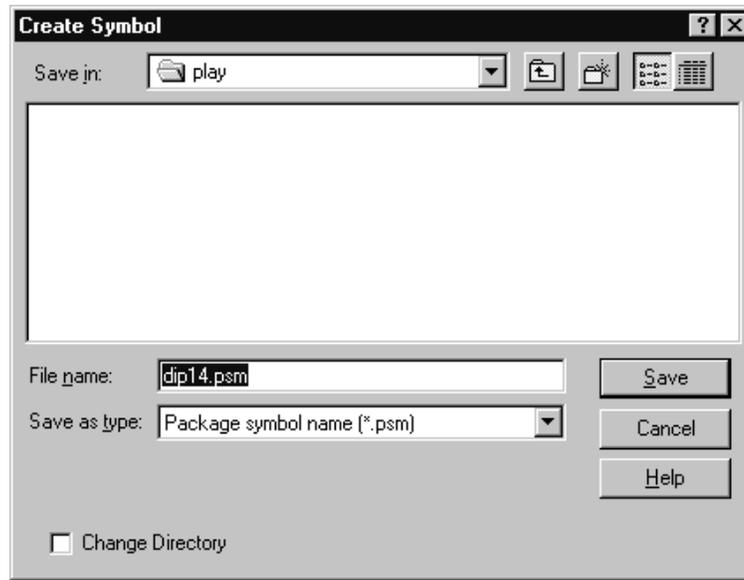
2.   Click on **Save** to accept the current name.

The Allegro message area confirms symbol *dip14.psm* has been created
on disk. This file is used in the design process during component
placement.

3.   Select **File > Save** from the top menu.

The Allegro message area confirms that *dip14.dra* was saved to disk.

**STOP** **End of Lab**

Lab 4-3: Creating an SOIC 16 with the Symbol Editor (*optional lab*)

Objective: Learn how to use the Symbol Editor to create package symbols.

This lab shows you how to create a package symbol for a 16-pin small outline package (SOIC). You will be using the surface-mount padstack you created to represent the pins of this device.

Naming the Symbol

1. Select **File > New** from the top menu.

   The New Drawing dialog box appears.

2. Type the following name in the Drawing Name field:

   soic16

3. Select **Package Symbol** from the scrolling list of drawing types, as shown below:
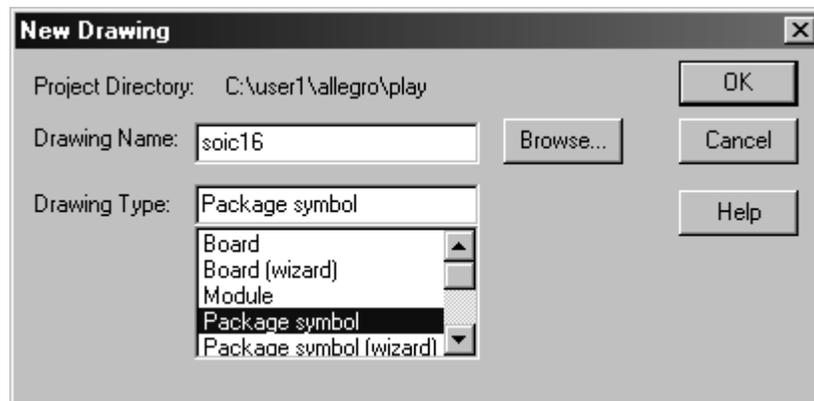
4. Click **OK** to close the New Drawing dialog box.

5. Select **Setup > Drawing Size**

   The Drawing Parameters form appears.

   Notice that all the previous settings have been retained.

6. Click **OK** to close the New Drawing form.

Setting the Grid

Because device pins are on 50-mil centers, change the grid from its default setting of 100 mils.

1. Select **Setup > Grids** from the top menu.

   The Grids Display form appears.

2. Locate the Non-Etch section at the top of the form. This is where you will make the grid spacing changes.

3. Double click in the Spacing: x: field and enter:

   25

4. Double click in the Spacing: y: field and enter:

   25

5. Click on **OK** at the bottom of the form.

Adding Pins

This device contains two columns of 8 pins. The spacing between the pins in each column is 50 mils. You will place pins 1 through 8 as one array (column), followed by pins 9 through 16 in a second array.

1. Click the **Add Pin** icon in the top menu.

The Options form displays fields for adding pins.

2. In the Options form, select the **"..."** button next to the empty field for Padstack.

   A Package Symbol Wizard padstack browser appears.

3. Select the padstack **76x24smd** (case is unimportant). This is the padstack that will represent the pins of this device.

4. Click **OK**.

   The Allegro message area states:

   ```
   Using '76X24SMD.pad'
   ```

   This means that the Allegro tool was able to locate the padstack you specified in the Options form. It is now attached to your cursor.

5. To add pins 1 through 8 in a column, double click in the Qty field for the **Y** direction, and enter:

   8

6. Press **Tab**.

The Options form is now ready to place an array of 8 pins. But the spacing between the rows is set to 100 mils by default. This needs to be changed.

7. Double click in the Spacing field for **Y**. (The X field is the spacing for columns, and the Y field is the spacing for rows.)

8. In the Y spacing field, enter:

   50

9. Press **Tab**.

   The first pin of the array will be pin 1 (see Pin #), followed by pin 2, and so forth, in a *downward* direction (Down).

10. Set the Y order to **Down**.

    The Allegro program is waiting for a location for the array of pins.

11. Click the Allegro command line and enter:

    x 0 0

    The array of 8 pins is placed, starting at the drawing origin and progressing in a downward fashion.

12. Zoom in to the area surrounding the pins you just placed.

13. To add another column of pins (9 through 16), change the direction for rows (currently set to Down), by setting the Y order field to **Up**.

14. To set the pin number text to the right of the respective pins, double click in the **Offset X:** field and enter:

    100

15. Press **Tab**.

    The Allegro tool is waiting for the start point for the array.

16. At the Allegro command line, enter:

    x 225 -350

    Remember that pin 1 is located at the drawing origin (0,0). The starting point for the array with respect to the drawing origin is (225, -350).

    The array of 8 pins is placed, starting with pin 9, and progressing in an upward fashion.

    Notice the pin numbers for pins 9 through 16 (to the right of their respective pins).

17. To exit the **Add Pin** command, click right and select **Done** from the pop-up menu.

Adding an Assembly Outline

1. Click on **Add > Line** from the top menu.

    The Options form states that the active class and subclass are PACKAGE GEOMETRY and ASSEMBLY_TOP. You add the assembly graphics to this layer.

    A typical assembly outline will be a rectangle that surrounds all the pins of the device.

2. Click to draw the corners of the rectangle.

3. To continue adding the Silkscreen, click right and select **Next** from the pop-up menu.

Adding a Silkscreen Outline

For this lab, assume a typical silkscreen outline is a polygon that exists between the two columns of device pins.

1. In the Options form, click the scroll button to show available subclasses and change ASSEMBLY_TOP to **SILKSCREEN_TOP**.

2. Click to draw the corners of the rectangle.

    A typical silkscreen outline is a polygon that contains some kind of "notch" showing part orientation.

3. To exit the **Add Line** command, click right and select **Done** from the pop-up menu.

Adding Labels

1. Select **Layout > Labels > RefDes** from the top menu.

    Before you add the label, we will change the orientation and text size.

2. In the Options form, change the setting in the Rotate field to **90**.

3. In the Options form, change the Text Block field to show a size of **2**.

    ### Note

    There are 16 text blocks, each corresponding to a different text size. You can select **Setup > Text Sizes** to see a table showing this information.

    The label is oriented vertically, and the text size is slightly larger.

4. Click under the device (within the assembly outline) to define a location for the text.

5. At the Allegro command line, enter:

    U*

6. Select **Layout > Labels > Device** from the top menu.

7. Click under the device (near the refdes label).

8. At the Allegro command line, enter:

    devtype

9. Click right and select **Done** from the pop-up menu.

    Now add a silkscreen label.

10. Select **Layout > Labels > RefDes** from the top menu.

11. In the Options form, change the subclass to **SILKSCREEN_TOP**.

12. Click outside the assembly outline to designate a text location.

13. Enter:

    U*

14. Click right and select **Done** from the pop-up menu.

    This is where the silkscreen reference designator will appear. The Allegro tools's automatic silkscreen optimization may move this location slightly but you have, at least, designated a starting point for this text.

Creating the Package Symbol and Drawing Files (.psm and .dra)

1. Select **File > Create Symbol** from the top menu.

    A create symbol form appears, showing the name of the package symbol as *soic16*.

2. Click on **Save** to accept the current *soic16* name.

    The Allegro message area confirms that symbol *soic16.psm* has been created on disk. This file is used in the design process during component placement.

3. Select **File > Save** from the top menu.

    The Allegro message area confirms that *soic16.dra* was saved to disk. This drawing file is stored in a library.

STOP **End of Lab**

Lesson 5:   Board Design Files

Learning Objectives

◆ Use the **Symbol Editor** to create board mechanical symbols.

◆ Use the **Layout Editor** to create master board designs.

Summary

In this section you will learn how to create board outlines or board mechanical symbols. Creating mechanical symbols can save you time when your designs use the same outline. Mechanical symbols will also improve the quality of the design, since the outline only needs to be checked once. After the outline has been verified, all designs using that outline will be correct.

Creating a Board Symbol
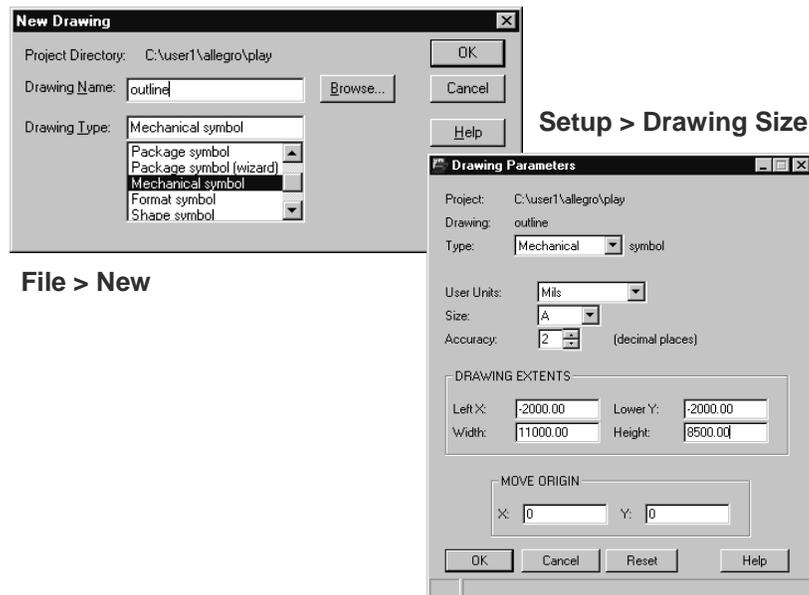
Setup > Drawing Size

File > New

More Information

To create a board symbol, select **Mechanical Symbol** as the drawing type.

Next, use the Drawing Parameters form to define the following:

Project is the current directory path name.

Drawing specifies the name of the mechanical symbol you are creating.

Type is mechanical (*.bsm*).

User Units can be Mils, Inches, Millimeters, Centimeters, or Microns. Default is Mils.

Size can be A, B, C, D or Other. (A1, A2, A3, A4 for metric units). The default is A.

Accuracy is the number of decimal places. Range is 0 - 2. The default is 1.

Move Origin section can be used to place the drawing origin inside the drawing area (to establish a mechanical datum point).

Typical Board Outline
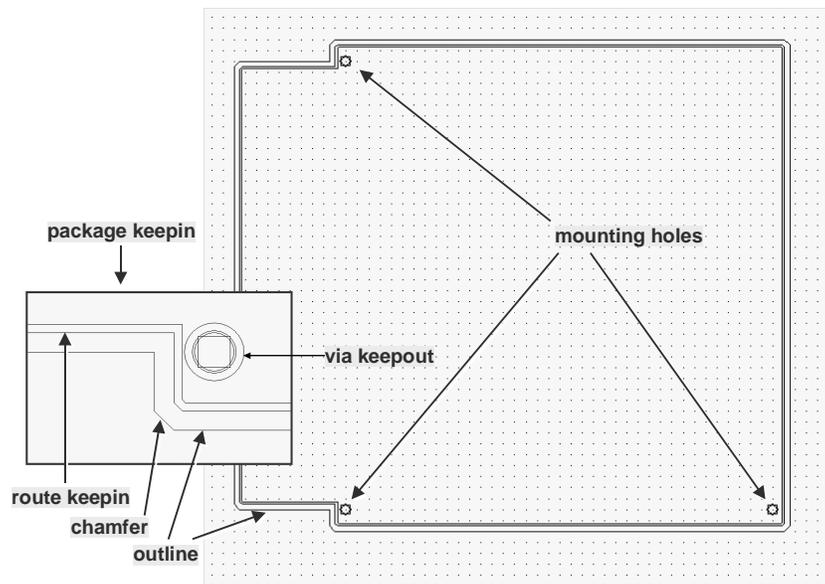
More Information

This is an example of a card outline with keepins, keepouts, and mounting holes.

To create an Allegro mechanical outline symbol:

1. Define the card outline.
2. Define mounting holes (added as pins).
3. Define package and routing keepin/keepout areas.

4. Create (save) the symbol file (*.bsm*).

5. Save the file (*.dra*).

Drawing a Board Outline
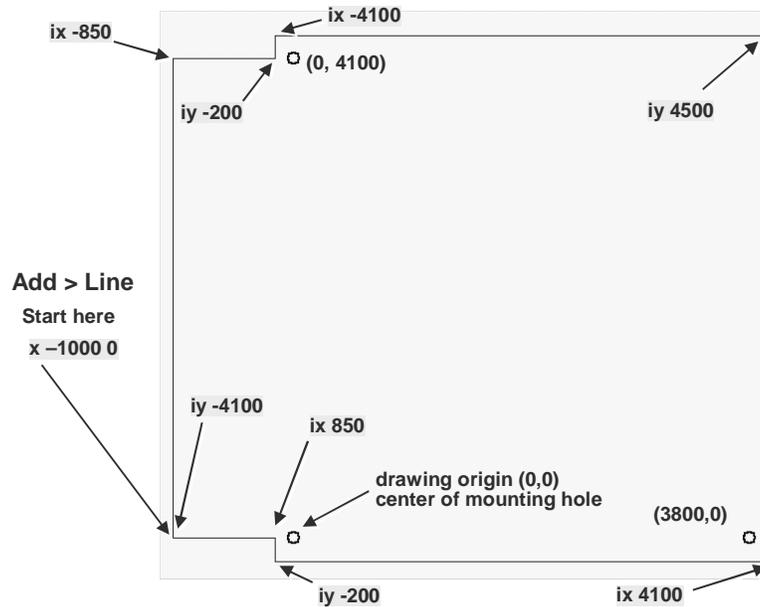
Summary

You define the card outline using the **Add Line** command to add lines and arcs on the OUTLINE subclass of the BOARD GEOMETRY class. You can select line endpoints with the left mouse button or by typing in coordinates at the Allegro command line. When you select line endpoints with the left mouse button, the selection will snap to the nearest grid point. When you type coordinates on the command line, you can enter them in either absolute coordinates by using the "x" command, or incremental coordinates by using either the "ix" or "iy" command.

You can use the "x", "ix" or "iy" commands at any time with any other command, such as routing, when adding vias, and so on.

More Information

You will probably use a mechanical drawing as your source of data. It might contain both absolute (reference to datum point) and relative dimensions. Use the Allegro command line to enter X, Y coordinates for line endpoints in absolute (x 1900 1800) or incremental (ix -900) mode.

Chamfering and radius corners can be performed with the **Dimension > Chamfer** and **Dimension > Fillet** commands to redefine the corners while in the Geometry toolset.

Dimensioning utilities are also available from the top menu bar while in Mechanical Symbol mode.

## Tooling/Mounting Holes

Layout > Pins   or
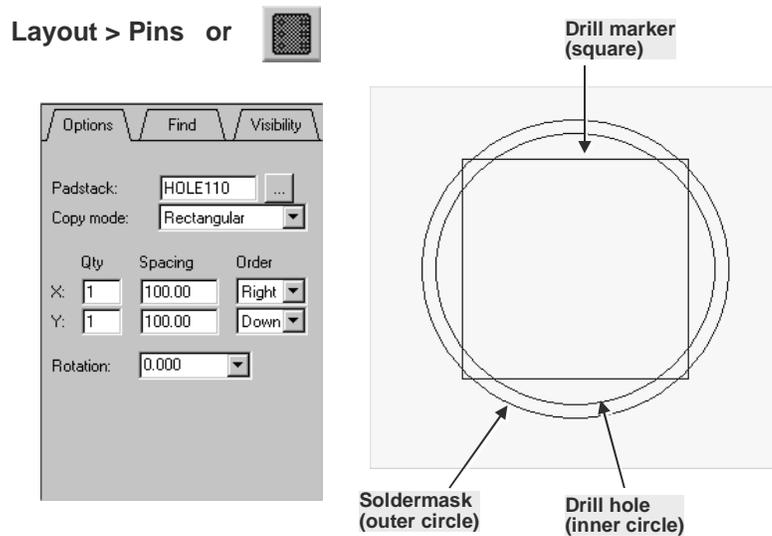
More Information

You add tooling holes and mounting holes into your board outline using the same command as adding pins into your footprints. However, when adding mounting holes and tooling holes, you will notice that in the Options folder tab there is no field for the pin number. You cannot assign pin numbers to these types of holes. Since you cannot add pin numbers, you cannot assign a net name to these holes either.

If you wish to assign a net name to a tooling hole or mounting hole—possibly for grounding reasons—you will have to create the mounting hole as a one pin component.

Chamfers

Dimension > Chamfer
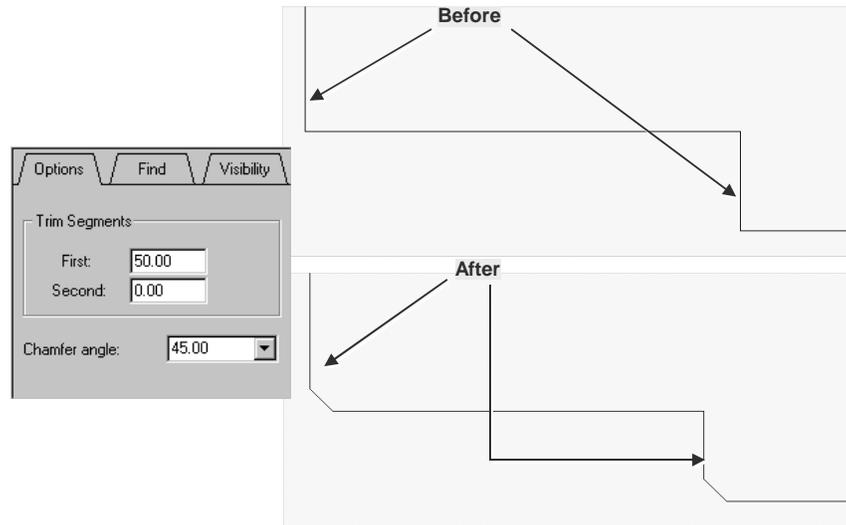
More Information

Even though the **Chamfer** command is located under the Dimension menu, you can still use this command to chamfer the corners of your board outline. If you need rounded corners, use the **Fillet** command located in the same menu chain.

Linear Dimensioning
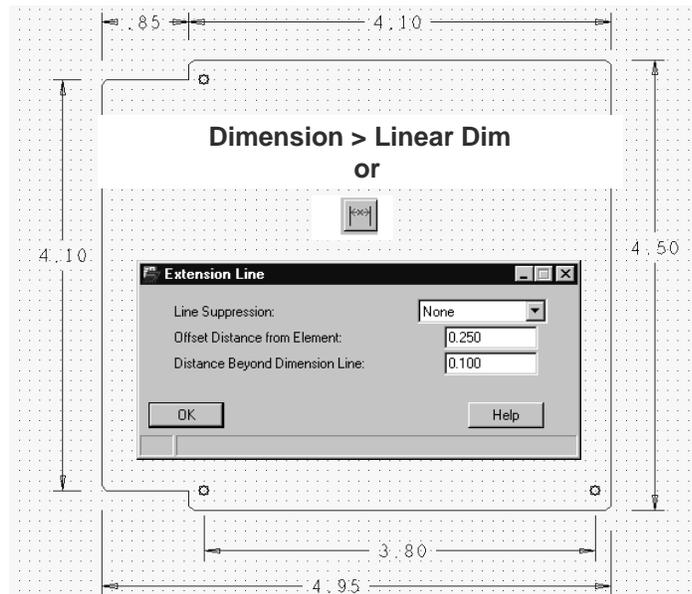
More Information

There are MANY different options available for dimensioning your design. The main menu option Dimension contains all of the dimension commands. The Parameters option allows you to set what type of dimensioning you will be doing, how the dimensions will look, and so on. By default, all dimensions are created on the BOARD GEOMETRY class, DIMENSION subclass.

Defining Constraint Areas (Keepins/Keepouts)

Setup > Areas…

Edit > Z-Copy Shape
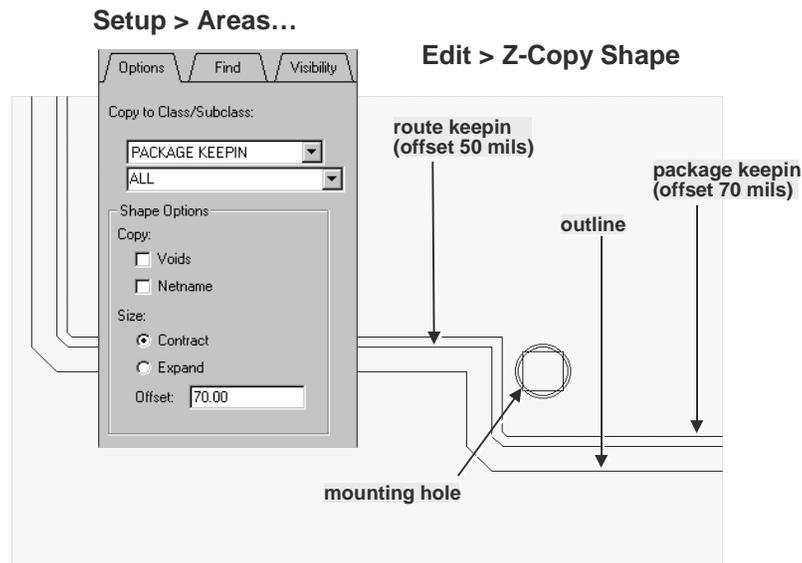
More Information

You define the keepin and keepout areas using the selections in the Setup-Areas pull-down menu. There are many different keepin and keepout areas that can be defined. Some of these are:

Route Keepin - User-defined route keepin, drawn as a polygon, defines the allowable area for routing. Defined for all etch layers at once.

Route Keepout - User-defined route keepout, drawn as a polygon, defines the avoidable area for routing. Defined for any etch layer or all at once.

Package Keepin - User-defined package keepin, drawn as a polygon, defines allowable area for placement. Defined for all placement layers at once.

Package Keepout - User-defined package keepout, drawn as a polygon, defines the avoidable area for placement. Defined for top, bottom, or both layers at once.

Via Keepout - User-defined via keepout, drawn as a polygon, defines the avoidable area for vias. Defined for any etch layer or all at once.

Package Height - Attached to a Package Keepout area. Converts the 2D area into a 3D keepout. If only one value is given, DRC assumes Max Height value is infinite. Defined for Top, Bottom, or All.

Saving Board Symbol Files (.bsm and .dra)

File >

New...	Ctrl+N
Open...	Ctrl+O
Save	Ctrl+S
Save As...	
Create Symbol...	
Import	▶
Export	▶
Viewlog...	
File Viewer...	
Plot Setup...	
Plot Preview...	
Plot...	
Properties...	
Change Editor...	
Script...	
Exit	

.bsm

+

.dra
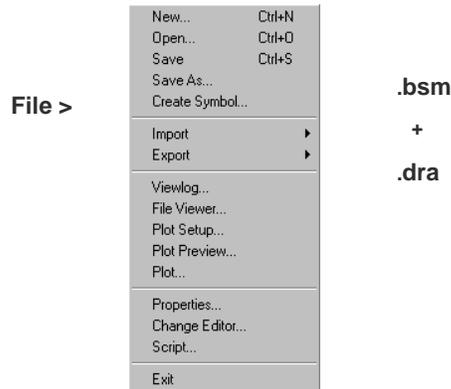
IMPORTANT: Save as *both* types of file.

More Information

Saving the *.bsm* File

Once your drawing is complete, you can make a board symbol file (*.bsm*). This file is the binary equivalent of your drawing file. Use this file to represent the mechanical layout of your design (outline, restricted areas, and mounting holes).

It is not mandatory to create a board symbol for every design, but if board outlines are similar from one design to the next, using a board symbol can eliminate duplication of work. You may want to maintain a library of board symbols if several types are used repeatedly.

Use **File > Create Symbol** to generate the *.bsm* file.

Saving the *.dra* File

The binary board symbol file (*.bsm*) cannot be viewed or edited. You can only open the drawing file (*.dra*). Therefore, you must save the drawing file to disk, and keep it in the library directory in the event you need to make a revision.

Use **File > Save** to generate the *.dra* file.

Note

Save both the *.bsm* and the *.dra* files. You can extract these files from an archived design, but you should keep both files available during the current project.

Lab

◆ Lab: Creating a Board Mechanical Symbol
- Name the symbol.
- Set the grid.
- Create the board outline.
- Change your working directory.
- Add tooling holes.
- Chamfer corners.
- Include linear and chamfer dimensions.
- Add placement and routing keepin and keepout areas.
- Add via keepout areas.
- Create and save the mechanical symbol (.bsm) and drawing (.dra) files.

More Information

The following lab will allow you to familiarize yourself with the process required to create a board mechanical symbol. Items covered include creating the board outline, adding tooling and mounting holes, adding keepins and keepouts and so on.

Lab 5-1:   Creating a Board Mechanical Symbol

Objective: Learn to use the Symbol Editor to create mechanical drawings.

In this lab you will create a mechanical symbol to match the following design and dimensions.
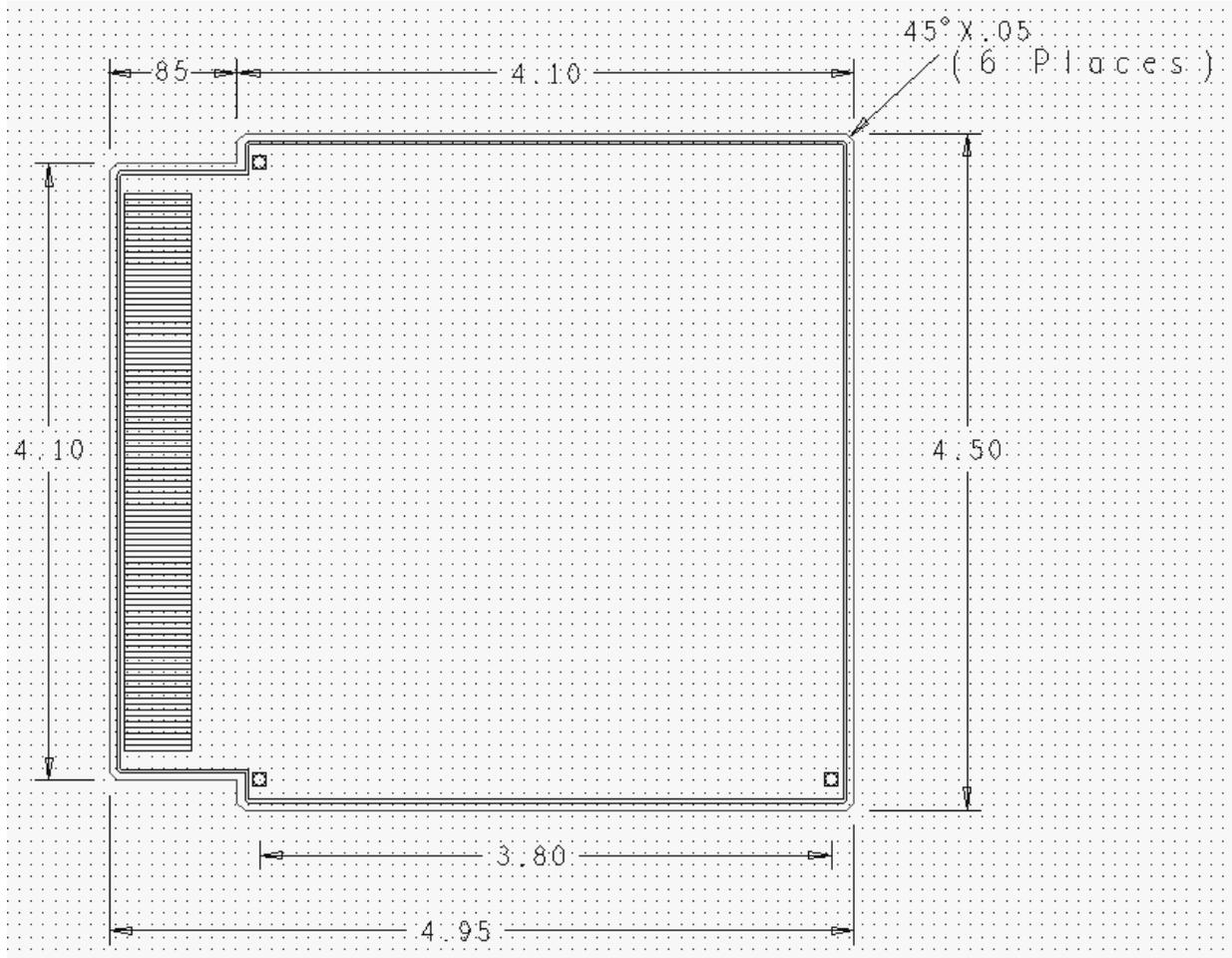
Naming the symbol

1. Choose **File > New** from the top menu.

   The New Drawing dialog box appears.

2. In the Drawing Name field, type the following name:

   outline

3. Choose **Mechanical Symbol** from the scrolling list of drawing types, as shown below.
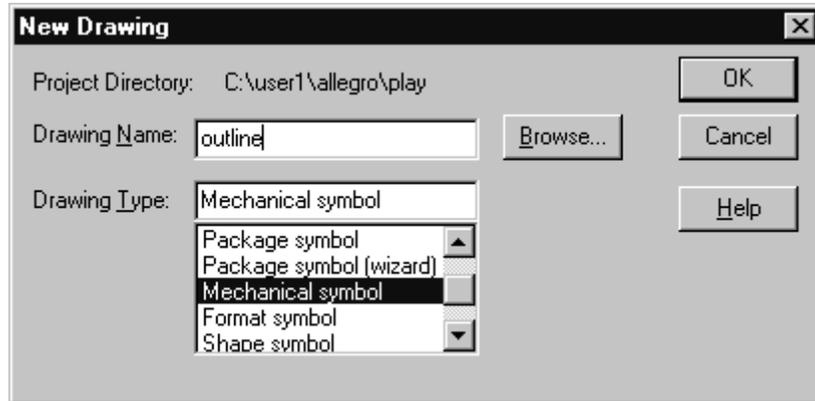
4. Click **OK** to close the New Drawing dialog box.

5. Choose **Setup > Drawing Size** from the main menu.

    The Drawing Parameters form appears.

    Notice that all your previous settings are retained. If you typed a value
    in the Move Origin section, it would cause cumulative results. An
    easier method for setting the origin point for this instance is to change
    the coordinates in the Drawing Extents fields.

6. Change the Drawing Extents fields to match the values in the following
    figure.

These settings cause the drawing origin to be placed 2 inches (2000 mils) up and to the right of the lower left corner of the drawing.

7. Click **OK** to close the Drawing Size form.

Setting the Grid

1. Choose the **Setup > Grids** item from the top menu.

The Grids Display form appears.

2. In the **Non-Etch** section at the top of the form, make the following spacing changes.

   a. Click in the Spacing: x field and enter: **25**

   b. Click in the Spacing: y field and enter: **25**

3. Click **OK** at the bottom of the form.

Creating the Board Outline

As indicated in the mechanical drawing at the beginning of this lab, the datum (0,0) point for this outline is the center of the lower left mounting hole.

1. Choose **Add > Line** from the top menu.

2. In the Options form, set the active class and subclass to
   BOARD GEOMETRY / OUTLINE if necessary.

3. At the Allegro command line, type each of the following sets of values
   and press **Enter** after each entry. You might want to use the following
   series as a checklist to keep track of which line segments you have
   entered:

   x -1000 0

   ix 850

   iy -200

   ix 4100

   iy 4500

   ix -4100

   iy -200

   ix -850

   iy -4100

4. Right click and choose **Done** from the pop-up menu. Your outline
   should look like the outline in the figure.

First point of outline placed here (-1000,0)
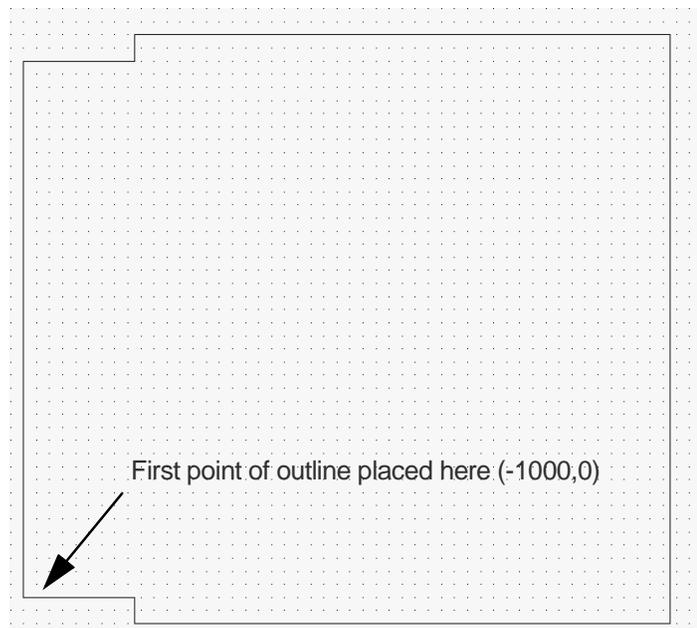
Adding Tooling Holes

In this part of the lab, you will add three holes. To define these tooling and
mounting holes within a mechanical symbol drawing, you must add them
as pins (padstacks).

1. Click the **Add Pin** icon in the top menu.

   The Options form displays fields for adding pins.

2. In the Options form, click in the Padstack field, then enter:

   hole110

   This is the padstack that will represent the mounting holes on this board.

3. Press the **Tab** key.

   The Allegro message area states:

   ```
   Using 'HOLE110 pad'.
   ```

   This means that the Allegro tool was able to locate, in the *solutions* directory, the padstack you specified in the Options form. The hole110 padstack is now attached to your cursor.

4. In the Allegro command line, enter the following data:

   x 0 0

   x 3800 0

   x 0 4100

5. Right click and choose **Done** from the pop-up menu.

   Three tooling holes are now placed within the board outline. Your outline should look like the figure below.

Three tooling holes placed
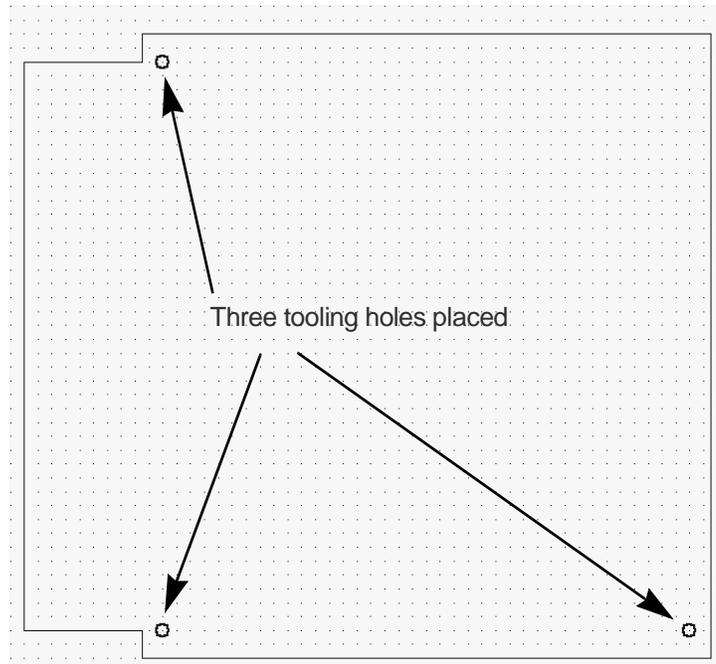
Chamfering Corners

You will now use a drafting process to add 45-degree chamfers to the corners of the board outline. Then you will add dimensions to the mechanical part.

1. Zoom to display the lower left corner of the board outline, then choose the **Dimension > Chamfer** menu option.

The Options form changes to show trim segment and chamfer angle settings. The drawing at the beginning of this lab showed a requirement for 50-mil chamfers.

2. In the Trim Segments section of the Options form, change the First segment trim size to 50, as shown.
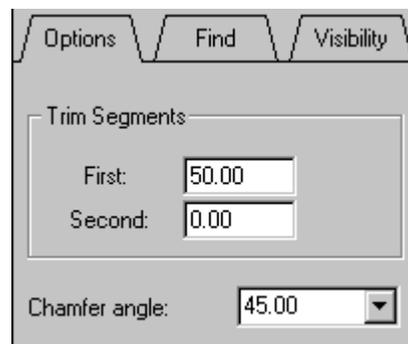
The Allegro message area prompts:

    Pick first segment to be chamfered.

3. Click on the lower left vertical edge of the board outline, as shown in the figure:
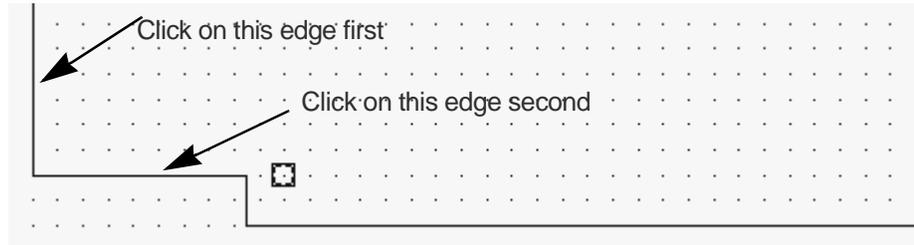
The Allegro message area prompts:

```
Pick second segment...
```

4. Click on the lower adjacent horizontal edge of the board outline.

The lower left corner (where the two line segments you selected intersect) is trimmed, as shown in the figure. It is not important which edge you select first.
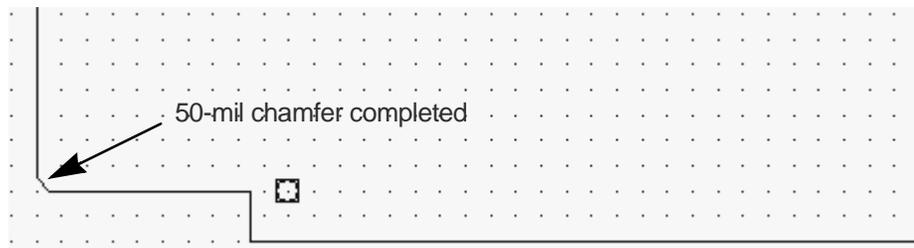
5. Continue adding chamfers to the remaining outside corners of the outline, as shown in the mechanical drawing at the beginning of the lab. Your outline should have a total of six chamfers.

Note

The procedure for adding fillets ("rounded corners") is the same as for adding chamfers.

6. When you are finished making the chamfers, right click and choose **Done** from the pop-up menu.

Adding Linear Dimensions

To ensure extension lines don't run into each other, you first need to set dimension parameters, then place the dimension boxes.

1. Choose the **Dimension > Parameters** menu item.

The Drafting dialog box appears.

2. Click **Extension Lines** and complete the Extensions dialog, as shown in the figure.
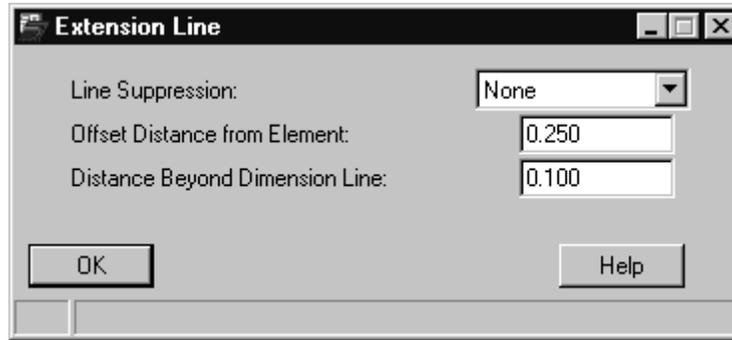
3. Select **OK** to close the Extension Line form.

4. Select **OK** to close the Drafting form.

5. Pan to view the bottom half of the board, then click the **Dimension Linear** icon from the toolbar.

The message window prompts you to pick a point or element to dimension. Notice that the Active Class and Subclass in the Options form have changed to BOARD GEOMETRY and DIMENSION.

Note

You may want to set the color of the DIMENSION subclass to white or some other bright color.

6. Click on the left edge of the outline, near the chamfer corner, as shown below.

A marker is placed at the vertex on the left edge, as shown.

Marker placed here after first click
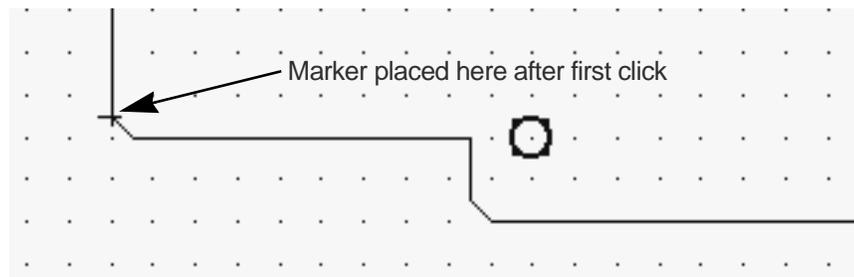
Note

As long as you click *within* a grid point spacing of a vertex, dimensioning will snap to the vertex. If you click more than a grid point spacing away from a vertex, Allegro assumes you want to dimension the *entire* segment between vertices.

The message window prompts you to pick a location for the dimension value.

7. Click anywhere on the right edge of outline. Be sure to make sure you select on the board outline. You may want to zoom in some to make sure you get the board outline and not a grid point.

   The message prompts you to indicate X or Y direction first. This is the direction in which you want to lay out the dimension extension lines.

8. To display the dimension box, move your cursor down and to the left, to a location just outside the board outline and centered between both edges of the outline, as indicated in the figure below, and click.
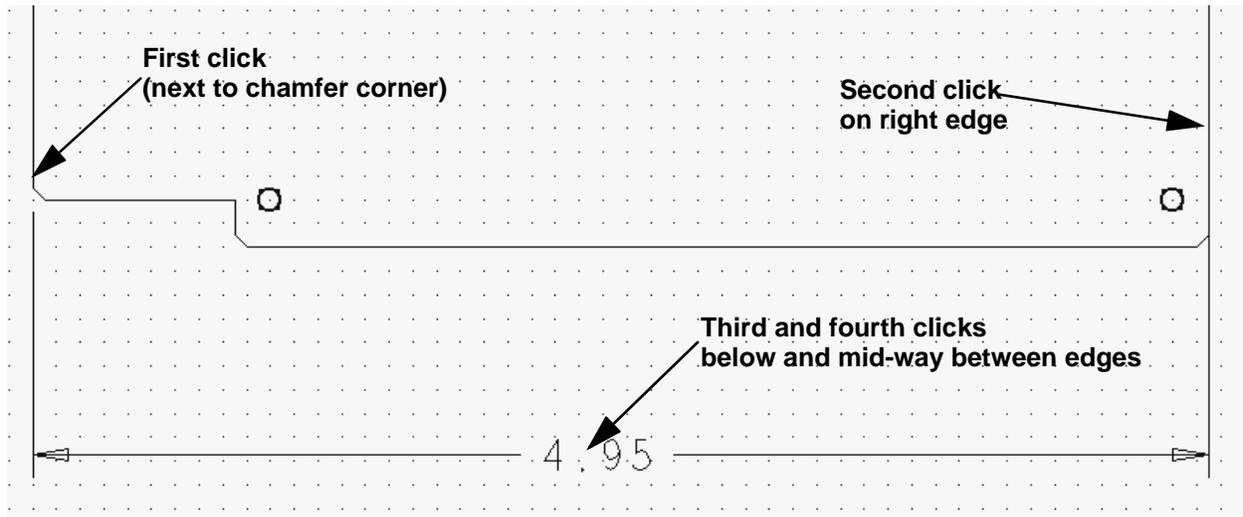

As you do so, notice the extension lines and dimension box highlighted in white. When you click the value 4.95 is automatically calculated and appears. The message prompts you to pick a location to place the dimension value.

9. Click to place the dimension box.

   The dimension 4.95 inches, with arrows to the left and right, is placed at the point where you have clicked.

10. Following the same procedure as you used in steps 2 through 5, place the following dimensions, as shown in the figure.
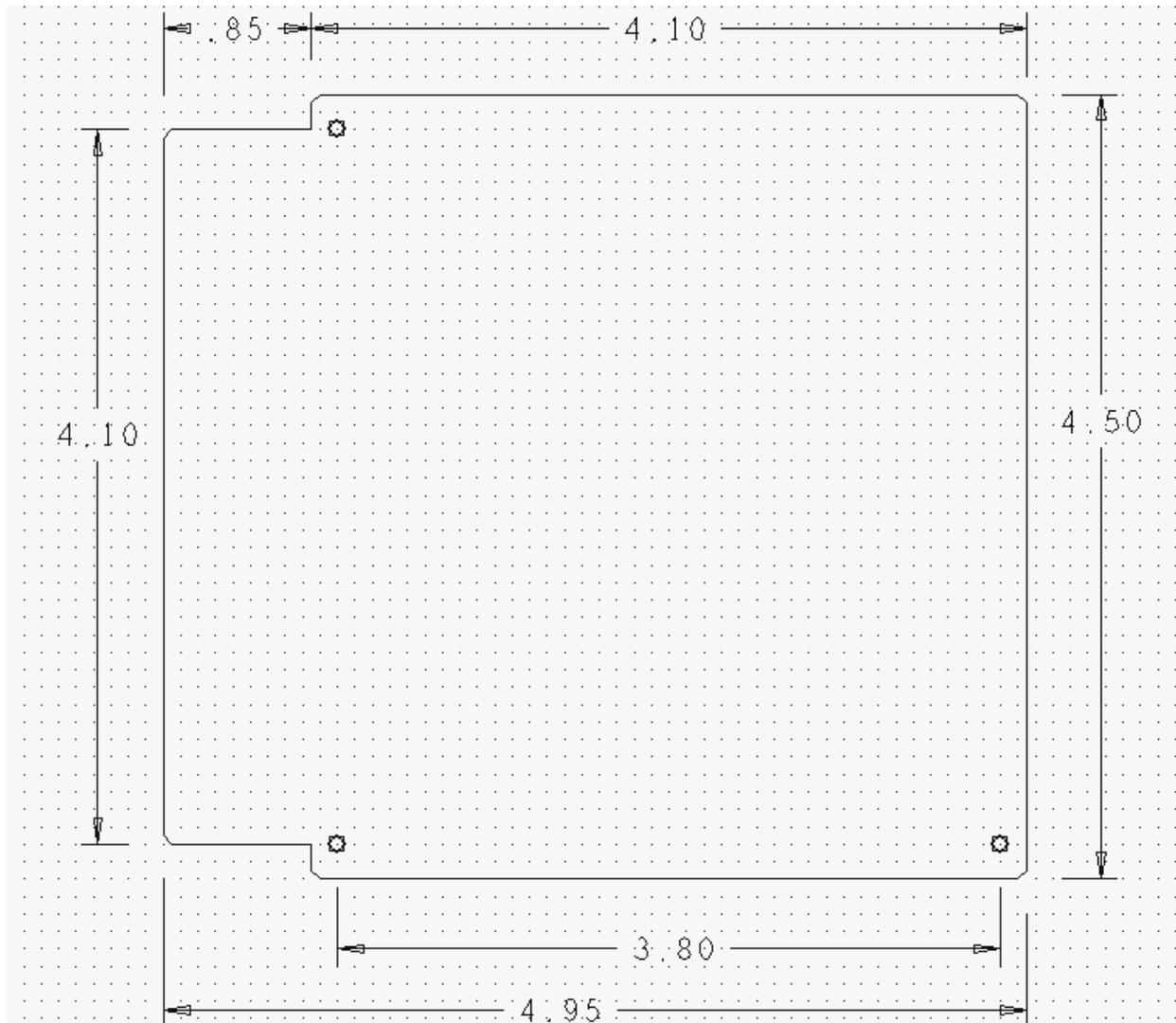
11. When you are finished, right-click and choose **Done** from the pop-up menu.

Dimensioning a Chamfer

1. Zoom in to the chamfer at the upper right corner.

2. Choose **Dimension > Chamfer Leader** from the top menu.

3. Click on the 45-degree chamfer line.

The dimension text is attached to your cursor.

**4.** Pull the cursor up and to the right, then click to create a leader line.

The leader line is the line between the dimension text and the 45-degree chamfer. Be sure to pull the text away from corners on the leader line. The line is automatically shortened by half the width of the text.

5. Right click and choose **Done**.

Your chamfer dimension should look like the figure.
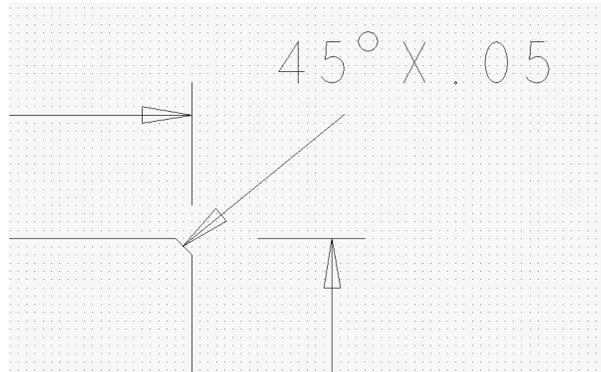

6. To place the final note text specifying the number of chamfers on the board, choose the **Add > Text** menu item. Fill in the text parameters to match those in the figure:
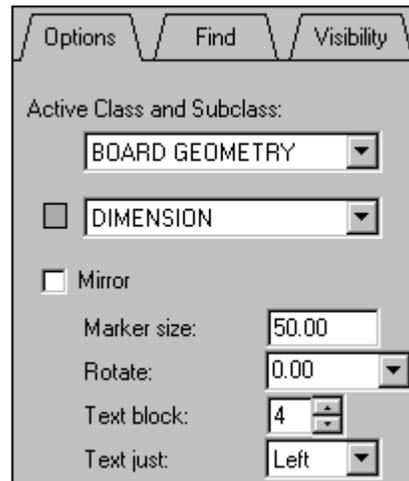
7. Place the text as shown in the figure, then right click and choose **Done** from the pop-up menu. Pay close attention to the command line for prompts as to which action to perform.
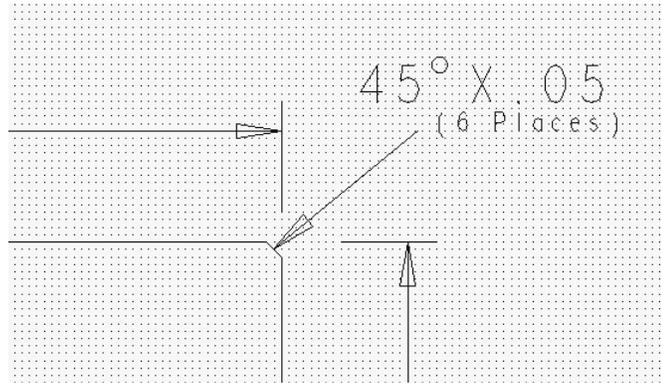
Note

You can view the Drafting and Dimensioning section of the online help files for more information about this and related topics.

## Adding Placement and Routing Keepin Areas

In this part of the lab, you will create package and route keepin areas to define the available board areas that you can use for part placement and signal routing.

1. Zoom to view the entire board.

2. Choose **Edit > Z-Copy Shape** from the main menu.

   The message window now prompts you to enter a selection point.

3. In the Options form, set your Active Class and Subclass to **PACKAGE KEEPIN** and **ALL**.

4. Under Shape Options, set the Offset to **70** and enable the **Contract** option.

5. Select on the board outline.

   A place keepin is drawn 70 mils inside the boundary of the board outline.

6. In the Options form, this time set your Active Class and Subclass to **ROUTE KEEPIN** and **ALL**. Under Shape Options, set the Offset to **50** and make sure the **Contract** option is enabled.

7. Select a point on the board outline.

   A route keepin is drawn 50 mils inside the boundary of the board outline. Your board outline should resemble the following figure.
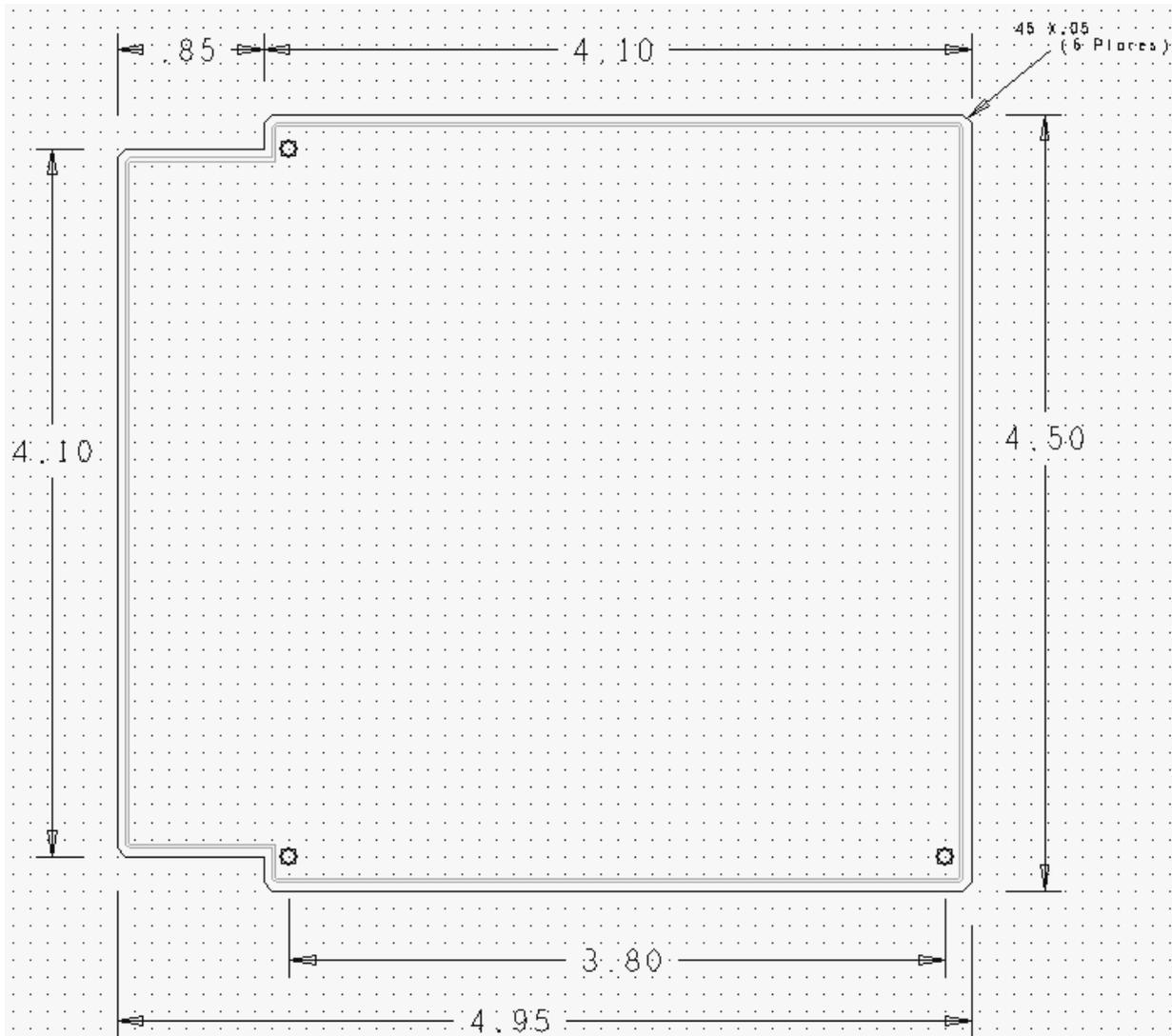
8. Right click and choose **Done**.

Adding Placement and Routing Keepout Areas

In this part of the lab, you will use package and route keepouts to exclude areas of the board for part placement or tracks. Generally, this would include areas inside the previously created keepins (such as holes or cutouts in the board).

You use the **Setup > Areas > Package Keepout** and **Setup > Areas > Route Keepout** commands from the top menu to create the keepout areas (closed polygons). During this exercise you will create temporary keepouts for demonstration purposes only. You will then delete them.

> **Note**
>
> The Allegro tool recognizes keepins and keepouts as shapes.
> Keepins are unfilled shapes, while keepouts are filled.

1. Choose **Setup > Areas > Package Keepout** from the top menu.

2. Click to set the vertices of a polygon shape in the center of the board.

    When the polygon is closed, it is automatically filled solid.

3. Right click and choose **Done** from the pop-up menu.

    This filled polygon represents an area that must be free of parts, a
    package keepout. The process for creating a route keepout areas is very
    similar.

4. Zoom into the area around the mounting hole at the bottom right of the
    board.

5. Choose **Setup > Areas > Route Keepout** from the top menu.

    The Allegro message area prompts you to enter a shape outline.

6. Set the parameters in the **Options** tab as shown in the figure. These
    settings allow you to create a circle as a line figure comprising four 90-
    degree arc segments.
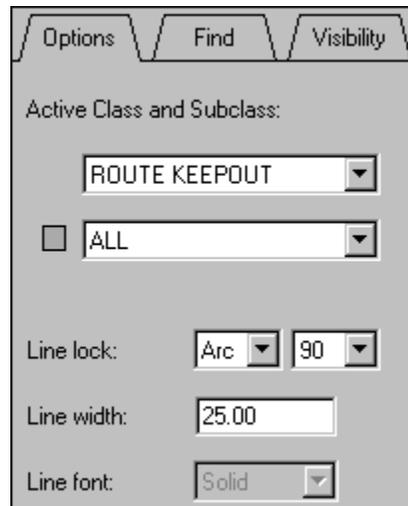
7. Complete a circle shape around the mounting hole by clicking at 5
    points to create 4 arcs, as shown in the figure.
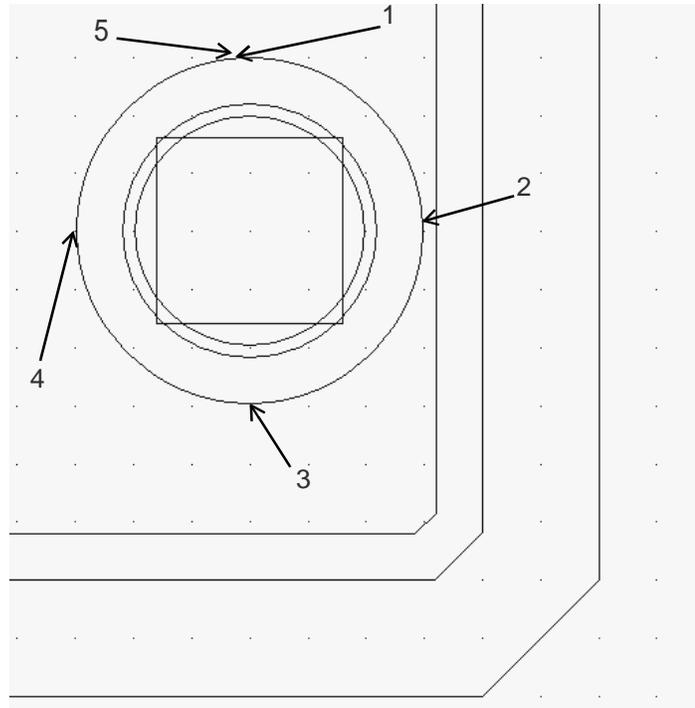
The circle fills in to complete the route keepout shape when you reach the initial starting point.

8. Right click and choose **Done** from the pop-up menu.

9. Choose **Edit > Delete** from the top menu.

10. Be sure that only **Shapes** is checked in the Find Filter, then click twice on both the polygon and circle you just created. Zoom in and out as needed.

The package keepout and route keepout are deleted. No package or route keepout areas are required for this mechanical symbol.

11. Right click and choose **Done** from the pop-up menu.

Adding Via Keepout Areas

In this design, you create a via keepout area to prevent vias from being routed in the region of the plug-in connector.

1. Choose **Setup > Areas > Via Keepout** from the top menu.

The Allegro message area prompts you to enter a shape outline.

2. In the Options tab, set the Line Lock option to **Line**.

3. At the Allegro command line, enter each of the following sets of values:

x -900 200

x -450 3900

4. Right click and choose **Done** from the pop-up menu.

The polygon fills solid and closes automatically. The complete board outline is shown in the figure.
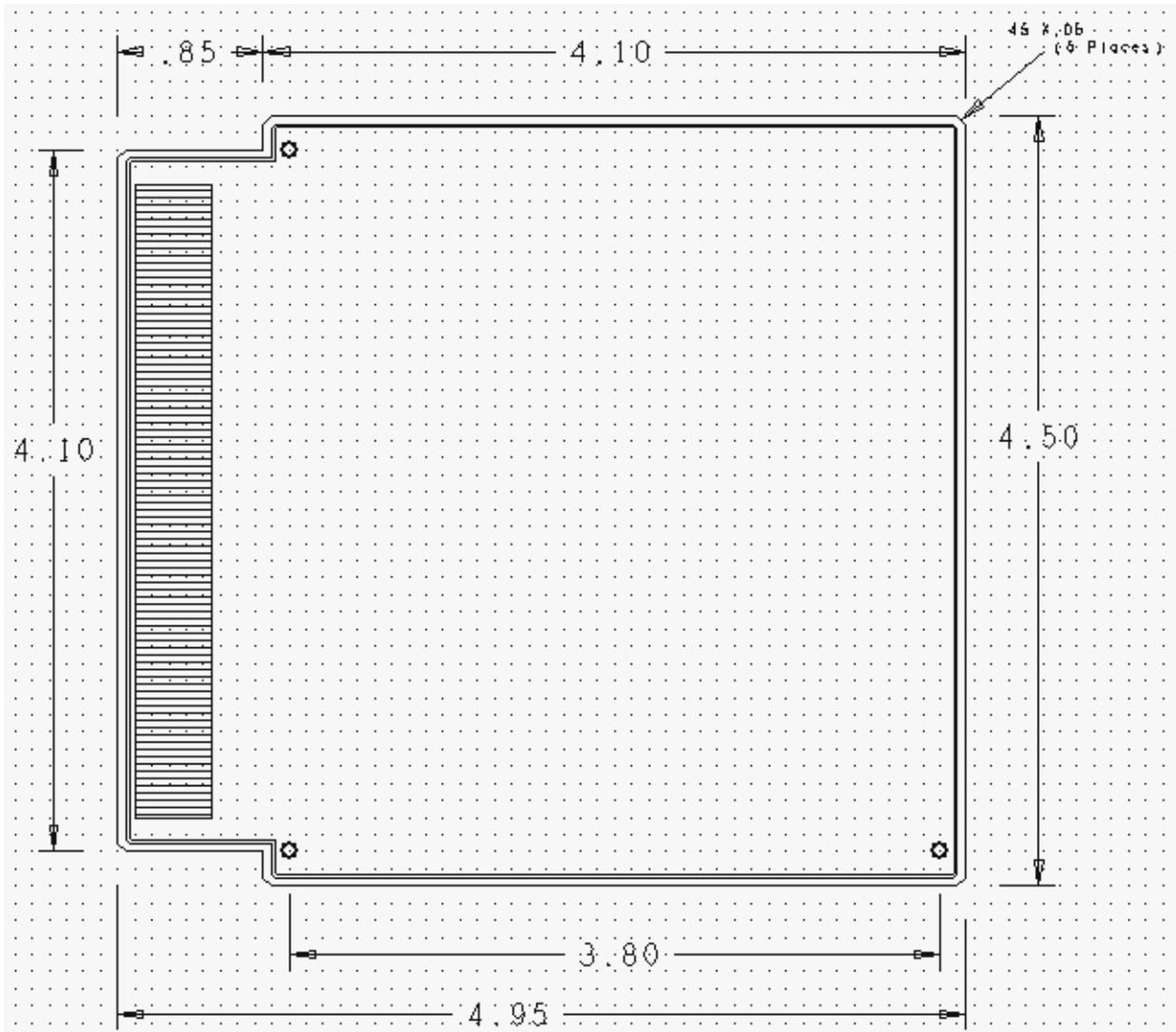
Note

The Allegro tool considers keepout areas as filled shapes. When you choose **Done**, the tool creates a shape boundary line from your last specified point back to the start point (in order to automatically close the polygon).

Creating the Mechanical Symbol and Drawing Files

1. Choose **File > Create Symbol** from the top menu.

A Create Symbol form appears, showing the name of the package symbol as *outline.bsm*.

2. Click **Save** to accept the current symbol name.

The Allegro message area confirms that the symbol *outline.bsm* has been created on disk.

This file is used in the design process during component placement.

3. Choose **File > Save** from the top menu.

The Allegro message area confirms that *outline.dra* has been saved to disk. You can also store this drawing file in a library.

STOP **End of Lab**

Board Wizard

Use the Board Wizard to create a starting board:

◆ Define the drawing units, size and origin.

◆ Define either a rectangular or round board outline.

◆ Define the grid spacing.

◆ Define the layer stackup.

◆ Define the initial constraints.

More Information

The Board Wizard can be used to quickly create a starting point for your design. You can define the standard drawing parameters such as units, drawing size and so forth. You can also define the cross section of the design which consists of routing layers and plane layers. The initial design constraints of minimum line width, line-to-line spacing, line-to-pad spacing, and pad-to-pad spacing—along with the default via padstack—can also be defined.

The supported board outline shapes are square, rectangular and round.

After running the board wizard, you can edit and modify any of the items created by using the standard Allegro user interface.

Lab

◆ Creating a Board using the Board Wizard

■ Use the Board Wizard to create a simple starting board.

More Information

The following lab will allow you to familiarize yourself with the process of creating a starting board using the Board Wizard.

Lab 5-2:   Creating a Board using the Board Wizard

Objective: Learn to use the Board Wizard to create the starting point of a design.

This lab shows you how to create a board mechanical symbol for a rectangular board outline that is 5 inches by 7 inches. The routing keepout will be 50 mils inside the outline, and the placement keepout will be 100 mils within the outline. A default trace width of 5 mils will be used, and all clearances will be set to 5 mils.

Naming the Symbol

1. Select **File > New** from the top menu.

    The New Drawing dialog box appears.

2. Type the following name in the Drawing Name field:

    testmech

3. Select **Board (wizard)** from the scrolling list of drawing types, as shown below:
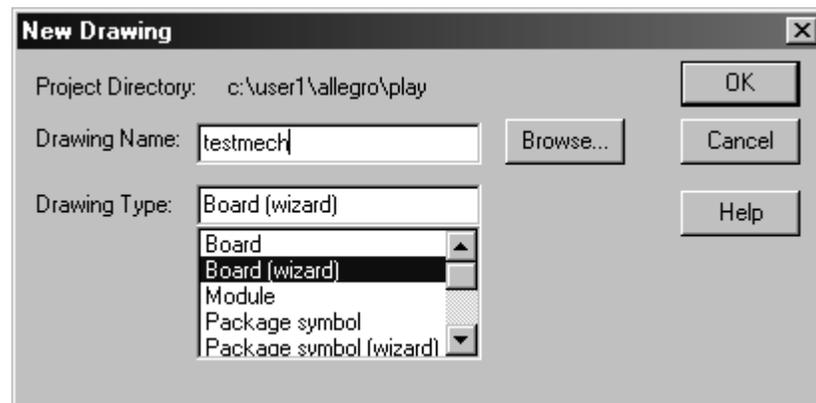
4. Click **OK** to close the New Drawing dialog box.

    The first Board Wizard form is displayed. This form is an introductory form to the wizard.

5. Select **Next>** to start the Board Wizard.

    The Template form is displayed

Using the Board Mechanical Wizard

1. Select **No** to the question "Do you have a board template that you would like to import in this board?" if this option is not currently selected.

2. Select **Next>** to not use a board template and continue to the next form.

The Tech File form is displayed.

3. Select **No** to the question "Do you have a tech file that you would like to import in this board?" if this option is not currently selected.

4. Select **Next>** to not use a tech file and continue to the next form.

The Board Symbol form is displayed.

5. Select **No** to the question "Do you have a board symbol that you would like to import in this board?" if this option is not currently selected.

6. Select **Next>** to not use a tech file and continue to the next form.

The General Parameters form is displayed.

This form is used to specify some of the drawing parameters, as well as the origin of the drawing.

7. Set the values of Units to **Mils**, drawing size to **B**, and the location of the origin to **At the center of the drawing** if these values are not currently set.

8. Select **Next>** to continue to the next form.

The General Parameters (Continued) form is displayed.

This form is used to specify the Grid Spacing, number of etch layers, and whether or not to create the default artwork films.

9. Set the values of Grid Spacing to **25.00**, Etch layer count to **4,** and the generation of artwork films to **Generate default artwork films** if these values are not currently set.

10. Select **Next>** to continue to the next form.

The Etch Cross-section details form is displayed.

This form is used to specify the layer names for each etch layer, excluding Top and Bottom, and for specifying whether the layers are for routing or for planes.

11. Change Layer2 to **GND** and Layer 3 to **VCC**. Set the Layer type to **Power plane** for these two layers. Set **Generate negative layers for Power planes** if this option is not currently set.

12. Select **Next>** to continue to the next form.

The Spacing Constraints form is displayed.

This form is used to specify the default constraints for the board.

13. Modify the form as required to match the following values:

Minimum Line Width:	5
Minimum Line to Line spacing	5
Minimum Line to Pad spacing:	5
Minimum Pad to Pad spacing:	5

14. Enter in the padstack name **via** for Default via padstack.

15. Select **Next>** to continue to the next form.

The Board Outline form is displayed.

This form is used to specify the shape of the outline.

16. Select **Rectangular Board** if this option is not currently set.

17. Select **Next>** to continue to the next form.

The Rectangular Board Parameters form is displayed.

This form is used to specify the rectangular board outline details.

18. Modify the form as required to match the following values:

Width(W):	5000
Height(H):	7000
No Corner cutoff will be used.	
Route keepin distance:	50
Package keepin distance:	100

19. Select **Next>** to continue to the next form.

The Summary form is displayed.

This form is used to verify that the correct file will be created. This is also your last chance to go "backwards" through any previous forms to change any data or specifications.

20. After verifying that the file *testmech.brd* will be created, select **Finish** to complete the Board Wizard and create the starting design.

The drawing *testmech.brd* is created and is opened in the Allegro Editor. At this point you can make any changes that you require. You will not save this Allegro database.

STOP **End of Lab**

Creating a Master Design File
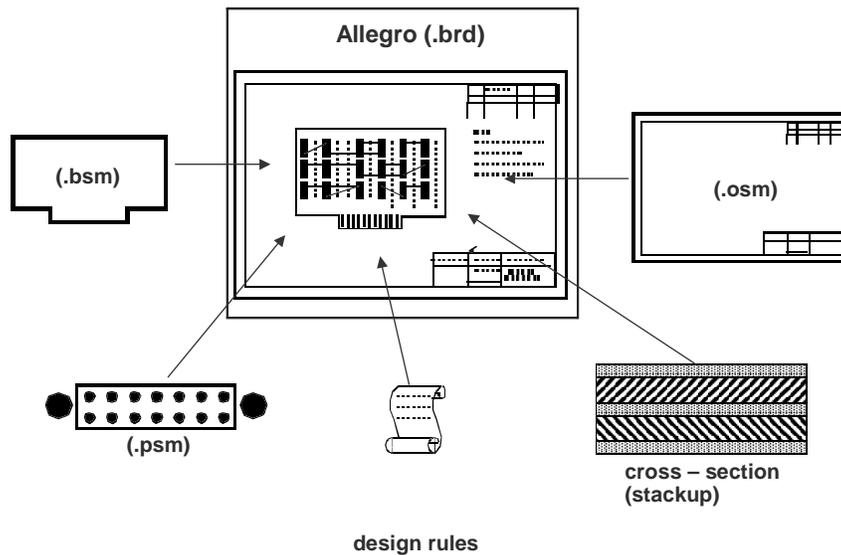
Summary

When you have the same basic board used many times, it is common to build a master design file as a starting point. The master design file will have the board outline placed, the cross section defined, the design rules set, and optionally may have common components such as connectors already placed. The master design file is simply a started board file that is saved in a library so that it can be used as a starting point for multiple designs. Using this method saves time and also ensures the accuracy of the design.

More Information

The Allegro design (board layout) database is created and saved in a design file format known as a board, or *.brd* file. It can be created initially as a mechanically correct (but logically non-intelligent) starting point for all designs using the same physical board configuration. Schematic connectivity information is loaded later (see the lesson titled *Logic Import*).

The advantages of creating a master design file are:

◆ It ensures that all physical layouts with a common geometry start from a "template" that has been thoroughly checked and approved (for example, mechanical dimensions, location/rotation of IO devices, LEDs, and so on).

◆ It provides a way to control the consistency of the end product (for example, drawing formats, fab and assembly notes, drawing size and accuracy settings, and datum points).

◆ You can read a "technology file" into this master design to establish board cross section information (layer stackup) and design rules (spacing and physical rule sets). See the lesson titled *Design Rules* for more information.

Use **Place > Manually** to insert package, mechanical, and format symbols into the design database.

Defining Layer Stackup
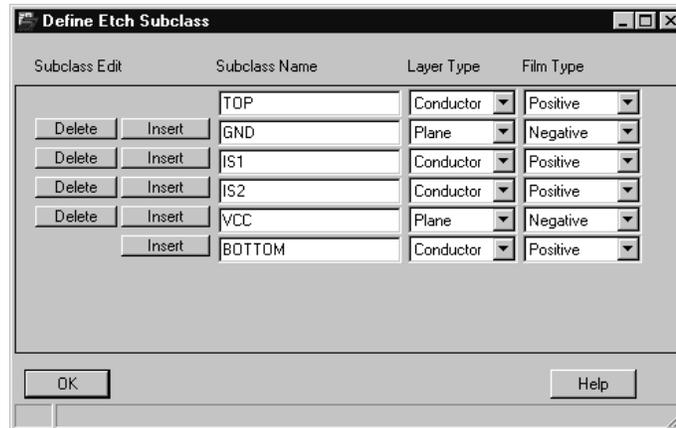
More Information

The **Setup > Subclasses > Etch** command opens the Define Etch Subclass form. Use this form to define your cross section (layer stackup) for the design. You define your routing layers and plane layers in this form. The first time this form is opened on a design, the stackup is simply TOP and BOTTOM.

By selecting from the Layer Type pull-down fields, you define the type of function for the selected layer. These fields include such types as conductor (used for routing layers), plane (used for embedded planes), and so forth. All the types are predefined.

The Etch Subclass Name field is used to define the layer name. As implied, this is the subclass name that will appear under the Etch class, Pin class, Via class, and so forth. Each name MUST be unique. If you have a single plane used multiple times (such as many occurrences of a Ground plane), you can define the layer names as GND1, GND2, and so on.

Lab

◆ Lab: Creating a Master Design File (.brd)
- Set drawing parameters.
- Place the mechanical symbol.
- Add format symbols.
- Add package symbols.
- Set color and visibility.
- Define the cross section (layer stackup).
- Save your board template.

More Information

The following lab will allow you to familiarize yourself with the process required to create a master design file. Items covered include placing the board mechanical symbol, adding common footprints, defining the cross section, and so on.

Lab 5-3:   Creating a Master Design File (.brd)

Objective: Learn to use the Layout Editor to create a design template.

In this lab, you will create an Allegro design (*.brd*) file. This design file will contain only mechanical data; no logical (schematic) data will be loaded.

This design file serves as a master template, or starting point, for all layouts that require its mechanical specifications. This ensures that all physical layouts with a common geometry start from a mechanical template that has been thoroughly checked and approved for use.

1. Choose **File > New** from the top menu.

2. Select **No** to not save the changes just made.

    The New Drawing dialog box appears.

3. Type the following name in the Drawing Name field:

    master
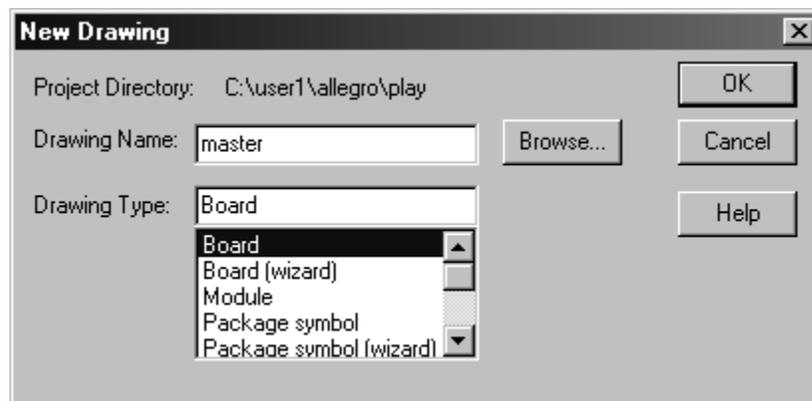
4. Click **OK** to close the New Drawing dialog box.

Setting Drawing Parameters

All designs created from this mechanical template will have the same drawing size, accuracy, and datum point.

1. Choose **Setup > Drawing Size**.

    The Drawing Parameters dialog box appears.

2. Change the settings in the Drawing Parameters dialog box to match those in the figure below.
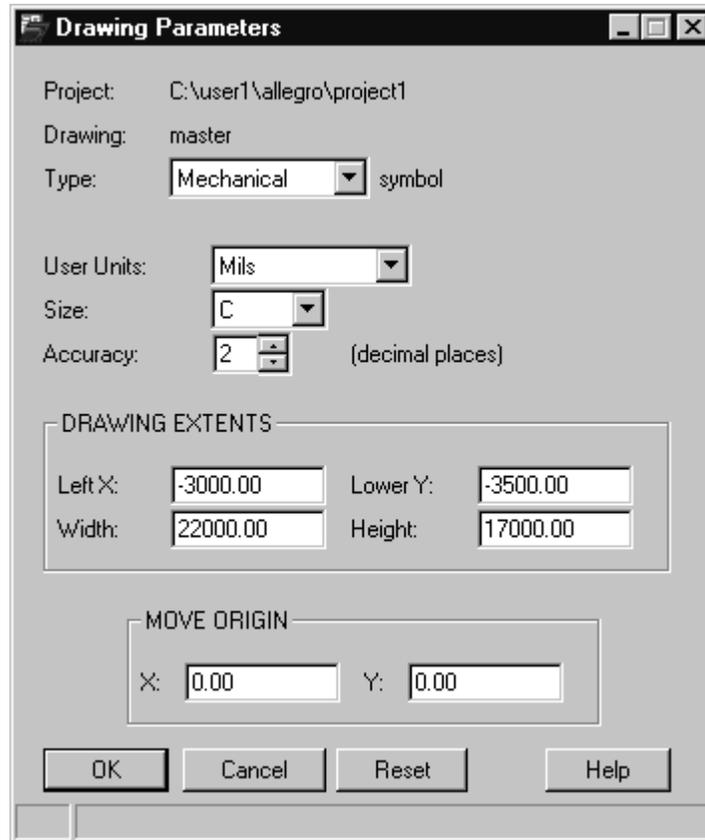
These settings cause the drawing origin to be placed 3.5 inches up and 3 inches to the right of the lower left corner of the drawing.

3. Click **OK** to close the Drawing Parameters form.

Adding the Mechanical Symbol

1. Choose **Place > Manually** from the top menu.

The Placement dialog box appears.

2. Click the **Advanced Settings** tab and enable both the **Database** and **Library** options under the Display definitions from: heading.

3. Click the **Placement List** tab, expand the **Mechanical symbols** directory, and check the **OUTLINE** symbol, as shown in the figure.
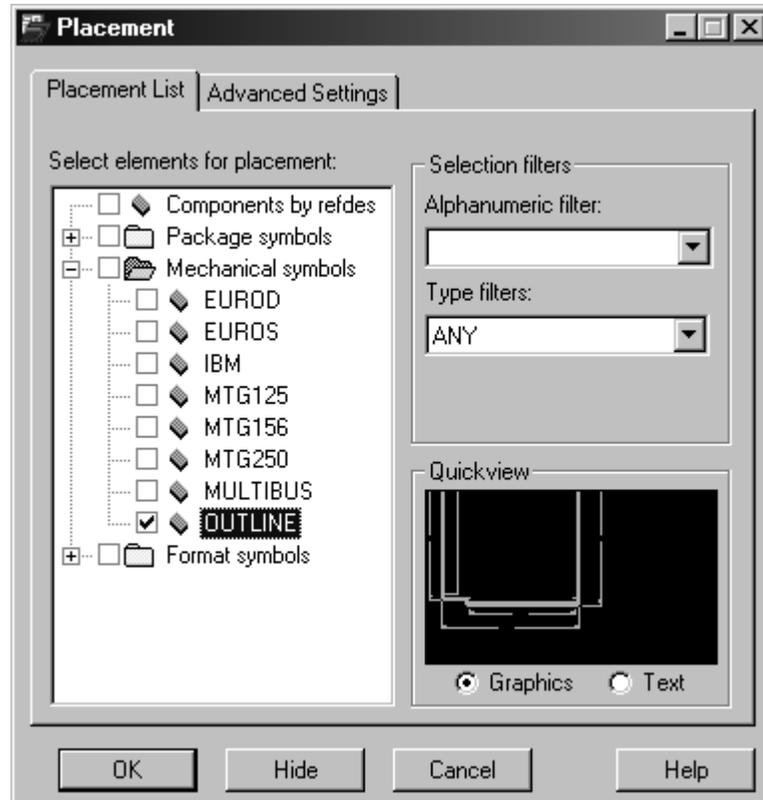
Notice the graphics representation displayed in the Quickview window. This is the *outline.bsm* symbol you completed in previous labs.

4. Click **Hide** in the Placement form.

   The mechanical symbol is attached to your cursor and the Placement form disappears.

5. At the Allegro command line, enter:

   x 0 0

   The outline is placed at the drawing origin.

6. Right click and choose **Done** from the pop-up menu.

   You will now verify that you have actually placed the same *outline.bsm* symbol that you created.

7. Choose the **Tools > Reports** menu item.

8. In the Reports dialog box, select **Symbol Library Path** and click **Report**.

   A report opens listing the *play* directory as the location of *outline.bsm*.

9. Close the Symbol Library Path Report form and the Reports form and zoom out to view the entire design, including the dimensioning text.

10. Click the **Color** icon. Under the Geometry group and the Board Geometry class, reset your colors to toggle **Dimension** off.

11. Select **OK** to close the Color and Visibility form.

The dimension text disappears, but the board outline remains visible.

Adding Format Symbols

In this part of the lab, you will add a drawing format and fabrication notes.

1. Choose **Place > Manually** from the top menu.

The Placement dialog box appears.

2. Click the + box next to **Format symbols** to expand this branch of the symbols tree.

A list of format symbols appears in the dialog box.

3. Click the symbol name **BSIZE** in the list, as shown in the figure.
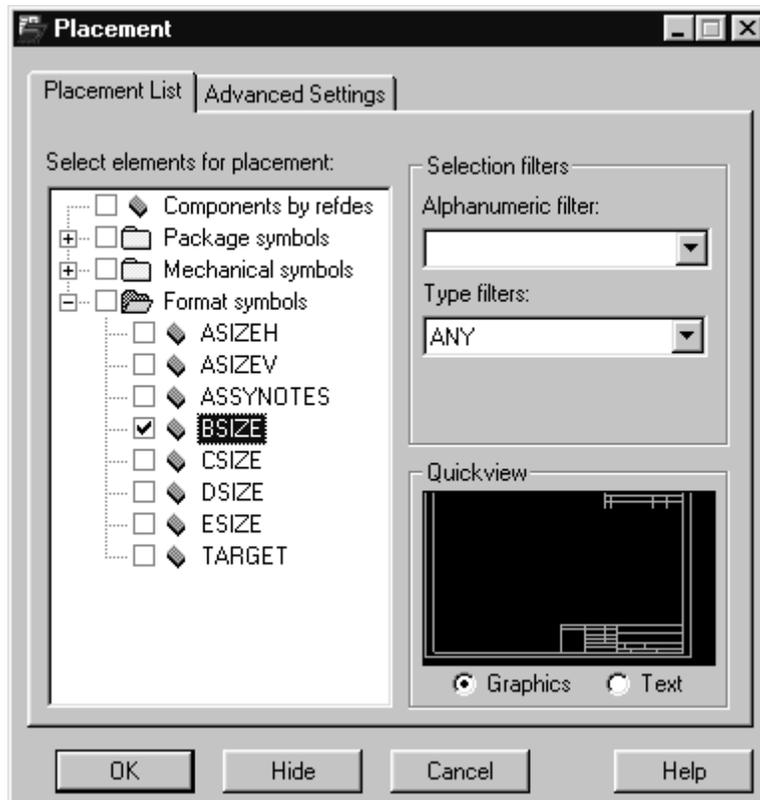
The format symbol, which is a B size, horizontal drawing format, is now attached to your cursor.

4. Click to place the drawing format. Use your zoom functions as needed.

The board should be surrounded by the drawing format outline, but leave some space to the right of the board outline, as shown in the figure below.

5. To add notes, in the Placement dialog box, enable the check box next to the name for the **ASSYNOTES** symbol.

6. Click to place the notes where you want them (on the right side of the board outline, within the format borders), as shown in the figure.

Adding Package Symbols

You can add any mechanically constrained devices that are common to all designs. By placing these into a master file, you ensure a consistent level of accuracy, which helps reduce error checking and corrections. Types of devices that should be preplaced in a master design *.brd* file include connectors, LEDs, switches, and any standard part that has a fixed placement.

1. Click the **-** box next to the **Format symbols** folder to collapse the list of format symbols.

2. Click the + box to the left of the **Package symbols** folder to expand the folder.

3. Scroll through the list of library symbols and enable the check box next to the symbol **DIN64**.

   This is a 64-pin connector symbol. When you move your cursor into the Allegro workspace, a connector symbol is attached to your cursor.

4. Select in the Allegro command line and enter:

   x -700 500

   The connector is placed.

5. Zoom in to the lower left corner of the connector area.

   Since a master design file is simply a mechanical template with no logical (schematic) database, the edge connector you placed has a generic reference designator (**J***).

6. Click the **Advanced Settings** tab and Disable the **Autonext** option.

7. Click the **Placement List** tab.

8. In the Placement dialog box, scroll through the list of Package symbols and enable the check box next to the symbol **BNC**.

9. Select in the Allegro command line and enter the following coordinates:

   x 3700 350

   x 3700 1100

   Both BNC connectors are placed on the right edge of the board.

10. Right click and choose **Done** from the pop-up menu.

Setting Color and Visibility

In Lesson 1, you created a script file that sets color and visibility for various layers of a drawing. You will use that script file now.

1. At the Allegro command line, enter:

   replay colors

   The *colors.scr* file sets the color and visibility automatically.

2. Choose **View > Zoom World** from the top menu.

   Notice that the drawing format, fab notes, and board dimensions have been turned off, leaving just the board elements on.

3. Choose **View > Zoom Fit** from the top menu to zoom into the entire board.

Defining the Cross Section (Layer Stackup)

By default, all new design files are created with just two layers, top and bottom. In this part of the lab, you will learn how to add more layers to the stackup. This process is significantly different, depending on which Allegro Editor you are using.

1. Choose the **Setup > Subclasses** menu item.

   The Define Subclass dialog box appears.
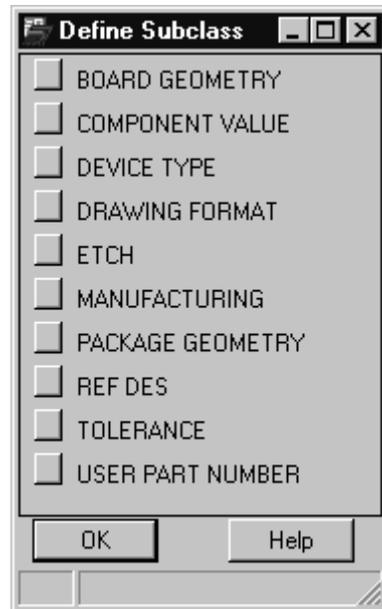
2. Select the **ETCH** subclass.

   The Define Edit Subclasses dialog box appears.

   Notice that a TOP and BOTTOM layer are already defined by default as conductor layers.

3. Click **Insert** to the left of the BOTTOM layer.

   A new layer is inserted in the stackup. The default values of the Subclass Name, Layer Type, and Film Type are those of the layer just below the added layer.

   ## 🗒 Note

   New layers are always inserted above the layer you selected. You change the layer parameters after the layers are inserted.

4. Repeat step 3 until there are four layers in between TOP and BOTTOM.

5. Set up your stackup to match the layer specifications shown in the figure.
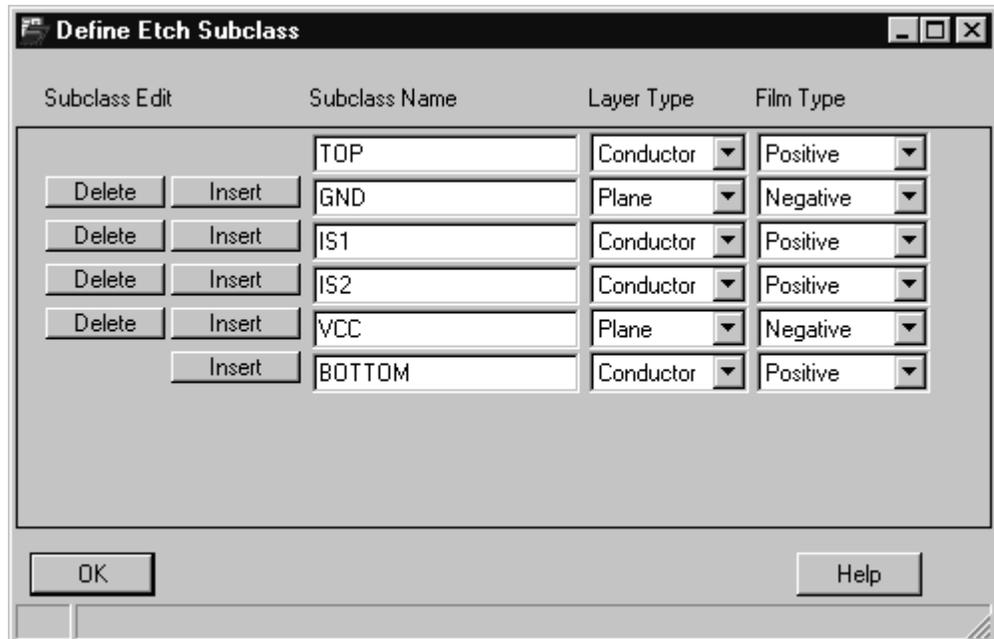
Note

The GND and VCC planes are both negative. In the lesson that covers copper areas you will change one of these to positive. We will set one to positive and the other to negative so that you can gain experience creating one of each type.

In this master design file you have added a power and a ground plane and two inner layers for routing. All designs created from this mechanical template would start as six-layer boards. However, for this design, only a four layer board is required.

Deleting Layers from a Stackup

1. Select the **Delete** button to the left of layers IS1 and IS2 to delete these layers from the stackup.

   The layers are deleted from the design leaving a four layer design. This is the stackup you will use for the rest of the design.

Saving Your Board Template

You have learned how to add internal plane and wiring layers. You can now save the board template so it can be used again and again.

1. Click **OK** to close the Define Etch Subclass dialog box.

2. Click **OK** to close the Define Subclass dialog box.

3. Choose **File > Save As** from the top menu.

   A Save_as browser window opens.

4. Navigate to your working directory.

- If the schematic capture tool you want to use with Allegro is Concept, then your working directory is *../project1/worklib/root/physical.*

- If the schematic capture tool you want to use with Allegro is Capture, then your working directory *../project2.*

- If the schematic capture tool you want to use with Allegro is a third-party tool other than Concept or Capture, then your working directory is *../project3.*

5. Enable the **Change Directory** box.

6. Click **Save** to save the *master.brd* file in the correct directory.

The *master.brd* file is saved to disk. It is important to save the *.brd* to this directory and to use the Change Directory check box.

7. Choose **File > Exit** from the top menu to exit the Allegro software.

You have completed the library development section of this course.

STOP **End of Lab**

Lesson 6: Importing Logic Information into Allegro

Note

The labs in this lesson demonstrate how to bring schematic data from the Concept tool, Capture tool, or a third-party front-end tool (such as ViewLogic). **Do not do all labs.** Choose the lab that matches your in-house needs.

Learning Objectives

◆ Understand the key choices to be made when importing logic information from a schematic tool into the Allegro layout environment.

◆ Set up and import logic information into Allegro from one of the these three schematic environments:

- Concept-HDL
- Capture
- Third-party

Summary

In this section you will learn about Logic Import, which is the process of importing logic from your schematic capture tool into the Allegro database. You will learn how to import from Concept into Allegro, from Capture into Allegro, and from a non-Concept tool, known as a third-party netlist.

Design Layout Process
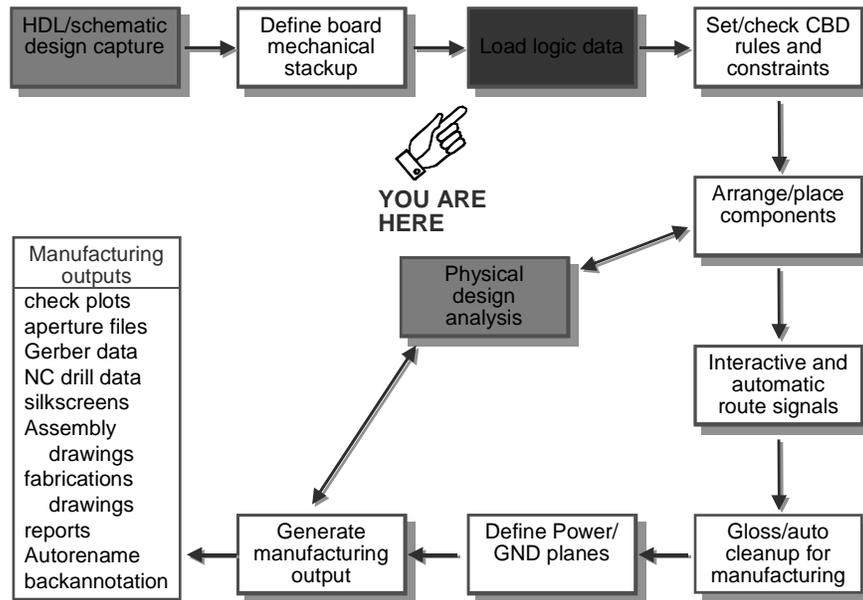
```
┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│ HDL/schematic│──▶│ Define board │──▶│Load logic data│──▶│Set/check CBD │
│design capture│   │  mechanical  │   │              │   │  rules and   │
│              │   │   stackup    │   │              │   │ constraints  │
└──────────────┘   └──────────────┘   └──────────────┘   └──────────────┘
```

YOU ARE HERE

```
                                              ┌──────────────┐
                                              │Arrange/place │
                                              │ components   │
                                              └──────────────┘

┌──────────────┐   ┌──────────────┐
│ Manufacturing│   │   Physical   │
│   outputs    │   │    design    │
│ check plots  │   │   analysis   │
│ aperture files│  └──────────────┘
│ Gerber data  │
│ NC drill data│                              ┌──────────────┐
│ silkscreens  │                              │Interactive and│
│ Assembly     │                              │  automatic   │
│   drawings   │                              │ route signals│
│ fabrications │                              └──────────────┘
│   drawings   │
│ reports      │   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│ Autorename   │◀──│   Generate   │◀──│ Define Power/│◀──│  Gloss/auto  │
│ backannotation│  │manufacturing │   │  GND planes  │   │ cleanup for  │
└──────────────┘   │   output     │   │              │   │manufacturing │
                   └──────────────┘   └──────────────┘   └──────────────┘
```

More Information

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the Load Logic Data box will now be discussed.

Concept-Integrated Logic Design with Physical Layout
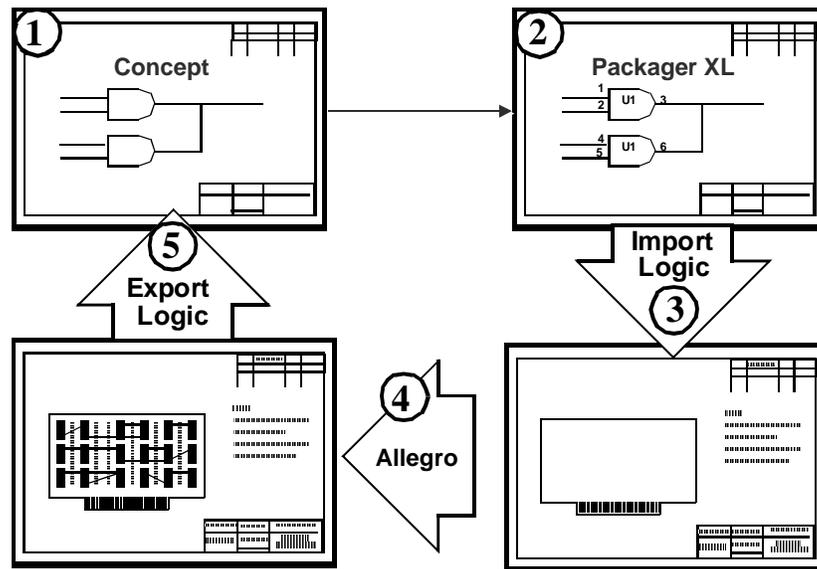
Summary

The following several pages cover the transfer of logic from Concept HDL into Allegro. Loading of Capture and a third-party netlist will be covered later.

More Information

The diagram illustrates the front-to-back integration between Concept and Allegro tools.

◆   Concept Front End

> **Concept**: All Concept HDL drawings for the project are contained in the worklib directory.

> **Packager-XL**: The Packager converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic. The packaged parts and their connections are written into transfer files.

◆   Allegro

> **Import Logic**: In the physical directory, the design now contains connection information.

> **Allegro**: Places, routes, pin and gate swaps for optimum routing results; generates manufacturing output.

> **Export Logic**: This program generates backannotation files the Concept tool uses to update the schematic.

Note

From the Concept or Project Manager point of view, Export Physical is the same as the Allegro Import Logic command. Likewise, Import Physical means the same as the Allegro Export Logic command.

Transfer Files (pst*.dat)

pstxprt.dat
```
FILE_TYPE=EXPANDEDPARTLIST;
{ Packager-XL
03-May-1995 A
DIRECTIVES
 ROOT_DRAWING
 SOURCE_TOOL=
 ABBREV = 'MY
END_DIRECTIVE
PART_NAME
 U10 '74LS00'
 ROOM='HEX';
SECTION_NUMBE
 '(STOP LS00.
 C_PATH='/LOG
 PATH_NAME='(
 PATH='23P',
 ABBREV='LS00
 BODY_NAME='L
 PART_NAME='7
```

pstxnet.dat
```
{ Packager-XL ru
09-May-1995 AT 12
NET_NAME
'INT5'
 'INT5':
 C_SIGNAL='/:LOG
ROUTE_PRIORITY='2
MIN_LINE_WIDTH='1
NODE_NAME    U1
 '(STOP F00.18P)
 '-Y'<0>:;
NODE_NAME    U1
 '(STOP F74.20P)
 'D'<0>:;
NET_NAME
'MIN0'
 'MIN'<0>:
 C_SIGNAL='/:LOG
```

pstchip.dat
```
FILE_TYPE=LIBRARY_PARTS;
primitive '74LS00';
  pin
   'B'<0>:
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(13,10,5,2)';
     PIN_GROUP='1';
   'A'<0>:
INPUT_LOAD='(-0.4,0.02)';
     PIN_NUMBER='(12,9,4,1)';
      PIN_GROUP='1';
   '-Y'<0>:
OUTPUT_LOAD='(8.0,-0.4)';
     PIN_NUMBER='(11,8,6,3)';
   end_pin;
   body
PART_NAME='74LS00';
JEDEC_TYPE='SOIC14';
```

More Information

You use the transfer (pst) files generated by the Packager program to transfer information from the schematic to an Allegro design. These files are:

File	Description
pstxprt.dat	This is a parts list file. It lists each physical package (created by the packager) in the schematic, along with its reference designator and device type. For packages comprised of multiple logic gates, this file identifies which gate was placed in which section of the physical package.
	This file may also contain some properties attached to parts in the schematic, such as ROOM='IF', VALUE='4.7K'.

File	Description
pstxnet.dat	This is a netlist file. It uses keywords (net_name, node_name) to specify the reference designators and pin numbers associated with each net in the schematic. This file may also contain some properties attached to nets in the schematic, such as ROUTE_PRIORITY, ECL, and so forth.
pstchip.dat	This is a device definition file. It contains electrical characteristics (for example, pin direction and loading), logical-to-physical pin mapping, and voltage requirements. It defines the number of gates in a device, including gate and pin swapping information. This file also contains the name of the package symbol that represents this device type in the physical layout (such as JEDEC_TYPE='DIP14_3', ALT_SYMBOLS='(T:SOIC14)').

Importing Logic into Allegro from Concept

.../worklib/root/packaged/   .../worklib/root/physical/

Packager-XL

pstxprt.dat

pstxnet.dat

pstchip.dat

Design Sync ▶

master.brd

netrev.lst

eco.txt
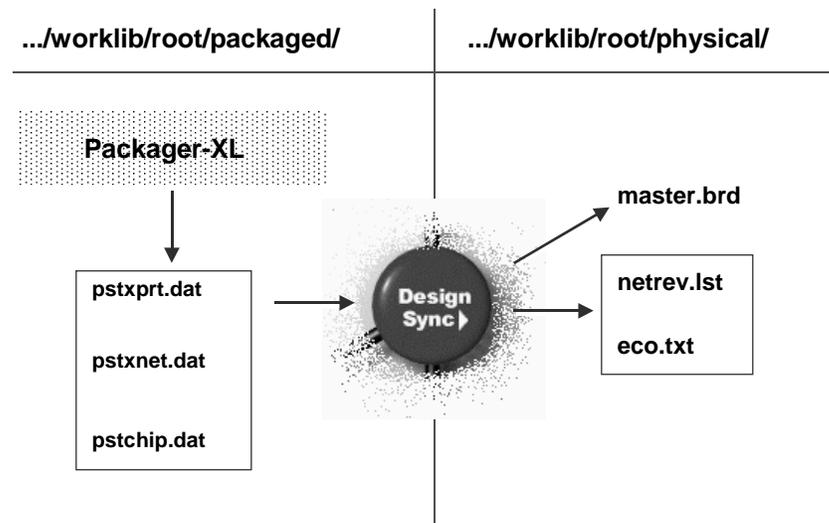
More Information

Netrev is the program that reads the transfer files into the Allegro design. It performs the following operations:

◆ Searches the library for the package symbols specified in the *pstchip.dat* file (including all alternate symbols). The Allegro program also searches the library for any padstacks required by each package symbol. If it is unable to locate a package symbol, warning messages are generated, but the program continues. Remember, the variable PSMPATH as defined by the env file tells the program where your libraries are located.

When the required package symbol(s) is found in the library, it is compared to the device definition file (*pstchip*.dat). The pins in the package symbol must match the pins specified in the device definition file. Any mismatches will generate error messages.

◆ Establishes an "association" between the sch_1 and physical directories. This association lets you cross-probe between Concept and Allegro tools.

◆ Creates log files (*netrev.lst* and *eco.txt*) indicating whether the process was successful. All errors and warnings will be listed in the *netrev.lst* file.

Importing Logic Data
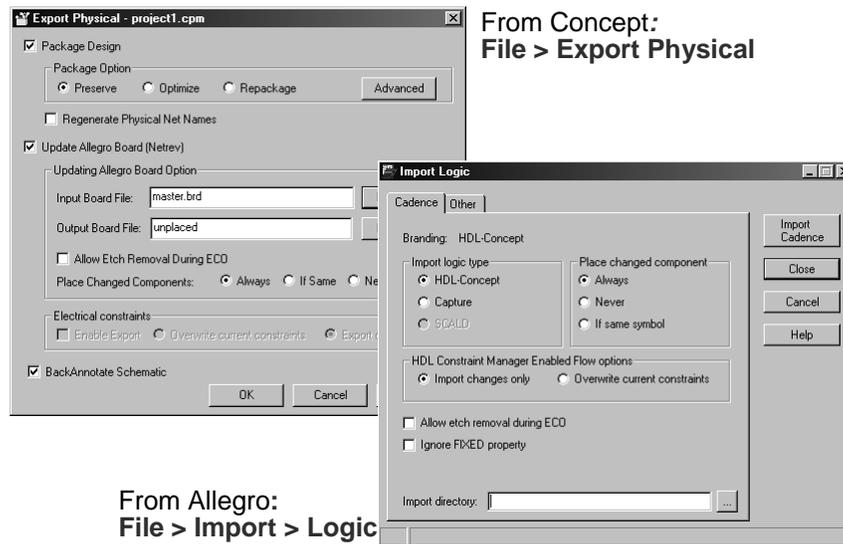
From Concept*:*
File > Export Physical

From Allegro**:**
**File > Import > Logic**

More Information

Use either of the menus shown to transfer logic data from Concept to Allegro programs. File transfer from Concept to Allegro can be accomplished through any of the following methods:

■ From the Concept top menu, select **File > Export Physical**.

■ From the Allegro top menu, select **File > Import> Logic**.

■ From the Project Manager, click **Design Sync**.

Data that was in Concept programs created prior to version 5.0 must use the SCALD logic type option, whereas data created in version 5.0 and later must use the HDL-Concept type.

Engineering Changes—placement
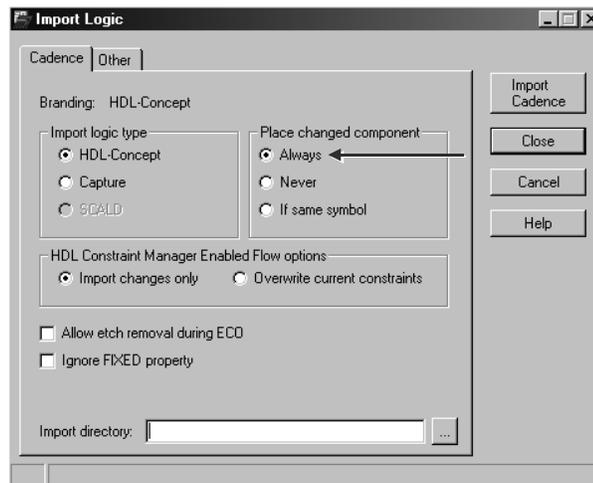
More Information

With an ongoing design, schematic changes are incorporated (ECO) with the netrev process, which brings in the transfer files from the edited schematics. If the Allegro design has not been placed or routed, the new transfer files simply replace the original Allegro database. If placement has already occurred, the following function and options apply:

Place Changed Component in Allegro: Determines how placed parts are treated in the ECO process. When a part in an edited schematic has a reference designator that matches a placed part in the Allegro layout, parts are compared to determine if there are any changes. If the part has not changed, it maintains its location in the Allegro layout. If the part has changed, you can select one of the following options:

> **Always** replaces the old part in the Allegro layout with the changed part from the edited schematic, regardless of the type, value, or package symbol change (at the same x/y location and rotation as the old part).

> **If Same Symbol** replaces the old part in the Allegro layout with the changed part from the edited schematic if the package symbol has not changed (type/value change, but same package symbol). If the package symbol has changed, the old part is removed from the layout, and the changed part is added to the Allegro database (unplaced).

> **Never** removes the old part from the layout and adds the changed part to the Allegro database (unplaced).

Note

Parts in the edited schematic with no matching reference designator in the Allegro layout are added as unplaced parts. Parts in the Allegro layout with no matching reference designator in the edited schematic are deleted.

Importing Electrical Constraints
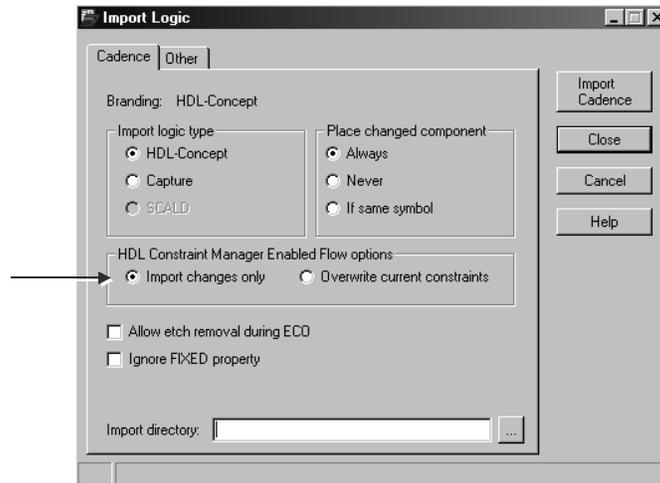
More Information

If you wish to import Electrical Constraints defined by the Constraint Manager, you must first toggle on the Enable import field. When this option is enabled, you have the choice of one of the following two options:

Import changes only - This option compares the current Constraint Manager database against the baseline Constraint Manager database and will only import the constraints that are different in the current database.

Overwrite current constraints - This option specifies to read the current Constraint Manager database and import ALL constraints in the current constraint database.

There is one constraint file that is used to read in the constraints (with an optional second file). These files are as follows:

pstcmdb.dat - Contains definitions of electrical constraints in the schematic as defined and created in the Constraint Manager database. This file must be present in order to import electrical constraints.

pstcmbc.dat - An optional file that defines the electrical constraint baseline in the schematic data.

Engineering Changes—Routing
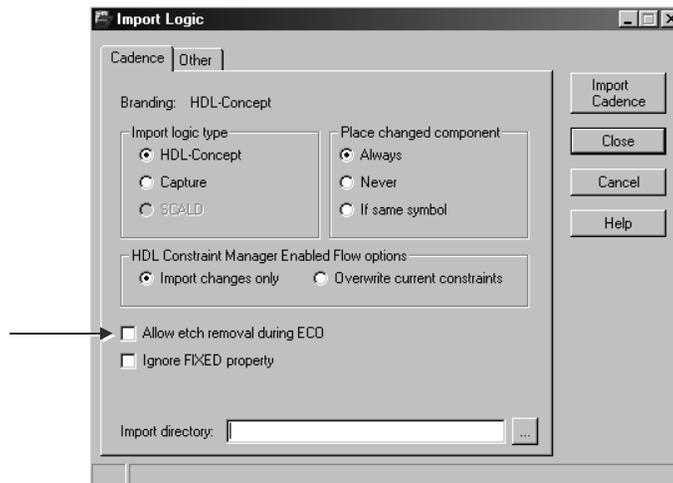
More Information

If routing has already occurred, you may choose to select the following option:

- ■ **Allow Etch Removal During ECO**: This function automatically resolves any conflicts between the edited schematic and any existing connections on the board. These conflicts can be due to wiring changes in the schematic, as well as part changes (see previous discussion regarding the handling of changed parts).

When an existing board connection conflicts with the new schematic data, it is flagged with a DRC error marker. You can then evaluate each error marker, and manually edit the connections in question in order to resolve the problems.

Rather than editing the conflicting connections manually, you can select an automatic edit process to resolve the problems. In this case, the Allegro tool will remove any wiring segments that do not match the edited schematic (shorted signals at component pins). Once the connection at the shorted pin is broken, all dangling wire segments are eliminated.

When completed, the Allegro layout will be free of all conflicting wiring. You are left with unrouted connections, which represent the schematic changes. You can then route these missing connections manually or automatically.

All part and connectivity changes made to the Allegro layout during the ECO process are documented in a report (*eco.txt*).

Schematic-Driven Layout

Packager-XL capabilities include:

◆ Component definition properties

◆ Component instance properties

◆ Schematic instance properties

◆ Pin instance properties

◆ Net properties (compiler input buffer limit of 255 characters)

◆ Electrical rules
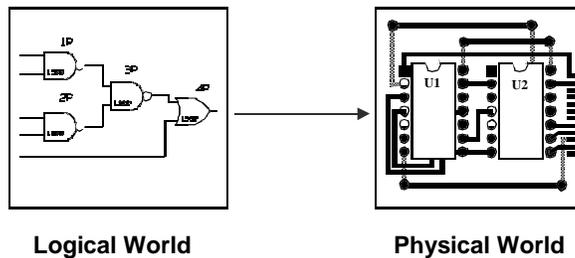
You can use the **Attributes** command to add part and net properties to the schematic.

Logical World   **Physical World**

More Information

It is possible to use the schematic to communicate your physical layout requirements. You can use properties attached to nets and parts in the schematic to affect component placement and signal routing.

Component Definition Properties are usually contained in the chips_prt or PPT files. These properties carry information about the type of physical package required (such as JEDEC_TYPE, ALT_SYMBOLS, PINCOUNT). You can also assign these properties to parts right in the schematic (to specify physical part requirements for the Packager). Schematic values for these properties will override values found in library files.

Use Comp_Name or Comp_Name_Suffix properties to control type names for new physical parts. These new physical parts (types) are shown in the *pstxprt.dat* and *pstchip.dat* files.

Component Instance Properties are properties related to the actual layout process (for example, ROOM, TERMINATOR_PACK, NO_PIN_ESCAPE, NO_MOVE, FIX_ALL, COMPONENT_WEIGHT). These properties appear in the *pstxprt.dat* file for passage to the Allegro tool. Use the COMP_INST_PROP directive (*pxl.cmd* file) to specify component instance properties that are included in the *pstxprt.dat* file.

Schematic Instance Properties control the packaging of functions (gates).

Pin Instance Properties address signal routing requirements.

Electrical Rules address signal integrity requirements created by the Constraint Manager.

Net Properties control signal routing and analysis (such as line sizes and clearances, layer restrictions, high speed, priority, length requirements and crosstalk thresholds). These properties appear in the pstxnet.dat file for passage to the Allegro tool.

Capture-Integrated Logic Design with Physical Layout
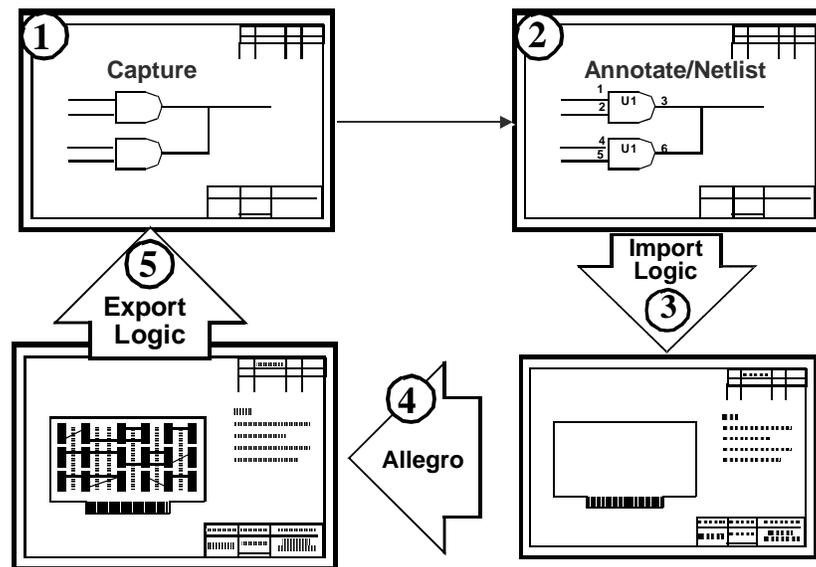
More Information

The diagram illustrates the front-to-back integration between Capture and Allegro tools.

Capture Front End

> **Capture**: It is not required that the Capture schematic reside in the same directory as the Allegro design. However, it is recommended that the two be kept together.

> **Annotate**: The Annotate program converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic.

> **Allegro Netlister**: The Allegro Netlister creates the transfer files used by Allegro. By default, these files are created in a directory named *allegro*.

Allegro

> **Import Logic**: After this step has been completed, the design contains connection information.

> **Allegro**: Places, routes, pin and gate swaps for optimum routing results; generates manufacturing output.

> **Export Logic**: This program generates backannotation files that the
> Capture tool uses to update the schematic.

Capture-Side Interface with Allegro
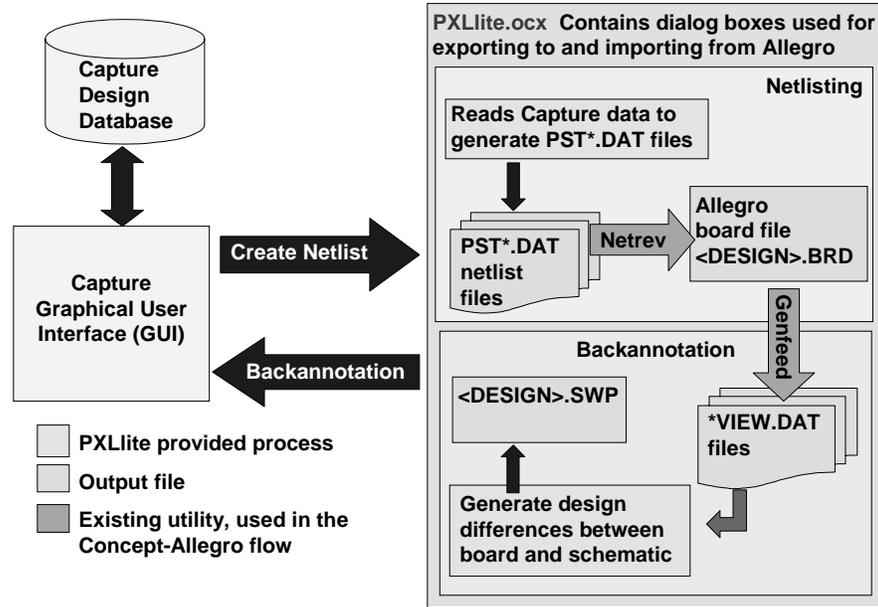
More Information

The Allegro Netlister (PXLlite) reads the Capture database and creates the
same format pst files as the Concept Packager XL routine. Therefore, the
same program (netrev) can be used by Allegro to read in either a Capture
schematic or a Concept schematic.

For Backannotation, the same Allegro program (genfeed) is used to create
the Allegro output files. These files are then read by Capture and used to
update the schematic to reflect any changes made to the design by Allegro
(pin and gate swapping, reference designator changing and so on).

Capture-Allegro Logic Import
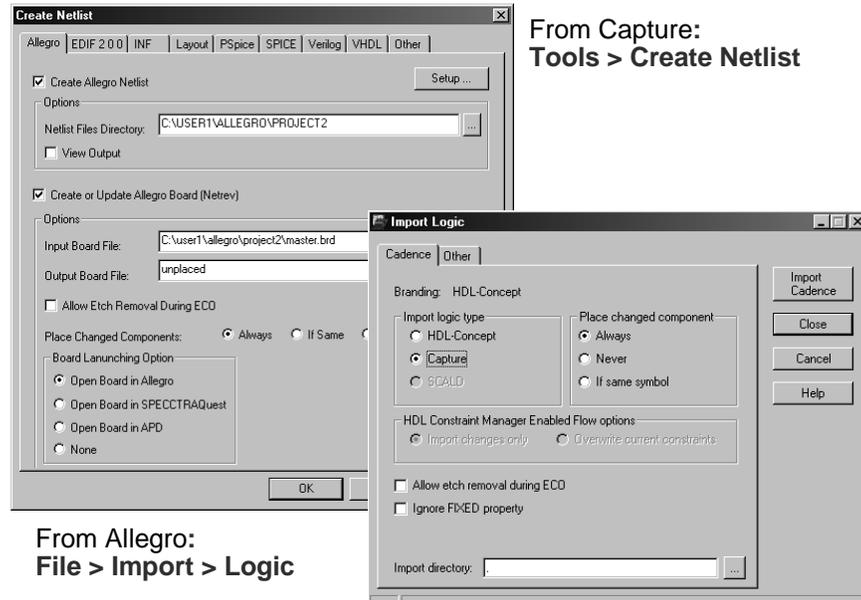
From Capture:
Tools > Create Netlist

From Allegro:
File > Import > Logic

More Information

After you have annotated your schematics, you must use the Allegro Netlister to create the input files for Allegro. Use the **Tools > Create Netlist** option from the Project menu in Capture or the Allegro tab to create the three "pst" files. These are the same three files (*pstchip.dat*, *pstxnet.dat*, *pstxprt.dat*) created and used in the Concept-to-Allegro transfer process.

At the same time you are creating the Allegro interface files, you can also "push" these files into Allegro by using the Create or Update Allegro Board (netrev) option. This option will run the Allegro netrev program that will read the interface files and create a new Allegro design or update an existing Allegro one.

If you do not want to run the netrev program from the Allegro Netlister inside Capture, you can import the interface files from within Allegro. Use the **File > Import > Logic** command from the top menu in Allegro and choose the Capture option. Use the **Import From** field to point to the three interface files created by the Capture-Allegro Netlister program.

Third-Party Logic Import
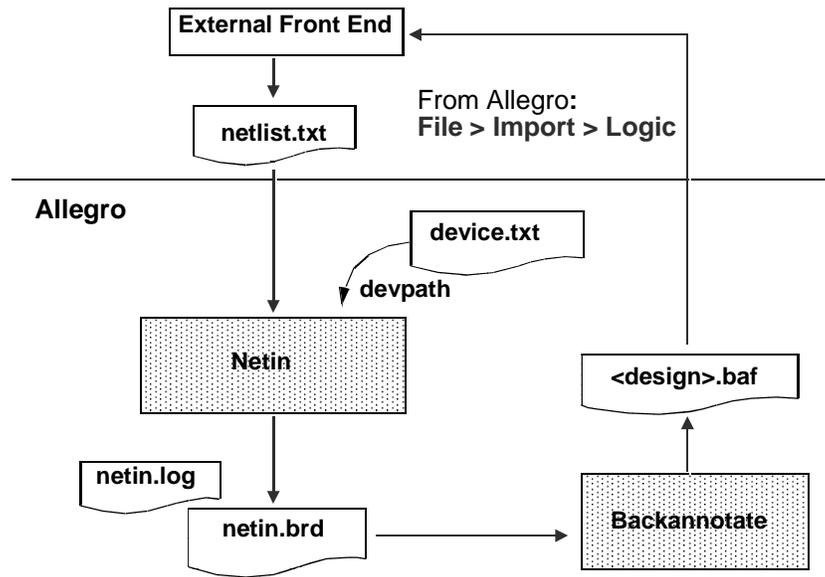
More Information

If you have not used the Concept or Capture front-end tools to generate the schematic, you must use a netlist and device files.

The netlist contains the part and connectivity data. Device files are library files that describe the parts in the netlist (one device file per device type). The netlist is read into an Allegro design using the Netin process. A log file (*netin.log*) lists any errors found in the netlist or device files.

You can also generate a backannotation file to return data back to the third-party system.

The Allegro tool looks at the DEVPATH environment variable to locate the device files required during the Netin process. Device files will be covered shortly.

Netlist Format

```
(NETLIST)
(Wed Dec 25 12:25:53 1996)
$PACKAGES
CAP400 ! 'CAP-22UF' ! '022UF' ; C21 C22 C23 C24 C25,
C26 C27 C28
CONN140 ! 'CONN140' ; J1
CRYSTAL ! 'OSC' ; Y1
DIP24_4 ! 'MEMORY' ; U15
SMDCAP ! 'CAP-.01UF' ! '01UF' ; C1 C2 C3 C4 C5 C6,
C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19,
C20
SMDCAP ! 'CAP-1UF' ! 1UF ; C29 C30 C31 C32 C33
SMDRES ! 'PRES0' ! 10 ; R1
SOIC16 ! '74F153' ; U10 U11 U12 U13
$A_PROPERTIES
ROOM BUFFER; U10 U11
ROOM ONE; C8 C9 R1
$NETS
A1 ; J1.2 U13.10 U12.10 U11.18 U10.10
A2 ; J1.3 U13.6 U12.9 U11.5 U10.9
A3 ; J1.4 U11.10 U12.8 U13.5 U10.8

$END
```

- **parts list section** →
- **(optional)** →
- **pin/signal section** →
- **line continuation character (comma)**

More Information

The netlist contains two main sections. The first is the PACKAGES section. The line $PACKAGES starts this section, which is basically a parts list. Each reference designator in the design MUST be identified here. See the Help files for the exact syntax of this section.

The second area of the netlist is the NETS section. The line $NETS starts this section, which contains all the nets in the design and the pin connections for those nets. See the Help files for the exact syntax of this section.

If you wish to add properties in your netlist, use the $A_PROPERTIES section. If you want to add component or part level properties, then the line $A_PROPERTIES should appear after all the parts have been defined in the $PACKAGES section. If you want to add net or signal level properties, then the line $A_PROPERTIES should appear after all the nets have been defined in the $NETS section.

You use the $SCHEDULE section to define specific pin order connection. It must appear after the $NETS section. An example of a schedule section to describe a "T" connection is shown below.

U1.1 — U2.1 — U3.1 $NETS
       | $SCHEDULE
      U4.1   CLK; U1.1 U2.1 U3.1; U2.1 U4.1
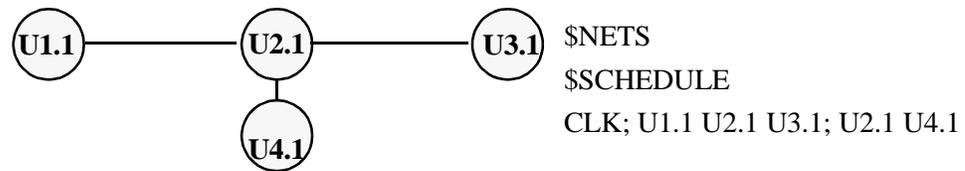
General Rules for Netlists

| Field name	length	Acceptable characters
package name	27	A to z, 0 to 9, dash (-) and underscore (_)
device type	30	All except ! and '
function designator	30	All except ! and '
reference designator	30	All except ! and '
pin number	30	All except ! and '
pin name	30	All except ! and '
net name	30	All except ! and '
property value	30	All except ! and '
tolerance	30	All except ! and '
user part number	30	All except ! and '

More Information

The table shows the maximum field width and allowable characters for each data field in an Allegro netlist.

Other rules to remember:

- Data fields are not case-sensitive.

- Each data record must have no more than 78 characters on a line. Extend records by adding a comma after the last instance in a line. The comma acts as a continuation mark.

- You can include comments in parentheses; they are ignored by the Netin process. (Do not include comments inside a data field.)

Device Files

filename = 7400.txt

```
(Netlist contains device type 7400)
PACKAGE DIP14_3
CLASS IC
PINCOUNT 14
PINORDER   7400 A B -Y
PINUSE     7400 IN  IN OUT
PINSWAP    7400 A  B
FUNCTION G1 7400 1  2  3
FUNCTION G2 7400 4  5  6
FUNCTION G3 7400 9  10 8
FUNCTION G4 7400 12  13 11
POWER    +5V; 14
GROUND   GND; 7
END
```
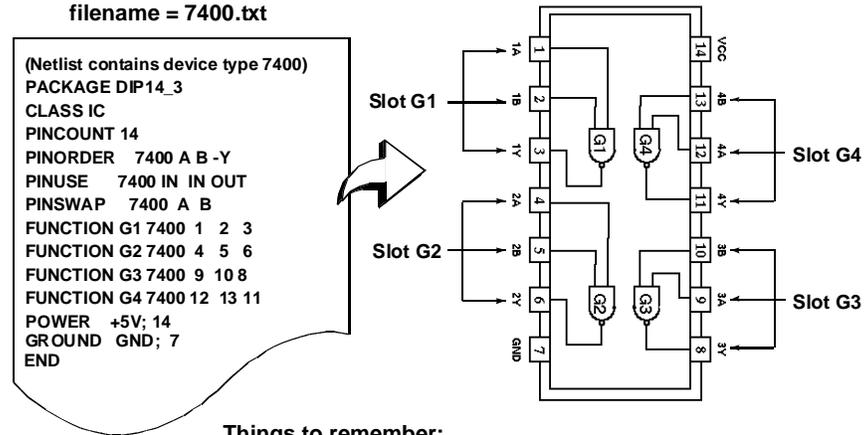
Things to remember:
Device file names must be lowercase, with a *.txt* extension.
Contents of device files are not case sensitive.
Use parentheses for comments.

Summary

A device file must exist for each different part type used in the netlist. The device file disk file name must be the part type as it appears in the netlist, with the extension *.txt*. The path used for locating the device files will be determined by the Allegro environmental variable DEVPATH, which is defined in the env file. See the Help files for the exact syntax of the device files.

More Information

You must use device files if you import third-party netlist data into the Allegro software. Cadence Concept and Capture schematic tools provide electrical component descriptions along with connectivity data. Third-party netlists do not contain electrical component descriptions and therefore necessitate the use of device files. Similar to symbol files, which provide physical component descriptions, device files provide electrical descriptions. Where physical descriptions include pin spacing, body size and padstack information, electrical descriptions define input and output pins, power pins, and gate assignments.

Things to remember when creating device files:

■   Device file names must be lowercase, with a *.txt* extension.

■   Contents of device files are not case-sensitive.

■   Use parentheses to enclose comments.

■   The only mandatory line in a device file is:

PINCOUNT

Package Properties in Device Files

Syntax:

PACKAGEPROP <property_type> <property_value>

For example:

PACKAGEPROP alt_symbols '(T:soic14;B:soic14_pe)'

PACKAGEPROP terminator_pack

PACKAGEPROP value 50ohm

More Information

If you wish to have properties associated with a device, use the PACKAGEPROP command in the device file. The syntax is the keyword PACKAGEPROP, followed by the property name and then followed by the value of the property. The following are common examples:

alt_symbols defines alternate package symbols that you can substitute for the primary package symbol during manual placement.

terminator_pack is used by the terminator assignment program to match the correct terminator with the appropriate ECL net. No additional value is needed. When this PACKAGEPROP appears, it flags the ECL scheduler that the device is a terminator.

value is used by the terminator assignment program to create a match between an ECL net and an appropriate termination package. (The ECL net must have a LOAD_TERM_VALUE property.)

Loading a Third-Party Netlist
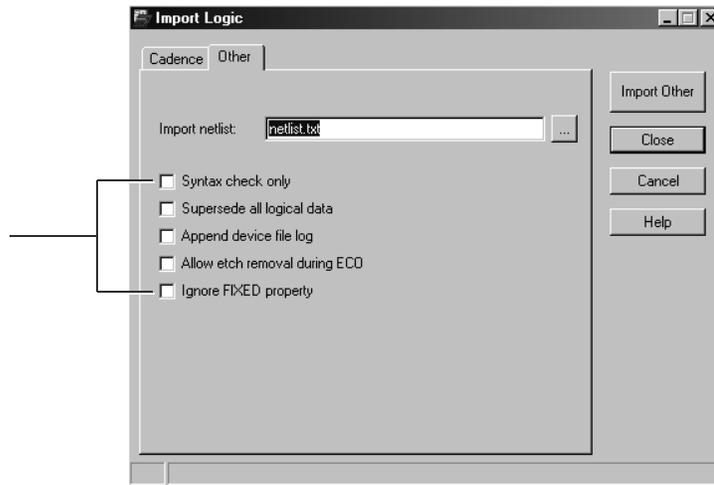
More Information

You cannot create a board by transferring design logic to Allegro software. Rather, you update an existing board displayed in the Allegro tool.

1. Before loading the design logic, set up the cross section and the board outline first.

2. Select **File > Save** (or **File > Save As**, where appropriate).

3. Select **File > Import > Logic**.

4. In the Logic Type section, select **Third Party**.

5. Enter or browse for the netlist *filename.txt* in the Import netlist field. (The file name shown in the illustration is an example.)

6. If the netlist is not in the Allegro working directory, specify a complete path.

7. Determine which (if any) third-party operating parameters to use (these are located in the Other folder tab):

    Syntax Check Only

    Supersede All Logical Data

   Append Device File Log

    Allow etch removal during ECO

    Ignore FIXED property

8. If you wish to save the settings applied in the dialog box, click **Apply**.

9. Click **OK**.

The tool uses the information from the Import Logic section to read and compile the netlist and generate the *netin.log* file.

Netin Checking

Netlist   **Device File**

```
(Netlist)
$PACKAGES
! 7400 ; U1 U2
! 54als244 ; u3 u4 u5

$NETS
clock ; u1.1 u2.20
enable ; u3.1 u5.19
signal1 ; u4.3 u5.6
signal3 ; u4.5 u2.9

$END
```

```
(Netlist contains device type 7400)
PACKAGE DIP14_3
CLASS IC
PINCOUNT 14
PINORDER  7400 A  B  -Y
PINUSE    7400 IN  IN OUT
PINSWAP   7400 A  B
FUNCTION G1 7400  1  2  3
FUNCTION G2 7400  4  5  6
FUNCTION G3 7400  9  10 8
FUNCTION G4 7400 12 13 11
POWER   +5V; 14
GROUND  GND; 7
END
```

More Information

Aside from checking the syntax of the netlist and device files, the Netin process checks the following:

- netlist content: Reference designators in $NETS section must be in $PACKAGES.

- device file content: Compares physical pin numbers in function, power/ground, and NC statements against the pincount statement.

- netlist to device file: Compares reference designator pin numbers in the netlist against pin counts for associated device types. In the above example, the following error message would be generated:

pin number U1.20 not in device file for 74f00.txt ... pin ignored.

- Also compares power, ground and NC statements against the netlist.

The pins in the package symbol must match the pins you specify in the device file. Any mismatches will generate error messages.

Guidelines for Importing Logical Data

◆ To import, choose **File > Import > Logic**.

◆ Browse to the location of your Allegro netlist file; if your netlist does not have a *.txt* extension, set the Files of Type to All Files (*.*)

◆ Allegro reads and compiles the netlist and also updates the current board file (*.brd*) from the third-party format netlist.

◆ Be sure to set up device and net properties completely in the schematic environment so you can generate an Allegro-compatible netlist.

◆ Property names are case-sensitive. All Allegro property names attached to parts and nets in Capture or Capture CIS should be in upper case letters.

More Information

These are good guidelines to follow when importing a schematic netlist into Allegro.

Labs

◆Lab: Concept to Allegro

- Start the Project Manager.
- Open the *master.brd* design.
- Export schematic information from Concept to Allegro.
- Save the new *.brd* design containing both physical and netlist information.

◆Lab: Capture to Allegro

- Open the *master.brd* design.
- Set up the logic import from Capture in the *project2* directory.
- Import logic and save the new *.brd* design containing both physical and netlist information.

◆Lab: Importing a Third-Party Netlist

- Open the *master.brd* design.
- Set up the logic import for a third-party *.txt* file in the *project3* directory and device files in the *devices* directory.
- Import logic and save the new *.brd* design containing both physical and

More Information

The following labs will allow you to:

■   Familiarize yourself with the process required to import a Concept schematic into Allegro. You should only perform this lab if you do not plan to perform either the Capture to Allegro lab or the Third-party to Allegro lab.

■   Familiarize yourself with the process required to import a Capture schematic into Allegro. You should only perform this lab if you have NOT performed the Concept to Allegro lab and you do not plan to perform the Third-party to Allegro lab.

■   Familiarize yourself with the process required to import a Third-party netlist into Allegro. You should only perform this lab if you have NOT performed either the Concept to Allegro lab or the Capture to Allegro lab.

Note

Do only one of the following labs. Do not perform all three labs. Perform the lab that most closely represents your design philosophy at work.

Lab 6-1:   Concept to Allegro

Objective: Learn how to read a schematic database from Concept into an Allegro design file.

Library preparation work has already been completed for you. You are now ready to begin the layout process. The first step is to read a logical (schematic) database into a master design file (mechanical template).

Cadence has integrated schematic capture systems for use with Allegro software. This lab shows you how to use the Project Manager and work with data from the Concept tool.

Starting the Project Manager

A project configuration has been set up for you that defines schematic file libraries, and layout files associated with your project. Use one of the following methods to start the Project Manager on your platform.

Windows

1. Choose **Start > Programs > Cadence PSD 14.2 > Project Manager**.

    The Project Manager Product Choices window may appear.

2. If the Product Choices window appears, click the box labeled **Use As Default**, select **PCB Design Studio**, and click **OK**.

    The Project Manager form opens.

UNIX

1. In a UNIX shell window, enter the following command:

   **projmgr**

2. If the Product Choices window appears, click the box labeled **Use As Default**, select **PCB Design Studio** and click **OK**.

   The Project Manager form opens.

Opening the Project

Before the schematics were created, a project configuration was created that defined schematic and library paths and established a directory for the layout portion of the project in which you will be working. This directory, called *physical*, is situated in your classroom directory structure as follows:

..<course inst dir>

allegro/

project1/ —— **project1.cpm**

worklib/

root/

physical/

master.brd
placed.brd
routed.brd
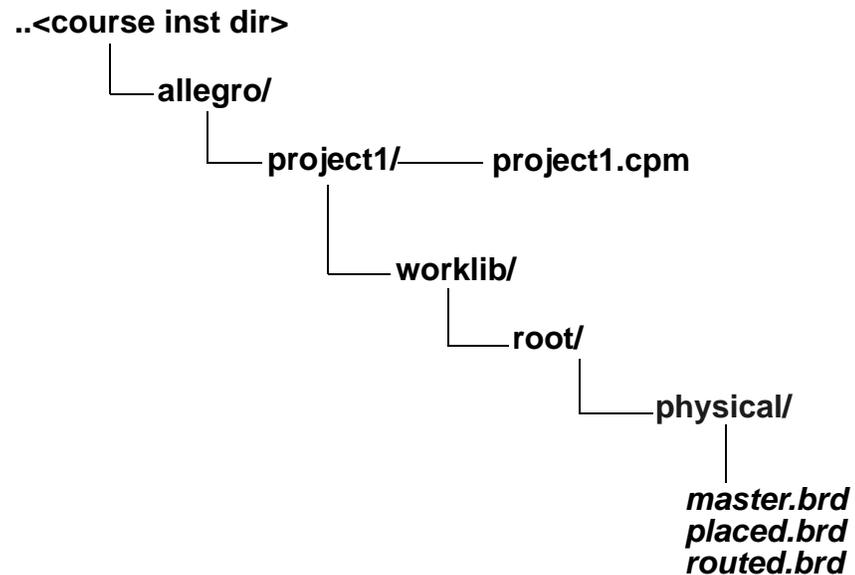
1. Click the **Open Project** button in the middle of the form.

   When you click **Open** in the Project Manager form, a file browser window appears.

2. Navigate to the *project1* directory. Select *project1.cpm*, then click **Open**.

   The Project Manager form changes and other large buttons appear.

Allegro Layout System   May 27, 2002
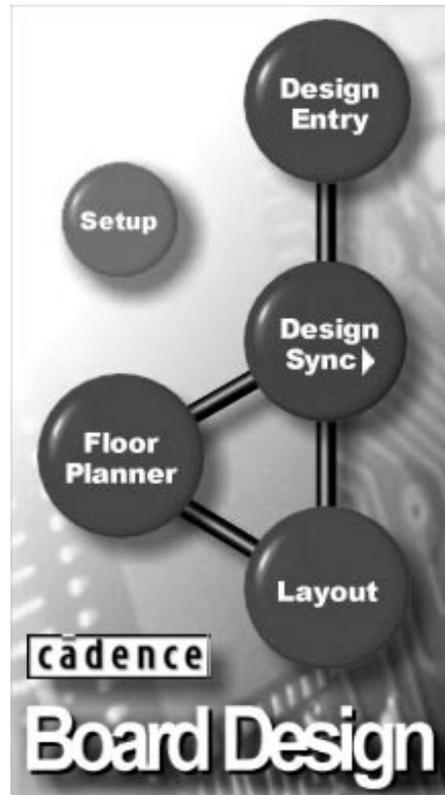
1. Click **Design Entry**.

   The Concept tool starts and a schematic appears. You will export data from this schematic into your layout, but first take a look at the schematic.

   DO NOT alter or make changes to the schematic.

2. Use the **Zoom In** and **Zoom Out** icons to explore the schematic pages.

   There are two pages to this schematic. You can use this group of icons as well as the **previous page** and **next page** icons to see the pages.

Synchronizing the Schematic Logic with the Physical Board

1. Select **File > Export Physical** from the Concept main menu.

   The Export Physical form appears.

2. Set the options in the Export Physical dialog box to match the figure.
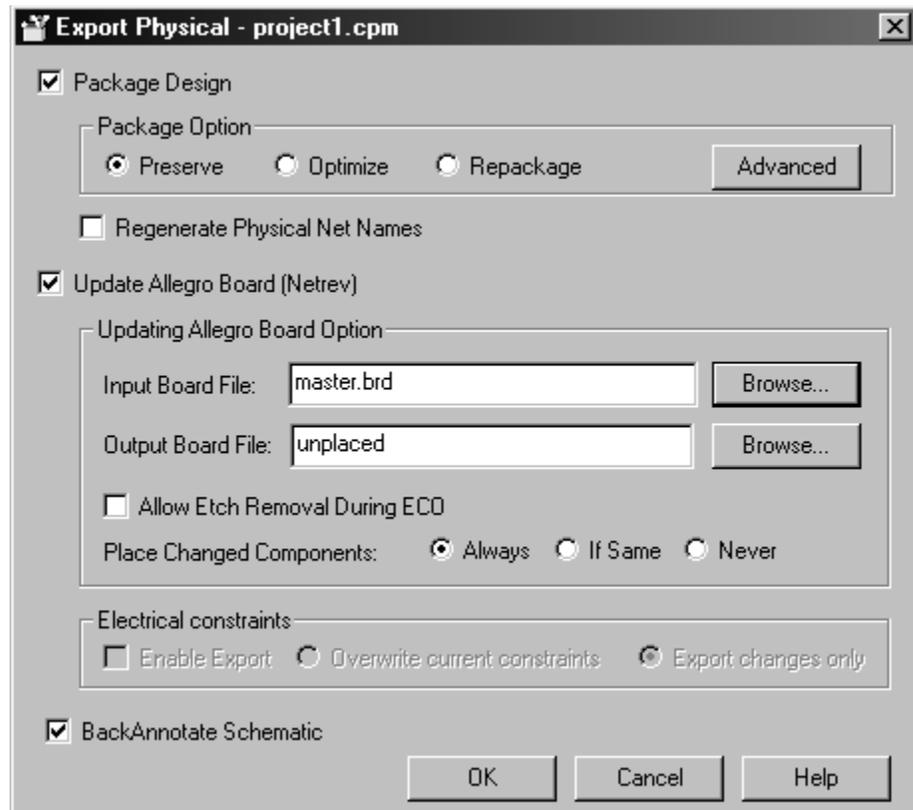
3. If the Input Board File does not display *master.brd*, click **Browse** next to the Input Board File field. In the Select Input Board File dialog box, select **master.brd** and click **OK**. This fills in the Input Board File field.

4. In the field labeled Output Board File, enter the following board name:

   unplaced.brd

   This will be the resulting file after reading in the schematic data.

5. Click **OK**.

   The schematic data is read into the *master.brd* file. The design is then written out as *unplaced.brd*. A message appears, asking if you want to check the results.

6. Click **Yes** to view the results.

The Progress dialog box appears. In this dialog box, you can scroll to view a report for the entire packaging and netlisting process. Also, from this dialog box, you can click View Results and access many other reports.

7. Close the Progress dialog box when you are finished viewing the report.

8. Select **File > Exit** to close Concept

9. Start Allegro.

Allegro opens the *unplaced.brd* design. This design looks exactly like the *master.brd* file you created in the previous lesson, except this one now has logical data in it and is ready for further processing and placement.

10. If the SigNoise Errors/Warning window appears, click **Close** to close this window.

11. At this point you can either exit from the Allegro program by choosing **File > Exit**, or you can leave the design open, ready to begin the next set of lab exercises.

12. End the Project Manager by selecting **File > Exit** from the Project Manager main window.

Note

When you exit from the Allegro program, files are saved that record your current working directory settings, as well as configuration settings and the last file you were working on. If you exit from the program at this point in the lab, you will find that when you restart Allegro it will automatically open the *unplaced.brd* file in the *<course inst dir>/allegro/project1/worklib/root/physical* directory.

STOP **End of Lab**

Lab 6-2:   Capture to Allegro

Objective: Learn how to read a Capture schematic into an Allegro design file.

1. If Allegro is not currently running, start the Allegro tool.

2. Open the *master.brd* design (if is not already open) from within the *project2* directory, as shown below:

```
.....<course inst dir>
         |
      allegro/
         |
   ┌─────┼─────────────┐
 play/  solutions/   project2/
                         |
                      master.brd
```
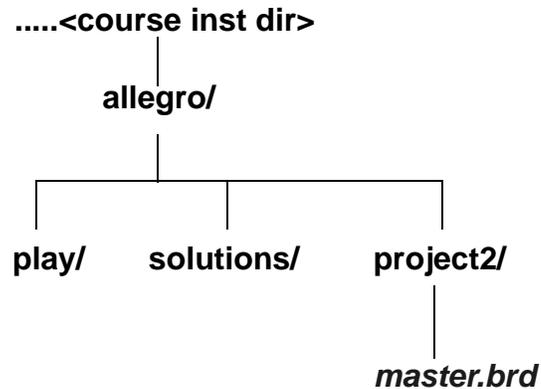
3. Choose **File > Import > Logic**.

   The Import Logic menu appears.

4. In the Logic Type section, click **Capture**.

5. In the Import From field, navigate to the *project2* directory.

   Your Import Logic dialog box should look this:
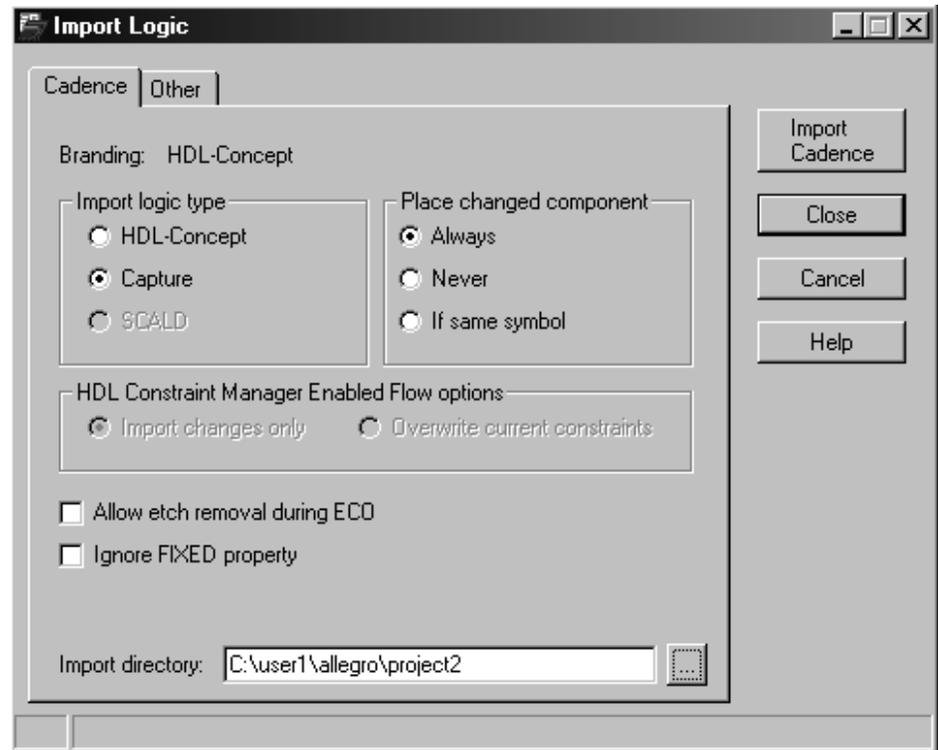
6. Click **Import Cadence**.

   The Capture schematic is checked and imported. If there are errors or warnings, the *netrev.lst* file automatically displays in a report window when the importing is done. If *netrev.lst* does not appear, select **File > Viewlog** to open this file.

7. Close the log file window.

   Next you will save this design in the *project2* directory.

8. Choose **File > Save As**.

   A file browser window opens.

9. In the File Name field, enter:

   unplaced.brd

10. Click **Save** to save the *unplaced.brd* file in the *project2* directory.

    The Capture schematic data has been combined with the master design file (mechanical template) to create a new Allegro design file called *unplaced.brd*. Use this design file to proceed to the next layout phase.

11. At this point you can either exit from the Allegro program by selecting **File > Exit**, or you can leave this design open, ready to begin lab exercises for the next lesson.

Note

When you exit from the Allegro program, files are saved that record your current working directory settings as well as configuration settings and the last file you were working on. If you exit from Allegro at this point in the lab, when you restart Allegro it will automatically open the *unplaced.brd* file in the *<course inst dir>/ allegro/project2* directory. This is what you want for the next lab.

End of Lab

Lab 6-3: Importing a Third-Party Netlist

Objective: Learn how to read a third-party schematic database into an Allegro design file.

Opening the master.brd File

1. If Allegro is not currently running, start the Allegro tool.

2. Open the *master.brd* design (if is not already open) from the *project3* directory, as shown below:
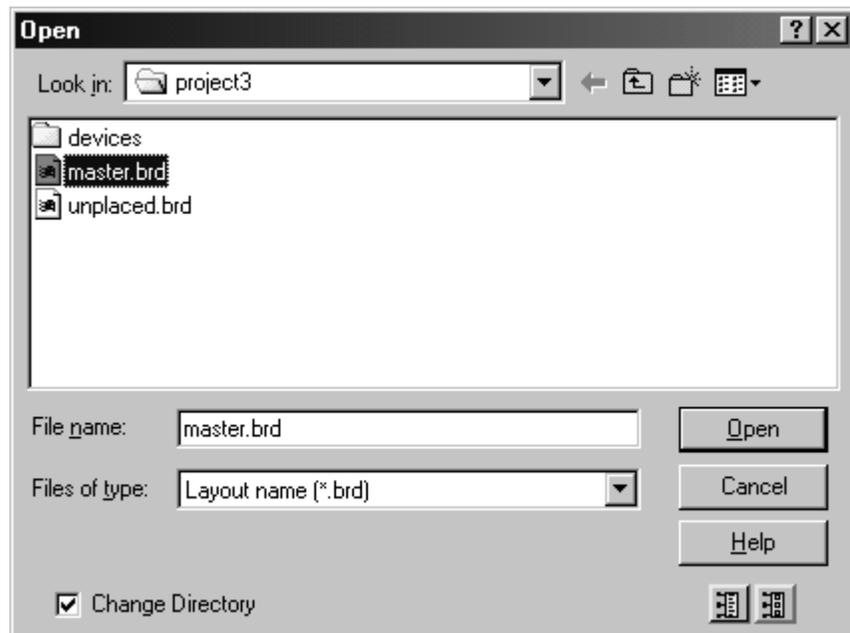
3. Choose **File > Import > Logic**.

    The Import Logic menu appears.

4. Select the **Other** folder tab.

5. In the Import Netlist field, enter:

    3rdparty.txt

6. Click **Import Other**.

    The third-party netlist data is checked and imported.

7. To view the log file that was created, choose **File > Viewlog**.

    A log file window appears. You may find some gate assignment warnings. These assignments will be taken care of during placement.

8. Scroll the log file to view it further.

9. Click **Close** to close the log file window.

    The third-party netlist data has been combined with the master design file (mechanical template) to create a new Allegro design.

    Next you will save this design in the *project3* directory.

10. Choose **File > Save As**.

    A file browser window opens.

11. In the File Name field, enter:

    unplaced.brd

12. Click **Save** to save the *unplaced.brd* file in the *project3* directory.

    The third-party schematic data has been combined with the master design file (mechanical template) to create a new Allegro design file called *unplaced.brd*. Use this design file to proceed to the next layout phase.

13. At this point you can either exit from the Allegro program by selecting **File > Exit**, or you can leave this design open, ready to begin the next lab exercises.

    ## Note

    When you exit from the Allegro program, files are saved that record your current working directory settings as well as configuration settings and the last file you were working on. If you exit from Allegro at this point in the lab, when you restart Allegro it will automatically open the *unplaced.brd* file in the *<course inst dir>/ allegro/project3* directory. This is what you want for the next lab.

    ## STOP End of Lab

Lesson 7:   Setting Design Constraints

## Learning Objectives

◆ Assign standard design rules.

◆ Assign extended design rules for spacing.

◆ Assign extended design rules for physical dimensions.

◆ Attach, change, and delete properties of components and nets.

Summary

In this section you will learn about setting your design rules. Design rules are known as Constraints in Allegro and are the rules that must be followed while routing your design. Typical constraints are the line width to be used during routing, line-to-line spacing, line-to-pad spacing, and so on.

Design Layout Process
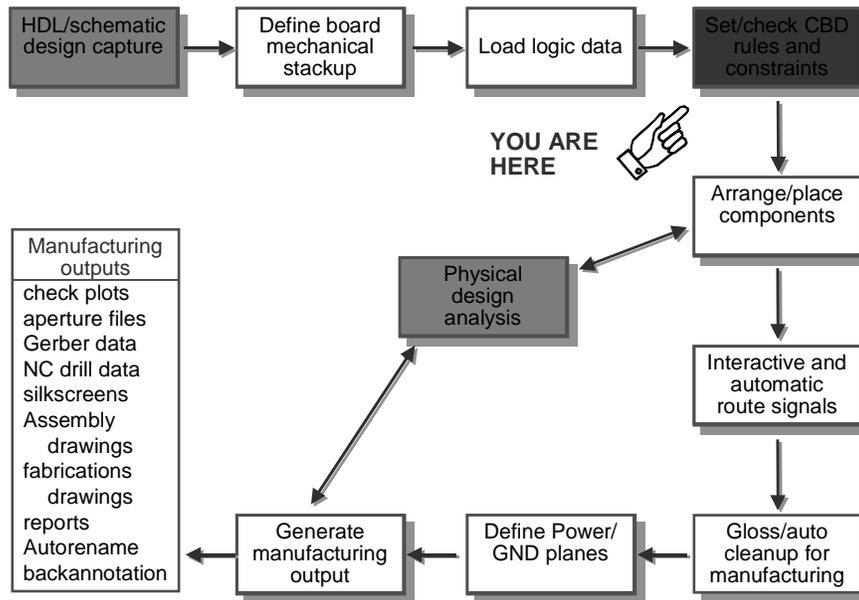
```
┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│ HDL/schematic│──▶│ Define board │──▶│ Load logic   │──▶│ Set/check CBD│
│design capture│   │  mechanical  │   │    data      │   │  rules and   │
│              │   │   stackup    │   │              │   │ constraints  │
└──────────────┘   └──────────────┘   └──────────────┘   └──────────────┘
```

YOU ARE HERE

```
                                                         ┌──────────────┐
                                                         │Arrange/place │
                                                         │ components   │
                                                         └──────────────┘
┌──────────────┐                    ┌──────────────┐
│Manufacturing │                    │  Physical    │
│   outputs    │                    │   design     │
│ check plots  │                    │  analysis    │
│ aperture files│                   └──────────────┘    ┌──────────────┐
│ Gerber data  │                                        │Interactive and│
│ NC drill data│                                        │  automatic   │
│ silkscreens  │                                        │ route signals│
│ Assembly     │                                        └──────────────┘
│   drawings   │
│ fabrications │   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│   drawings   │◀──│  Generate    │◀──│ Define Power/│◀──│ Gloss/auto   │
│ reports      │   │manufacturing │   │  GND planes  │   │ cleanup for  │
│ Autorename   │   │   output     │   │              │   │manufacturing │
│ backannotation│  └──────────────┘   └──────────────┘   └──────────────┘
└──────────────┘
```

More Information

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the design flow, the Set/check CBD (Correct By Design) rules and constraints step will now be discussed.

Introduction to Design Rules

There are four types of design rules:

- ◆ **Spacing Rule Set**: Clearances between lines, pads, vias, and copper areas (shapes)
- ◆ **Physical Rule Set**: Line width and layer restrictions
- ◆ **Design Constraints**: Package checks, soldermask checks and negative plane island checks
- ◆ **Electrical Constraint Sets**: Performance characteristics (crosstalk and propagation delay). *Not available in PCB Studio.*

There are two levels of detail for design rules:

- ◆ **Standard rules**: Describe the majority of nets in a design. These global rules are applied to all nets (all nets are created equal).
- ◆ **Extended rules**: Are performance related, and are assigned on a net-by-net basis. *Some rules not applicable in PCB Studio.*
  - ■ Timing and speed considerations (net length and propagation delay)
  - ■ Noise and distortion concerns (crosstalk, reflection, impedence).

More Information

The Allegro tool has a set of predefined rules, such as Line-to-Pin Spacing, or Minimum Line Width. You can define values for each rule within the context of a rule set. A rule set is a group of rules that have been bundled together to make value assignments easier for the user.

This rule 'bundling' is based upon the type of rule set.

- ■ **Spacing Rule Set** - constraints govern the spacing between objects on different nets (for example, line-to-thru-pin spacing).

- ■ **Physical Rule Set** - constraints govern physical construction of a net (for example, minimum line width and allowed etch layers).

- ■ **Design Constraints** - setting or unsetting of package DRC checking; Negative Plane Islands constraints; Soldermask constraints.

- ■ **Electrical Constraint Sets** - constraints govern electrical behavior and performance of an entire net (for example, maximum propagation delay). This constraint set is not available in the Studio product.

Setting up Design Rules

Setup > Constraints   or
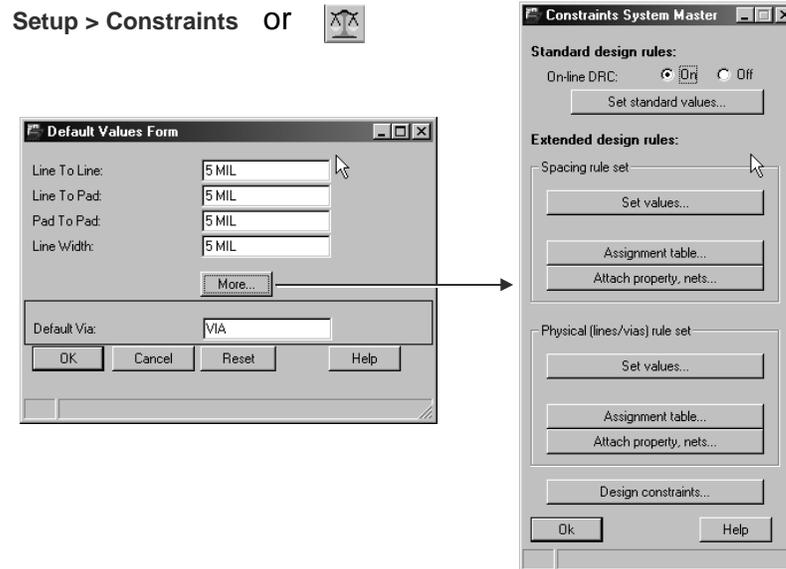
More Information

To set your design rules, use the **Setup > Constraints** command from the top menu, or select the **Constraint** icon. The Default Values Form, which is the initial form opened, is where you set the Standard Rules. You can access and create Extended Rules by selecting the **More** button from the Default Values Form.

Standard (default) Design Rules
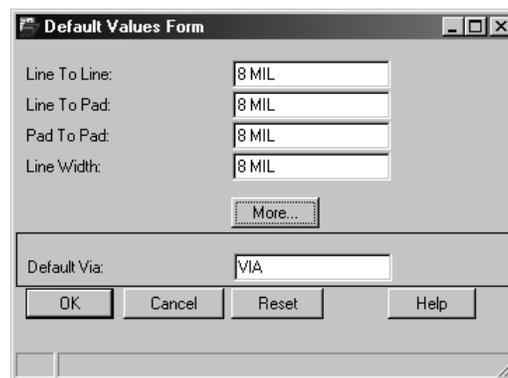
More Information

In the Default Values Form, you can define

■ **Line to Line Spacing** defines the clearance between two routing lines (edge-to-edge clearance or air gap).

■ **Line to Pad Spacing** defines the clearance between a routing line and a pad. In this case, a pad represents both a component pin and a routing via (edge-to-edge clearance or air gap).

■ **Pad to Pad Spacing** defines the clearance between any two pads. In this case, a pad represents both a component pin and a routing via (edge-to-edge clearance or air gap).

■ **Line Width** defines how wide a routing line should be.

■ **Default Via** defines which padstack should be used when a via is used in the design.

Lab

◆ Lab: Standard Design Rules
- Learn how to set up standard (default) constraints.
- Define basic constraints:
  ● Line to line
  ● Line to pad
  ● Pad to pad
  ● Line width
  ● Default via

More Information

The following labs will allow you to familiarize yourself with the process and steps required to set the Standard or Default design rules in your design.

Lab 7-1:   Standard Design Rules

Objective: Learn how to define a basic set of constraints in your design. In this lab, you define standard rules for all nets in the design.

Defining Basic Constraints

1. If you don't already have the Allegro tool running, start Allegro.

2. Choose **File > Open** and open the *unplaced.brd* design file you saved previously if it is not currently open.

3. Choose **Setup > Constraints** from the top menu.

   The Default Values Form appears.

4. Complete the form to match the following figure:

5. Click **OK** to exit from the Default Values Form.

   The Default Values form closes. If changes have been made, design rule checking (DRC) is automatically invoked.

   You just defined your standard rules for this design. For line-to-line, line-to-pad, and pad-to-pad you will be using 5-mil spacing. Also you defined the line width of 5 mils that is going to be used for all nets, and on all etch layers.

   These standard rules will now be referred to as the DEFAULT rule set. Unless otherwise specified, all nets will use these rules for routing.

6. Continue by choosing **File > Save As**.

   A browser form appears.

7. Rename this drawing by entering the following in the File Name field:

   constraints

8. Click **Save** to save the *constraints.brd* file.

The *constraints.brd* file is saved to disk.

Note

DO NOT exit from Allegro. The next lab will continue from this point.

STOP End of Lab

Extended Design Rules

Step 1: Create a "net class." (Which nets are special?)

Step 2: Create a rule set. (Why are they special?)

```
Constraints System Master           _ □ X

Standard design rules:

On-line DRC:        ○ On   ● Off

        Set standard values...

Extended design rules:

Spacing rule set
        Set values...

        Assignment table...
        Attach property, nets...

Physical (lines/vias) rule set
        Set values...

        Assignment table...
        Attach property, nets...

        Design constraints...

   Ok                    Help
```

Step 3: Apply rule set to net class.

More Information

As your designs become more complex, you will need to specify which nets require special consideration, and differentiate their requirements from the default rules. To do this, you select the **More** button in the Default Values Form, which will display the Constraints System Master form.

The first step is to identify which net(s) is special or different from the default rules. This is done with the **Attach Property, Nets** button in the Spacing or Physical Rule Set section (depending upon the type of constraints you need to define).

Once you have identified which net(s) is special, the next step is to specify why or how they are different. This is done with the **Set Values** button in the Spacing or Physical Rule Set section (depending upon the type of constraints you need to define).

The final step is to apply the new rule set created in step two to the net(s) you identified in step one. This is accomplished with the **Assignment Table** button.

Spacing Rule Set—Step 1
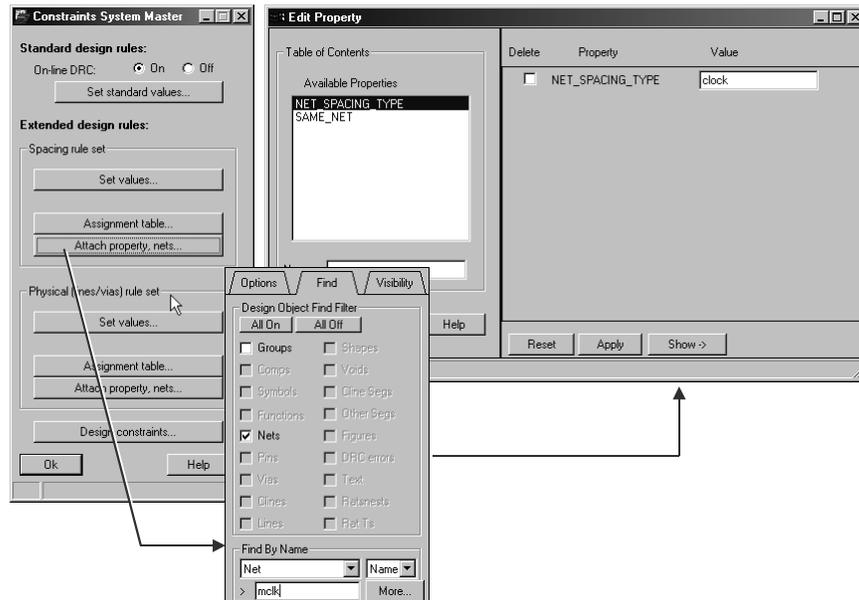
More Information

If your extended design rules require a different spacing requirement for special nets, the Attach Property, Nets option in the Spacing Rule Set section lets you attach a property that identifies these nets.

Use the Find Filter to specify the net(s) involved, and select the NET_SPACING_TYPE property from the Edit Property form. The value you assign to the NET_SPACING_TYPE property is then applied to the selected nets. Apply a value that represents a group or class of nets that is meaningful (such as clock, data, address, critical, high speed, ecl and so on).

By attaching the NET_SPACING_TYPE property, you identify which net(s) require special consideration.

Spacing Rule Set—Step 2
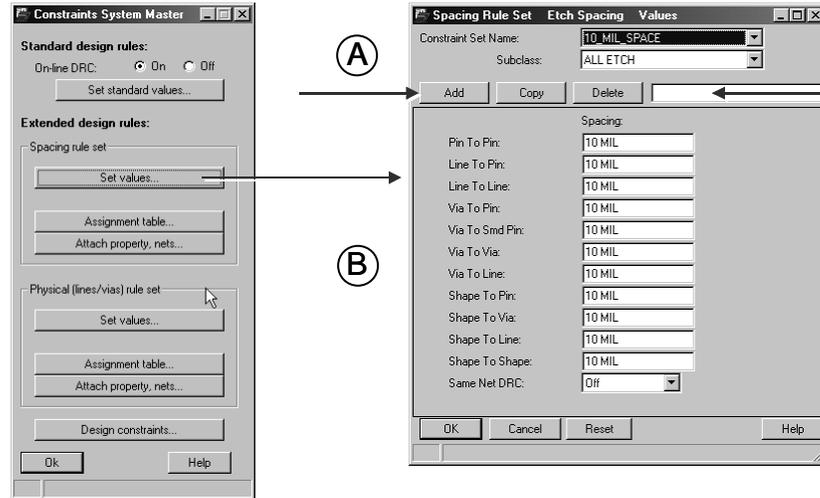
More Information

Now that you have identified which net(s) require special consideration, use the Set Values command to create the corresponding rule set that defines those requirements.

- Section A: Type in the name of the spacing rule set you want to create (be descriptive), and click **Add**. In this section you can also delete or copy rule sets. The maximum length is 31 characters. All special characters are allowed except ! @ ? '. Be careful using the asterisk (interprets * as a wildcard).

- Section B: Specify the line, pin, via, and shape spacing values as required, by typing their values in the field to the right of each element pair.

The Same Net DRC: On or Off option checks spacing constraints between connect lines having the same net name.

Spacing Rule set—Setting Rules by Layer

Click here …

… for these options
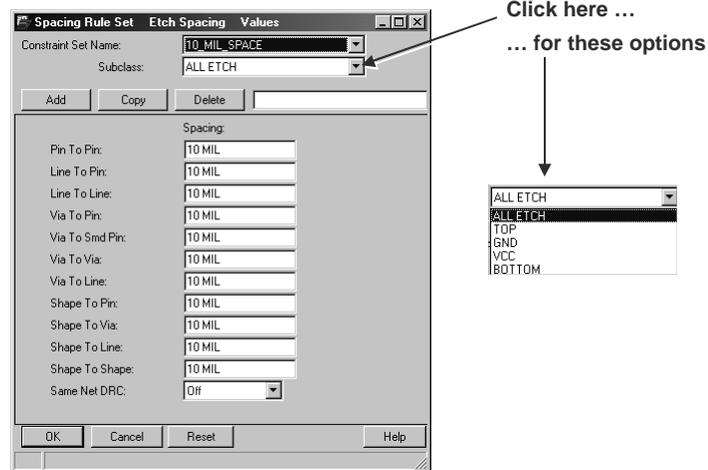
More Information

You can specify the same clearances for all routing layers in the design by selecting the ALL ETCH value in the Subclass field. If you require different clearances on different routing layers, use the scroll button in the Subclass field to select a specific layer and enter the required spacing values. The spacing values you enter apply only to the current layer selected. The layers available are based upon the current design layer stackup.

Spacing Rule Set—Step 3

When a "clock" net routes next to another "clock" net, the 10_MIL_SPACE rules are used.
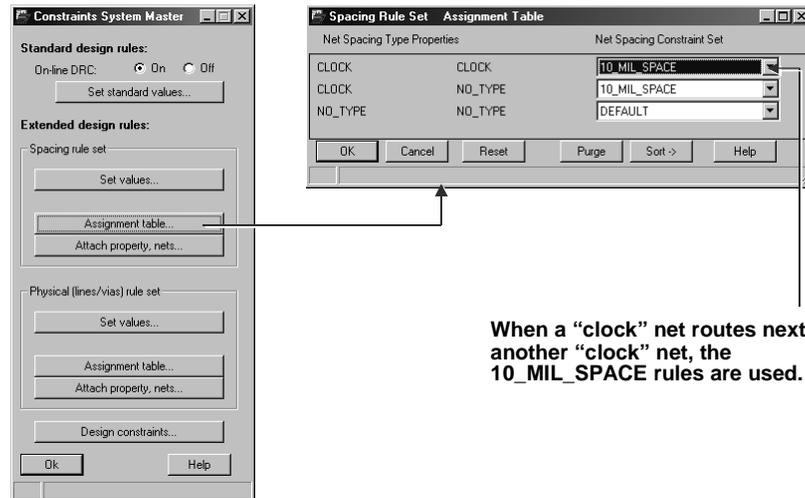
More Information

Now that you have created a net class and a rule set, you must assign the rule set to the net class using the Assignment Table.

The Assignment Table displays all current net class combinations. NO_TYPE stands for the default class (see Standard Design Rules). Use this form to correspond a spacing rule set to a specific combination of net classes.

In the example shown, there are three table entries. Each entry represents a unique combination of the default and clock net classes. The first entry (NO_TYPE to NO_TYPE) means that if two nets belonging to the default net class are adjacent, then the default spacing rule applies (see Standard Design Rules).

The second entry (CLOCK to NO_TYPE) represents two adjacent nets; one belongs to the clock class and the other belongs to the default class. In this case, the 10_MIL_RULE rule applies because the clock nets are sensitive to noise (crosstalk).

The third entry (CLOCK to CLOCK) means that if two nets belonging to the clock class are adjacent, then the 10_MIL_RULE rule applies. (Optionally, you can apply the default spacing, or any other existing spacing rule set.)

Use the scroll button in the Net Spacing Constraint Set field to select from a list of existing spacing rule sets.

Lab

◆ Lab: Extended Design Rules—Spacing

■ Create a spacing net group.

■ Define the spacing rules.

■ Set up the assignment table.

More Information

The following lab will allow you to familiarize yourself with the process required to create extended spacing design rules. You will learn how to identify the special nets, create new design rules, and apply the new design rules to the special nets.

Lab 7-2: Extended Design Rules—Spacing

Objective: Define design rules for special nets.

You use the Extended Design Rules section when you need to specify design rules on a net-by-net or layer-by-layer basis. The Extended Design Rules section is divided into two basic areas:

◆ Spacing Rules

◆ Physical (Lines/Vias) Rules.

In this lab, you will use the Spacing Rule Set section of the Constraints System Master.

Creating a Spacing Net Group

Assume two nets called VCLKA and VCLKC require more clearance than the default spacing defined in the previous lab.

1. Choose **Setup > Constraints** from the top menu and click **More** in the Default Values Form.

   The Constraints System Master dialog box appears.

2. In the Spacing Rule Set section, click **Attach property, nets**.

3. Click the **Find** tab to bring the Find Filter to the front.

4. If the Find By Name section is not set to Net, use the Find By Name drop-down list to set the field to **Net**.

5. Place the cursor in the blank Find By Name field, and enter:

   vclk*

   When you press the Enter key, the Edit Property form appears. The Edit Property form displays a list of spacing-related properties that are also available for attachment.

6. In the Edit Property dialog box, click on **NET_SPACING_TYPE**.

   This property now appears to the right of the table.

7. In the blank field next to NET_SPACING_TYPE property, enter this name for the spacing net class:

sync

```
Edit Property                                                    _ □ ×

Table of Contents                   Delete        Property              Value

Available Properties                 ☐      NET_SPACING_TYPE      sync
NET_SPACING_TYPE
SAME_NET
```
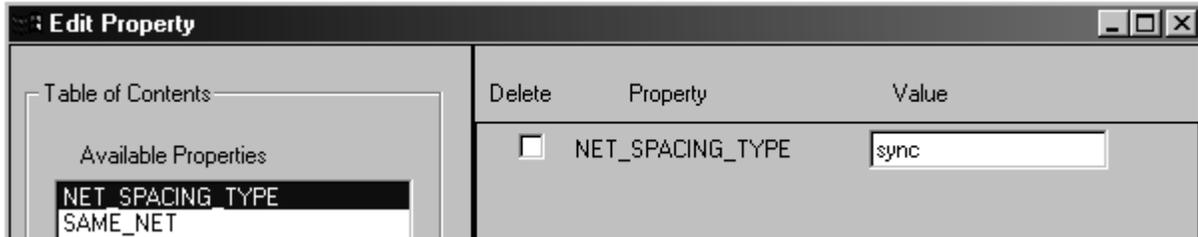
8. Click **Apply**.

In the Show Properties dialog box, the property NET_SPACING_TYPE is added to both nets.

```
Show Properties                                              _ □ ×
File   Close   Help

Net: VCLKC
    NET_SPACING_TYPE = SYNC
    LOGICAL_PATH = @project1_lib.root(sch_1):vclkc

Net: VCLKA
    NET_SPACING_TYPE = SYNC
    LOGICAL_PATH = @project1_lib.root(sch_1):vclka
```
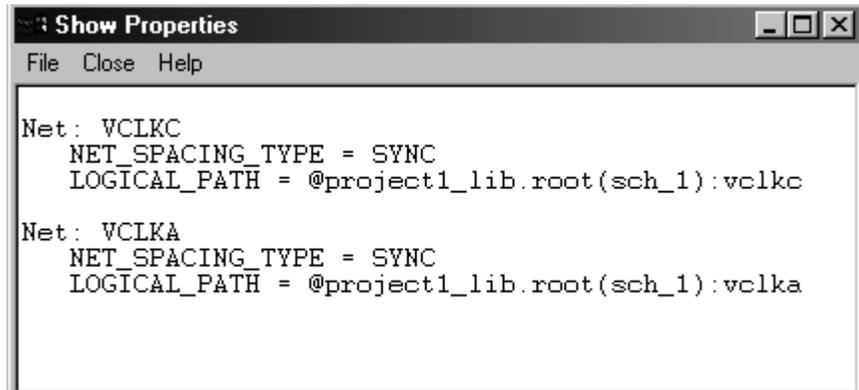
9. In the Edit Property form, click **OK** to exit.

The Show Properties window also closes.

You have just created a special net class called *sync*. Both the nets called VCLKA and VCLKC are members of this class. If there were other nets that required the same special clearance, you would need to add them to this net class also.

Defining the Spacing Rules

Now that you have identified the nets that need more clearance, you need to define how much clearance is required.

1. In the SPACING RULE SET section of the Constraints System Master form, click on **Set values**.

The Etch Spacing Values form appears. At the top of the form is the Constraint Set Name field (set to **DEFAULT**).

The form currently displays the spacing rules for the default rule set (defined in the previous lab). All nets that do not have an assigned NET_SPACING_TYPE property belong to this rule set by default.

2. To generate the spacing rule set required for net class sync, click in the blank field to the right of the DELETE button, and type:

    8_mil_space

Note

DO NOT press the Enter key.

3. Click **ADD**.

    The new spacing rule name appears in the Constraint Set Name field.

4. Change the values in the Spacing fields as shown below, from 5 mils to 8 mils, then click **OK**.
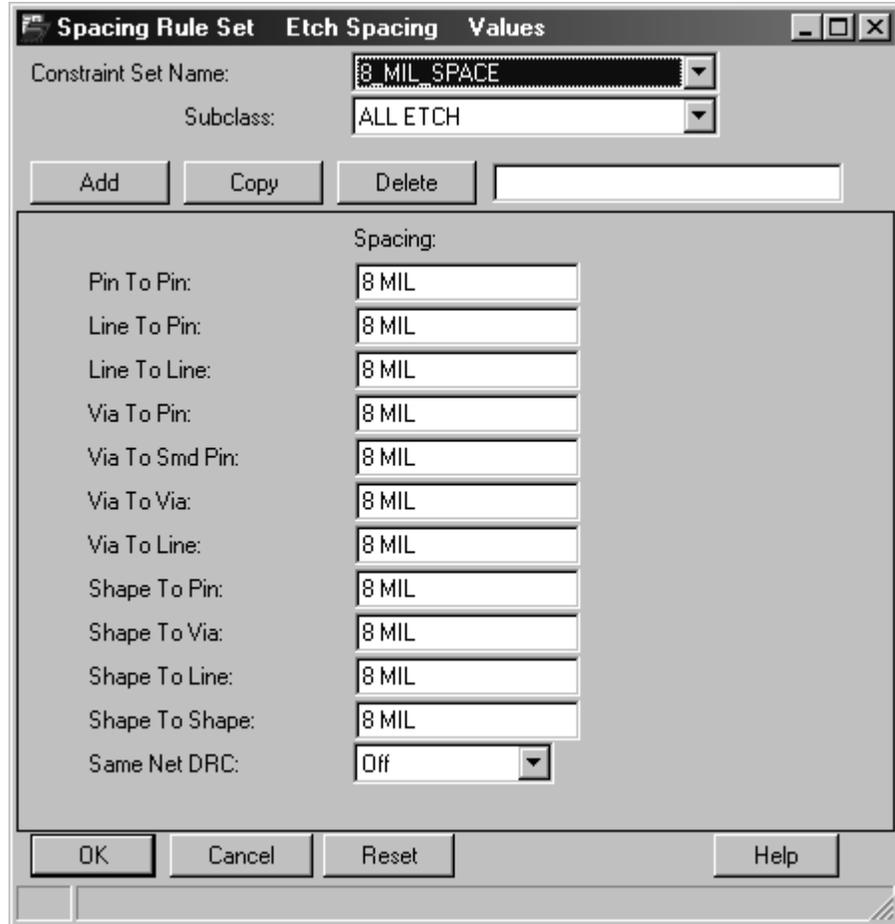
Setting Up the Assignment Table

Now that you have identified the nets requiring additional clearance (net group sync), and you have defined the spacing rules (rule set 8_MIL_SPACE), you need to assign the rule set to the net class.

1. In the SPACING RULE SET section of the Constraints System Master form, click **Assignment Table**.

    The Assignment Table form appears listing all the spacing net classes that exist in the design, in all possible combinations. These net class combinations are shown as pairs of Net Spacing Type Properties. The NO_TYPE net class represents all the nets that have no special spacing requirements (nets that obey the default rules).

2. Change settings in the Net Spacing Constraint Set field, as shown in the figure:
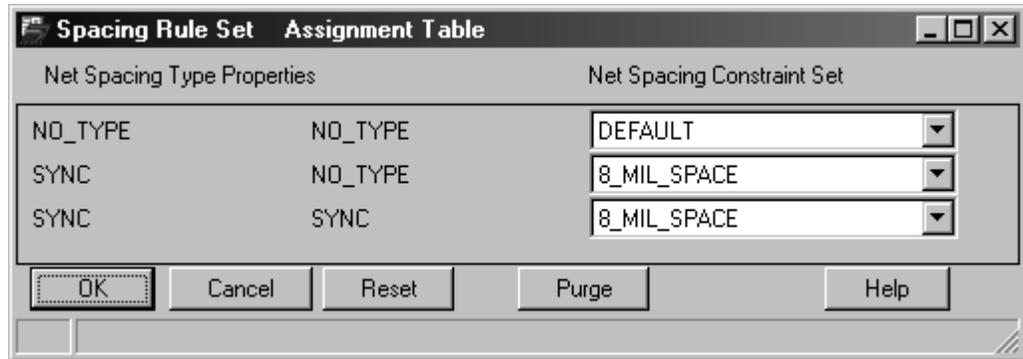
When two default nets route next to each other, they will obey the default spacing rules (5 mils). When a sync net routes next to a default net, or two sync nets route next to each other, they will obey the 8_MIL_SPACE rule set (8 mils spacing).

3. Click **OK** to close Assignment Table form.

4. Click **OK** to close the Constraints System Master form.

5. Save the drawing and continue by clicking **File > Save**.

6. Click **Yes** to confirm the overwrite.

The *constraints.brd* file is once more saved to disk.

 End of Lab

Physical Rule Set—Step 1
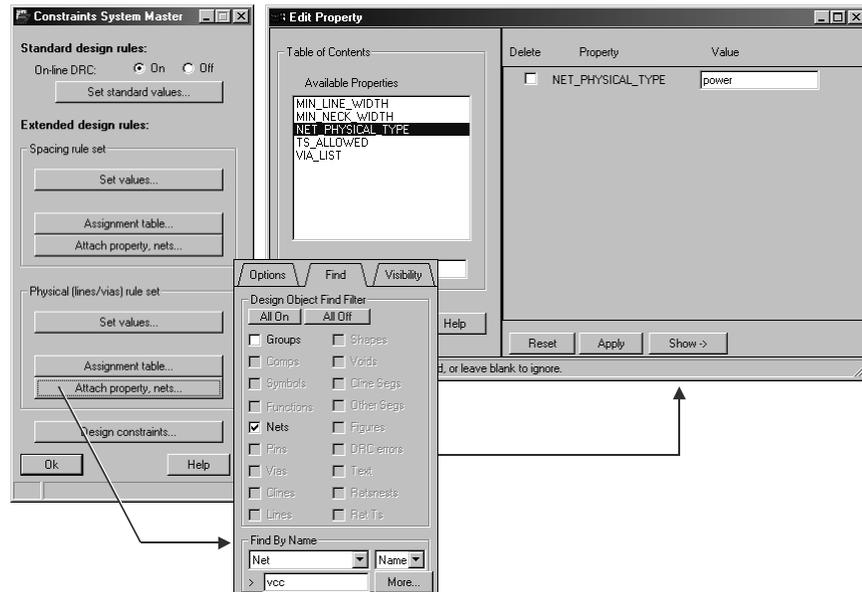
More Information

If your extended design rules require a different line width requirement for special nets, different via padstacks for special nets, and so on, the **Attach Property, Nets** command in the Physical Rule Set section lets you attach a property that identifies these nets.

Use the Find Filter to specify the net(s) involved, and select the **NET_PHYSICAL_TYPE** property from the Edit Property form. The value you assign to the NET_PHYSICAL_TYPE property is then applied to the selected nets. Apply a value that represents a group or class of nets that is meaningful (such as clock, data, address, critical, high speed, ecl and so on).

Physical Rule Set—Step 2
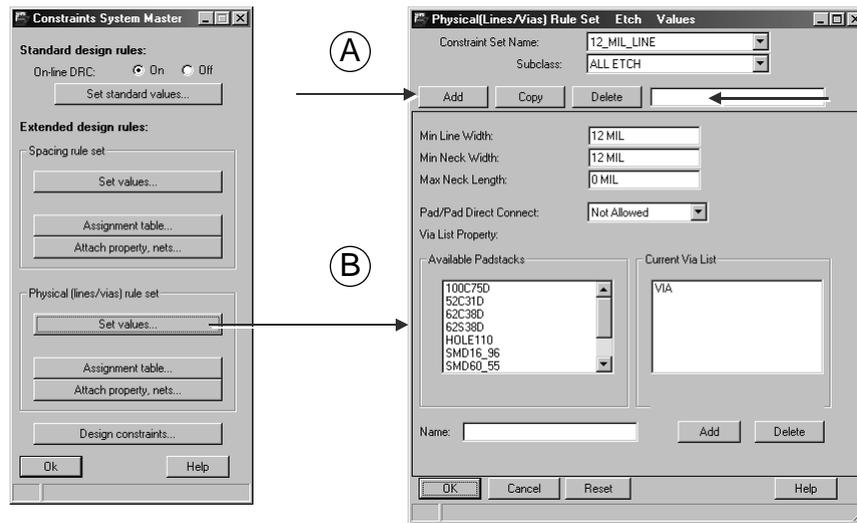
More Information

Now that you have identified which net(s) will require special consideration, the **Set Values** command lets you create the corresponding rule set to define those requirements.

- ■ Section A: Type in the name of the physical rule set you want to create (be descriptive), and select the **Add** button to the left. In this section you can also delete or copy rule sets. The maximum length is 31 characters. All special characters are allowed except ! @ ? '. Be careful using the asterisk (interprets the * as a UNIX wildcard).

- ■ Section B: Specify the minimum line width value as required.

Constraint	Description
Min Line Width	Specifies the width of conductor traces.
Min Neck Width	Specifies neckdown trace width (interactive routing only).
Max Neck Length	The maximum length of a neckdown trace segment.
Pad/Pad Direct Connect	Options are All Allowed, Via/Pin Allowed, Via/Via Allowed and Not Allowed. Determines whether connections are allowed to occur without the need for traces.
Via List Property	Displays a list of all padstacks in your design. Click on a padstack name to move it from the Available Padstacks list to Current Via list.

Physical Rule Set—Etch by Layer

Click here …

… for these options
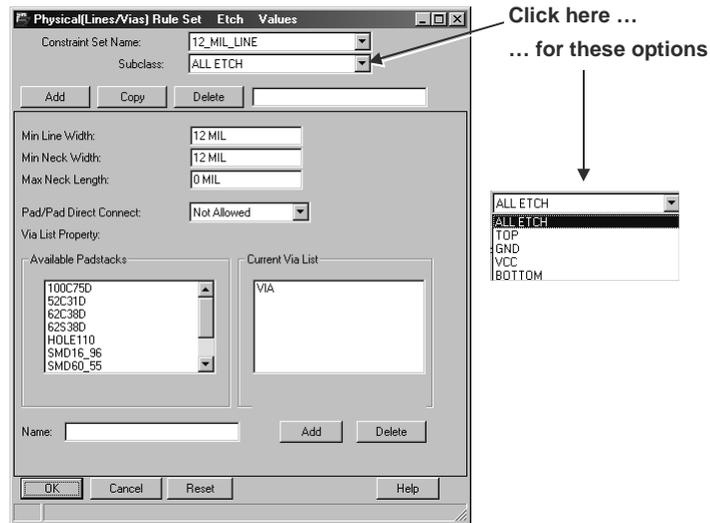
More Information

You can set separate (different) line width values for each ETCH layer. Use the scroll button in the Subclass field to select a specific layer. The values you enter apply to the current layer only.

The ALL ETCH selection sets physical values for all ETCH subclasses. Use this setting if all (or most) of your layers have the same physical rules.

Physical Rule Set—Step 3
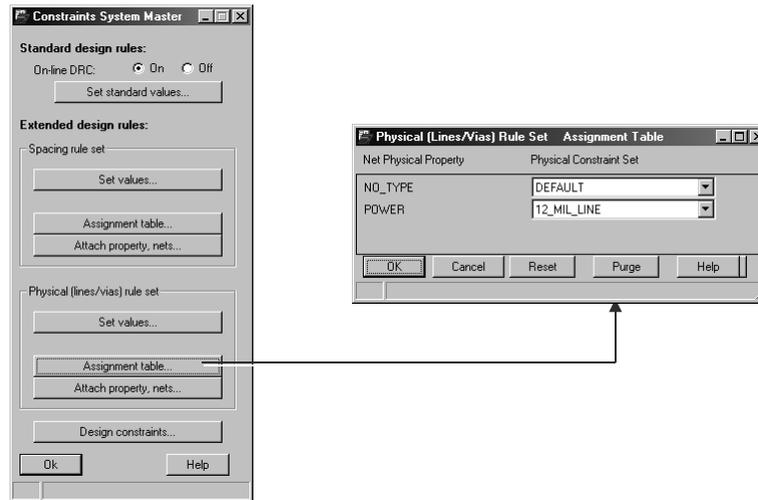
More Information

Now that you have created a net class and a rule set, you assign the rule set to the net class using the Assignment Table.

The Assignment Table displays all physical net classes. NO_TYPE stands for the default class (see Standard Design Rules). Use this form to correspond a physical rule set to a specific physical net class.

The first entry (NO_TYPE) means that the default net class is governed by the DEFAULT physical rule set (see Standard Design Rules).

The second entry (POWER) means the power net class is governed by the 12_MIL_LINE physical rule set.

Use the Purge button to remove unassigned physical net classes from the table.

Lab

◆ Lab: Extended Design Rules—Physical
  ■ Create a physical net class.
  ■ Define the spacing rules.
  ■ Set up the assignment table.

More Information

The following lab will allow you to familiarize yourself with the process required to create extended physical design rules. You will learn how to identify the special nets, create new design rules, and apply the new design rules to the special nets.

Lab 7-3:   Extended Design Rules—Physical

Objective: Define design rules for special nets.

This lab uses the Physical (Lines/Vias) Rule Set section of the Constraints System Master.

Creating a Physical Net Class

Besides more spacing, assume the nets VCLKA and VCLKC also require a larger line size.

1. If the Constraints System Master form is closed from the previous lab, choose **Setup > Constraints**, then click **More**.

    The Constraints System Master form appears.

2. In the Physical (Lines/Vias) Rule Set section of this form, click **Attach property, nets**.

3. Click the **Find** tab to bring the Find Filter to the front.

4. Click the scroll bars in the Find By Name section and select the **Net** and **Name** options, if these are not already selected.

5. Place the cursor in the blank Find By Name field, and enter:

    vclk*

    The Allegro message tells you that both nets have been selected. Also the Edit Property and the Show Properties forms appear.

6. In the Edit Property form, from the list of properties, click on **NET_PHYSICAL_TYPE**.

   This property appears to the right of the table.

7. In the blank field next to the NET_PHYSICAL_TYPE property, enter the name of the physical net class:

    sync
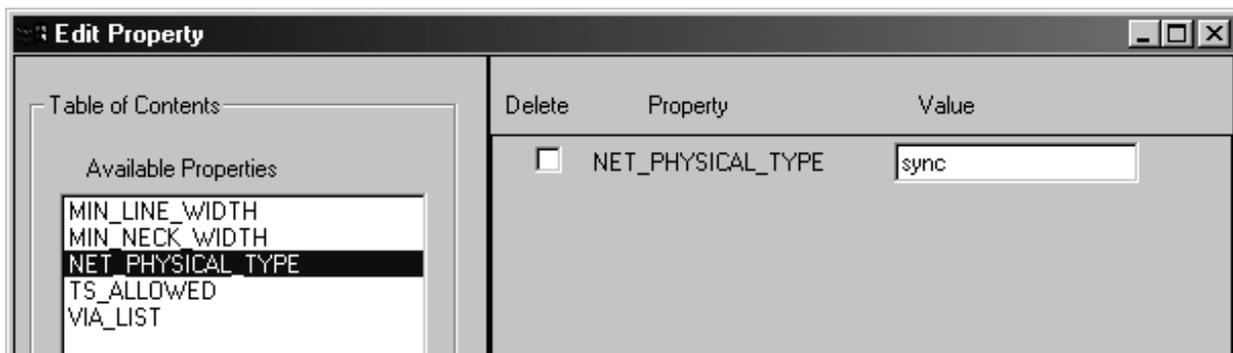
8. Click **Apply**.

In the Show Properties window, the property NET_PHYSICAL_TYPE is added to the net VCLKA and VCLKC.

```
Show Properties                                    _ □ X
 File  Close  Help

Net: VCLKC
    NET_PHYSICAL_TYPE = SYNC
    NET_SPACING_TYPE = SYNC
    LOGICAL_PATH = @project1_lib.root(sch_1):vclkc

Net: VCLKA
    NET_PHYSICAL_TYPE = SYNC
    NET_SPACING_TYPE = SYNC
    LOGICAL_PATH = @project1_lib.root(sch_1):vclka
```
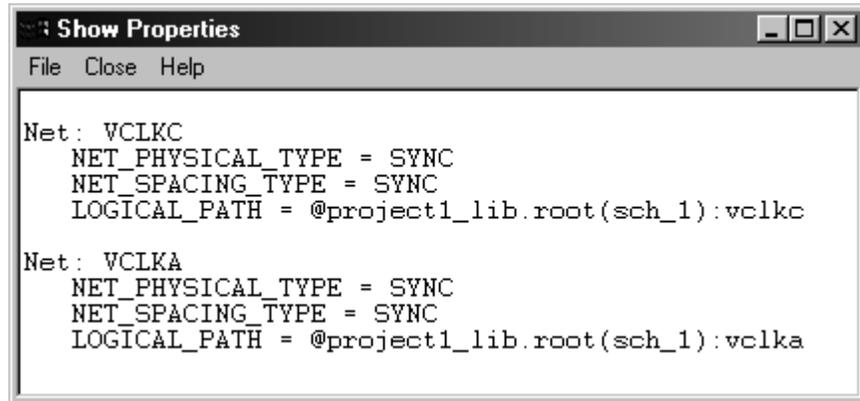
9. In the Edit Property form, click **OK**.

The Edit Property and Show Properties forms close.

Defining Physical Rules

Now that you have identified the nets that need a special line size, you need to define what that line size is.

1. In the Physical (Lines/Vias) Rule Set section of the Constraints System Master form, click **Set values**.

The Etch Values form appears. At the top of the form is the Constraint Set Name field (set to DEFAULT).

The form currently displays the physical rules for the default rule set which you defined in the first lab of this lesson. By default, all nets that do not have an assigned NET_PHYSICAL_TYPE property belong to this rule set.

2. To generate the physical rule set required for net class sync, click in the blank field to the right of the DELETE button, and type:

8_mil_line

```
Physical(Lines/Vias) Rule Set   Etch   Values          _ □ X
 Constraint Set Name:    DEFAULT          ▼
         Subclass:       ALL ETCH         ▼
   [ Add ]   [ Copy ]   [ Delete ]   [8_mil_line            ]
```
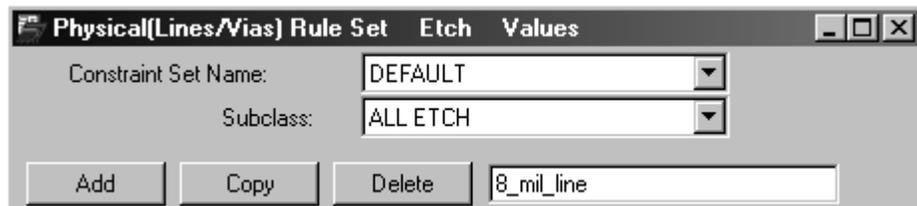
Note

DO NOT press the Enter key.

3. Click **ADD**.

The new physical rule set name appears in the Constraint Set Name field above.

4. Change the details in the Etch Values form as shown in the figure:


5. Click **OK** to close the form.

Setting Up the Assignment Table

Now that the nets requiring larger lines have been identified (net class sync), and the physical rules have been defined (rule set 8_MIL_LINE), you need to assign the rule set to the net class.

1. In the Physical (Lines/Vias) Rule Set section of the Constraints System Master form, click **Assignment Table**.

The Assignment Table form appears. It lists all the physical net classes that exist in the design under the Net Physical Property column. The NO_TYPE net class represents all the nets that have no special physical requirements (nets that obey the default rules).

**2.** Set the options under the Physical Constraint Set field to reflect the following:
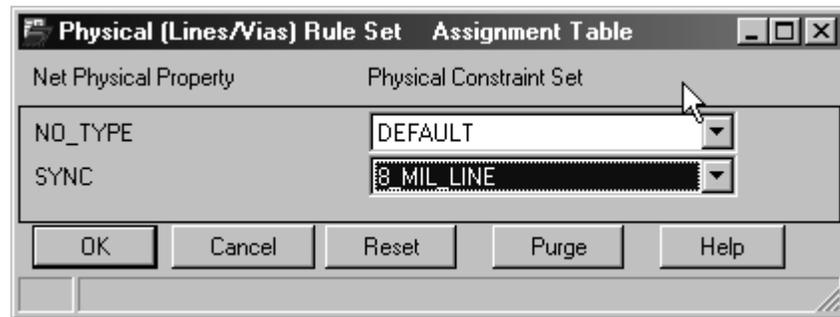
3. In the Assignment Table form, click **OK**.

4. Click **OK** to close the Constraints System Master form.

5. Save the drawing and continue by choosing **File > Save**.

6. Click **Yes** to confirm overwrite.

The *constraints.brd* file is saved to disk.

STOP **End of Lab**

Design Constraints
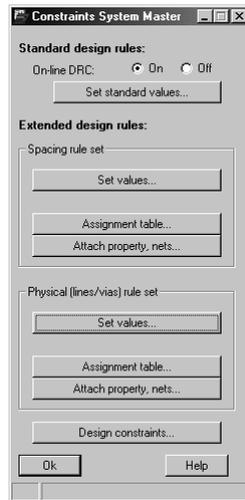
NOTE: DRC control not
available in PCB Studio
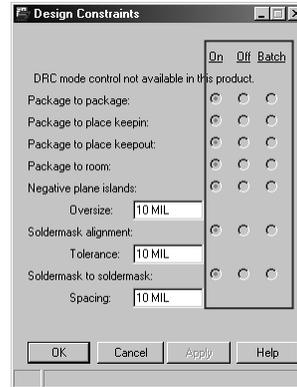
More Information

The Design Constraints form is used to set part placement checks, soldermask checks and negative plane island checks. All of these rules are checked at the global level. This means these checks are run on the entire design.

The constraints Package to Package, Package to Place Keepin and Package to Place Keepout check the package boundary of a footprint (defined as a shape in the Allegro Symbol Editor) against other footprint package boundaries, against the placement keepin shape, and against placement keepout shapes. A DRC will be generated if there is any overlap between the appropriate type of shapes.

In order for DRCs to be generated for the constraint Package to Room, you must also attach the property ROOM_TYPE with the value of HARD to the room.

The constraint Negative Plane Islands is used to check for isolations when using a negative plane. These islands are usually formed by a series of overlapping thermal reliefs and/or anti-pads creating a disconnect between two or more pieces of copper. The Oversize value is used to increase the pad geometry before the checks for shape islands is done.

The Soldermask Alignment constraint checks regular pad to soldermask pad clearance and part soldermask clearance (checks shape/frectangle on PACKAGE GEOMETRY, SOLDERMASK Top or Bottom against the place bound shape/frectangle).

The Soldermask To Soldermask constraint checks for a minimum spacing between any type of soldermask defined in the design (pin/via/part soldermask).

Property Assignments and Changes

Edit > Properties

Properties to delete or change

List of available properties
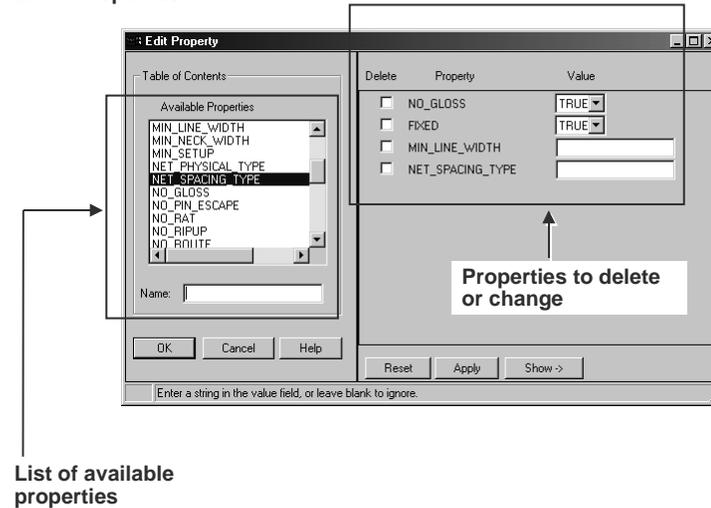
Summary

It is important to understand that there is overlap between properties and constraints. Properties override constraint values. For example, a design contains a special net class with an assigned physical rule set. This rule set calls out a Minimum Line Width of 8 mils. If the property min_line_width is set to 10 and is assigned to one or more nets from that group, those nets will obey the property value rather than the physical rule set value. Therefore, in this case, the net will be routed at a 10-mil line rather than an 8-mil line.

More Information

When you select the **Edit > Property** command, you must first identify the elements for property assignment. Use the Find Filter form to select elements either by pick or by element type plus name or list. Use the Find By Name/Prop section of the Find Filter to identify elements with existing properties. The Allegro tool then displays the properties available for that element type. Two examples of element types and their properties are:

- Components and component properties
- Nets and net properties

Once an element is identified, the Edit Property form appears. The Edit Property form lets you assign properties to design elements, or delete or modify the current values of an assigned property.

Select the properties you want to attach from the scroll list and click on the **Apply** button. Some properties require values (for example, min_line_width) while others do not. To modify existing property values, follow the same process. To remove an existing property, click the **Delete** button next to the selected property before applying.

DRC Marker Display

DRC markers store the following information about a design rule violation:
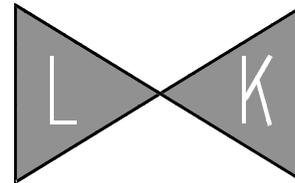
- ◆ DRC class, subclass, and location
- ◆ Type of constraint set (spacing, physical, or electrical)
- ◆ Name of constraint set
- ◆ Constraint type being violated (for example, *Line to Thru Pin Spacing*)
- ◆ Data concerning first element in violation (type of element, location, refdes, if a package/part, and so on)
- ◆ Data concerning second element (if there is one) in violation (type of element, location, refdes, if a package/part, and so on)

More Information

DRC markers have two characters, one in each side of the 'bow-tie', that identify the type of constraints violation being marked. Each character is a key as to what type of violation exists. In the example shown, the "L" represents a "Line." The "K" represents a "Keepout" (such as a routing keepout). So therefore, in this case, this is a line to routing keepout violation. In other words, a piece of etch exists in an area that has been identified as a routing keepout area.

To display the DRC filled, as shown in the example, enter on the Allegro command line "set display_drcfill" or use the User Preferences Editor. The display_drcfill option can be found under the Display category.

Lab

◆ Lab: Working with Properties

■ Learn to use the Edit Properties form to add, delete, and change property-value assignments.

● Attach properties to components.

● Add a ROOM property.

● Attach properties to components.

● Show existing properties on design elements.

● Delete properties.

More Information

The following lab will allow you to familiarize yourself with the process required to work with the design constraints and add, modify and delete properties. You will learn how to modify the design constraints, attach properties to nets, components and areas, show existing properties, and delete properties from database elements.

Lab 7-4:   Working with Properties.

Objective: Learn to attach, display, and delete properties in a design.

Attaching Properties to Components

In this section, you will attach properties to components and nets.

1. Start the Allegro tool and open the *constraints.brd* file in your working directory if it is not already the open design.

2. Choose **Edit > Properties** from the top menu.

3. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Comp (or Pin)**.

4. Click in the text entry field, and enter:

   `j1`

   When you press the Enter key, the Edit Property and the Show Properties forms appear. Notice that the J1 connector has no properties attached to it.

5. In the Edit Property form, select the **HARD_LOCATION** and **FIXED** properties from the scroll list.

   These properties appear on the right.
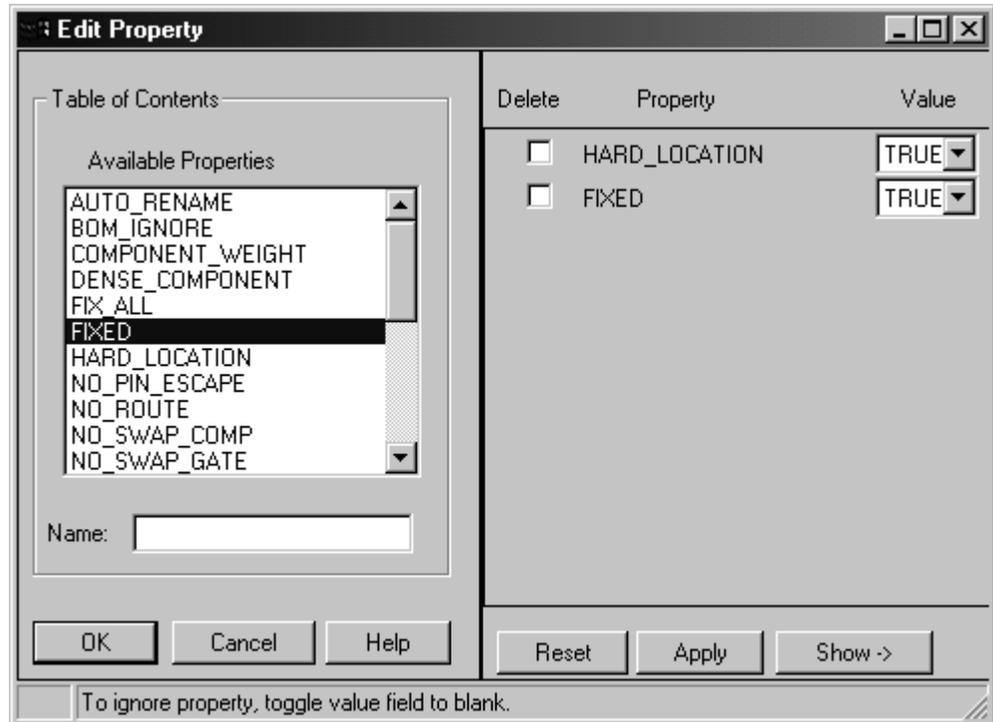
6. Click **Apply**.

In the Show Properties window, the properties HARD_LOCATION and FIXED are added to component J1.
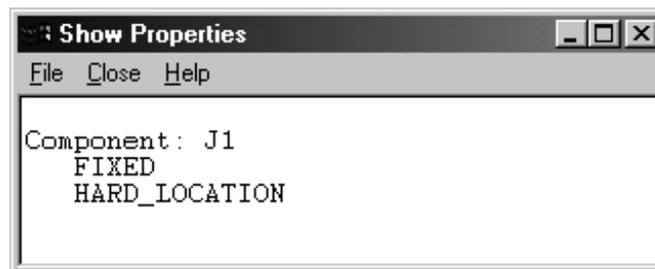
Note

The FIXED property prevents the component from being moved. The HARD_LOCATION property prevents the component reference designator from being changed during the automatic rename process.

7. Click **Close** to close the Show Properties window.

8. Click **OK** to close the Edit Property form.

Adding the ROOM Property

1. Choose **Edit > Properties** from the top menu.

2. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Comp (or Pin)**, if this is not already set.

3. Click **More**.

   The Find by Name/Property form appears.

4. Scroll through the list of component names and select **D1**, **D2**, **D3**, and **D4**.

   When you select each name, it disappears from the list on the left and is added to the list of Selected Objects on the right of the form, as shown:
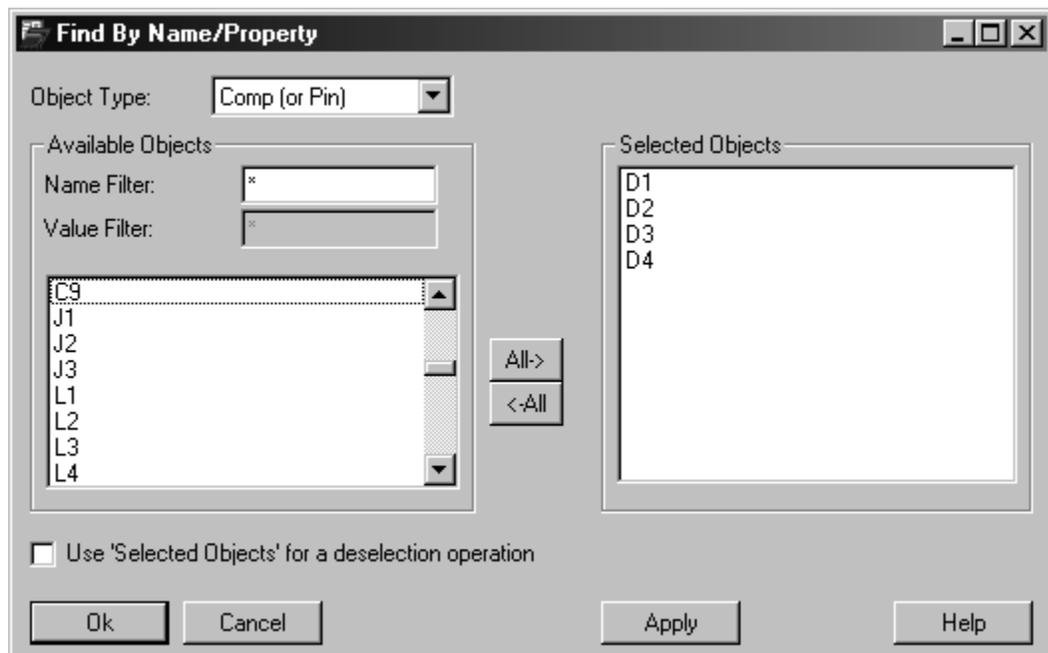
5. Click **Apply** in the Find By Name/Property form.

   Four components are now selected for editing.

6. In the Edit Property form, select the **ROOM** from the list of Available Properties in the scroll list.

7. In the blank Value field next to the ROOM property, enter the room name:

   LED

8. Click **Apply**.

   In the Show Properties window, the ROOM property is added to all four components.
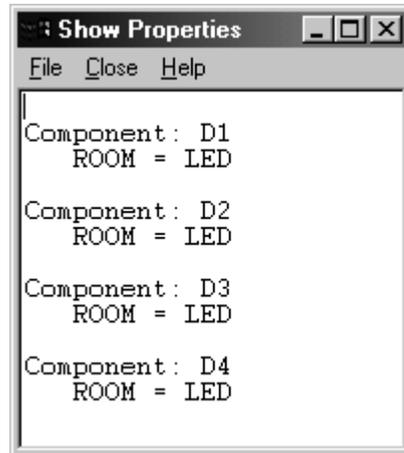
9. Click **OK** to close the Edit Property form.

10. Click **OK** to close the Find By Name/Property form.

Attaching Properties to Nets

In this section of the lab you will attach a property to several nets in the design.

1. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Net**.

2. Click in the blank field under Net, and enter:

   vcc

When you press the Enter key, the Edit Property and the Show Properties forms appear.

Note

Pre-existing properties in this net were added.

3. Scroll the list in the Edit Property form and click on **MIN_LINE_WIDTH**.

   This property now appears in the right side of the table.

4. In the blank field next to MIN_LINE_WIDTH property, enter the value of the line width:

   15
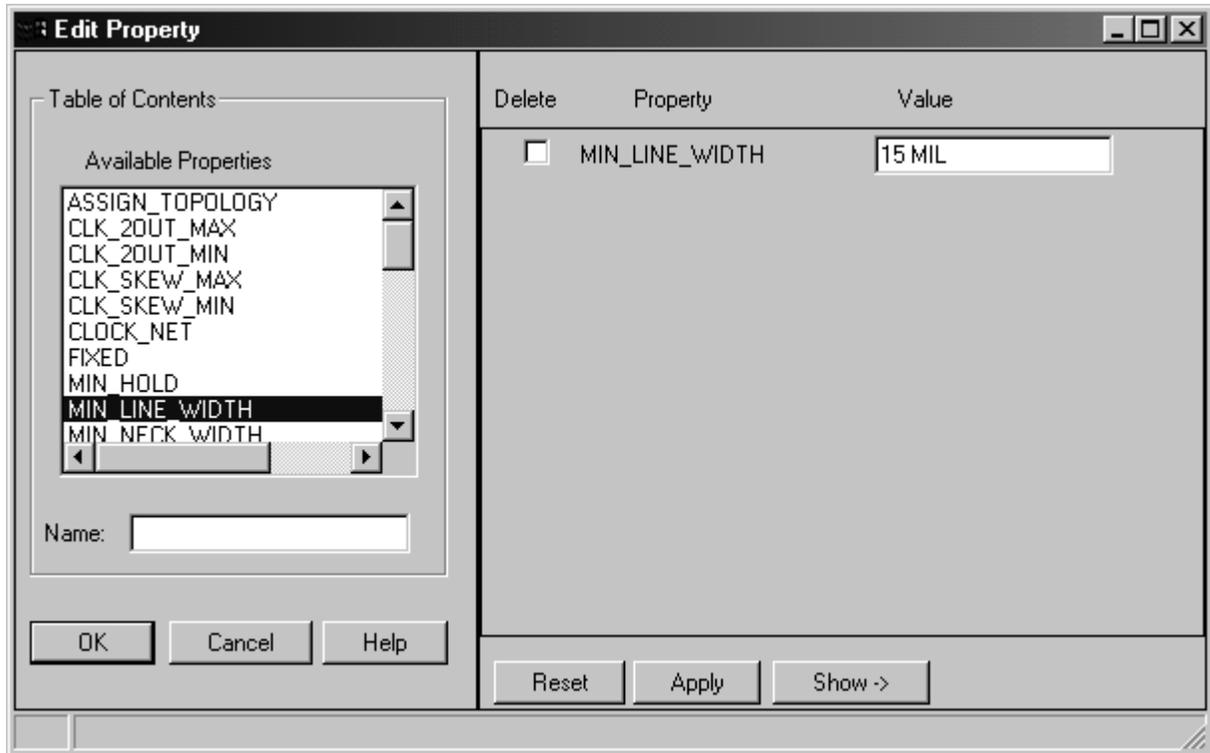
5. Click **Apply**.

In the Show Properties window, the MIN_LINE_WIDTH property is added to the net VCC.

6. Follow the same steps (2 through 5) to attach the MIN_LINE_WIDTH property to net GND, and set the value to **15 MIL**.

7. Click **OK** to close the Edit Property form.

8. Right click and choose **Done** to exit from the **Edit > Property** command.

Showing Existing Properties on Elements in the Design

There are several ways to display properties attached to elements in the design. The **Edit > Property** command lets you identify the parts or nets in which you are interested. The Show Properties window lets you identify the properties in which you are interested.

1. From the top menu, choose **Edit > Properties**.

2. Click the **Find** tab to bring the Find Filter to the front.

3. Click in the blank field under **Net**, and enter:

*

The Show Properties window displays *all* of the nets in the design, and the properties attached to each net. The GND and VCC nets where you just added properties show up at the end of the report.

4. In the Show Properties window, choose **File > Save As**.

    A browser form appears.

5. Enter the following name to save the file:

    netprops.txt

6. Click **Save** in the browser form.

    The file *netprops.txt* is written to the current working directory. This file contains the same information as the Show Properties window, and can be used to check property assignments for the design.

7. Click **Close** in the Show Properties form.

8. Click **OK** to close the Edit Property form.

9. Choose **Display > Property** from the top menu.

    The Show Property form appears. It contains a scrollable list of properties.

10. Select the **ROOM** property.

11. Click the **Show Val** button.

    The Show window displays a list of functions and components with the ROOM property attached.

12. Click **Close** in the Show window.

13. Click **OK** in the Show Property form.

Deleting Properties

1. Choose **Edit > Properties** from the top menu.

2. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Comp (or Pin)**.

3. Click in the blank field under Comp, and enter:

    j1

    The Edit Property dialog box appears and the Show Properties window displays all of the properties attached to J1.

4. In the Edit Property form, select the **HARD_LOCATION** property from the scroll list.

    The property appears to the right of the table. Notice the **Delete** check box to the left of the property name.

5. Enable the box on the left side of the property named HARD_LOCATION, as shown, then click **Apply**.
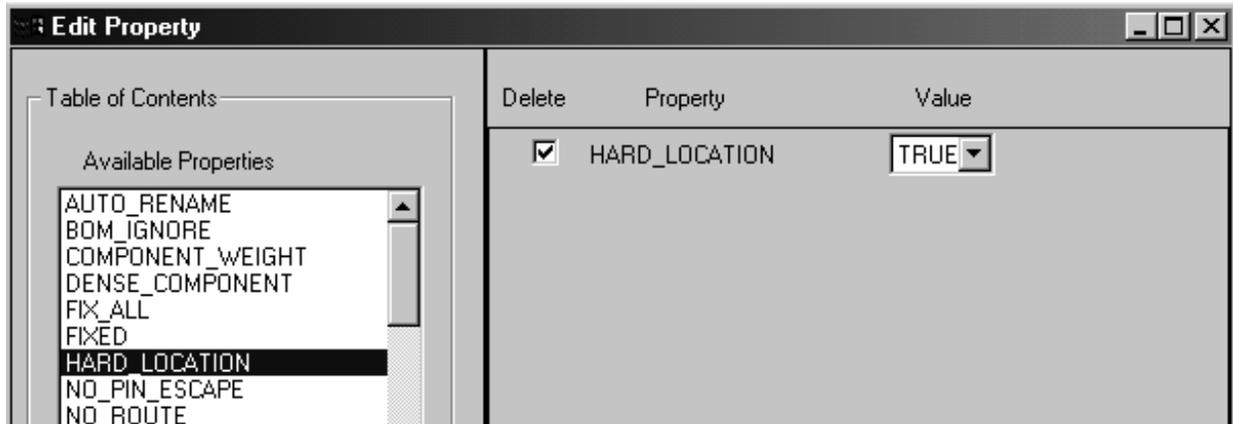
The property disappears from the Show Properties window. These steps can be used whenever you need to delete a property from an element.

6. Click **OK** to close the Edit Property form.

7. Right click and choose **Done** to exit the **Edit > Properties** command.

8. Choose **File > Save** from the top menu.

A Save window appears, prompting you to decide whether you want to overwrite the existing *constraints.brd* file.

9. Click **Yes**.

The *constraints.brd* file is saved to disk.

10. Choose **File > Exit** from the top menu of Allegro to exit the Allegro software.

STOP **End of Lab**

Lesson 8:   Component Placement

Learning Objectives

◆ Use floorplanning to organize the placement of components with the same ROOM property.

◆ Assign reference designators to preplaced parts.

◆ Learn how to use various placement commands to interactively place components on the board.

Summary

In this section you will learn how to place components on your board. You will learn how to create Rooms and assign components to rooms, how to assign reference designators to preplaced symbols, and how to quickly place components. You will also learn the interactive commands available when working with placement.

Design Layout Process
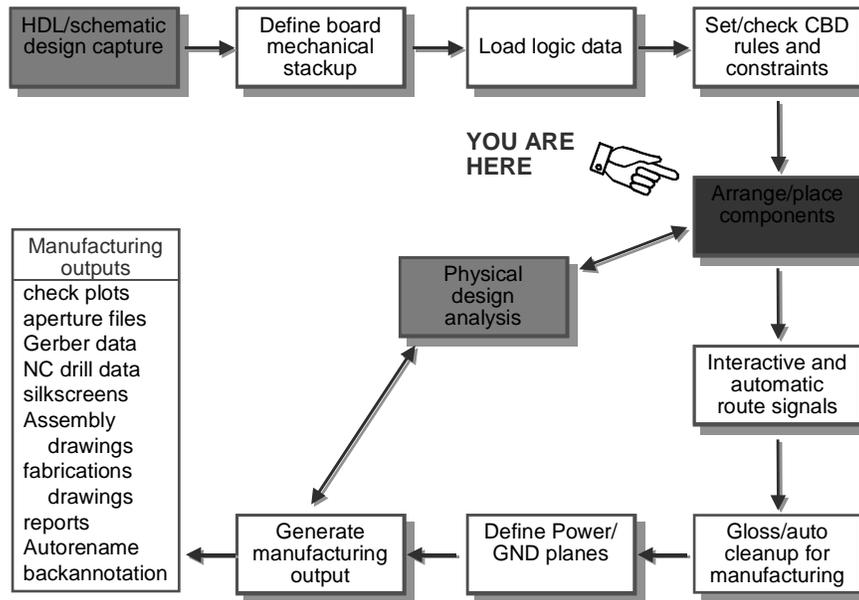
```
┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│ HDL/schematic│→ │ Define board │→ │Load logic data│→ │Set/check CBD │
│design capture│   │  mechanical  │   │              │   │  rules and   │
│              │   │   stackup    │   │              │   │ constraints  │
└──────────────┘   └──────────────┘   └──────────────┘   └──────────────┘
```

YOU ARE HERE ☞

Arrange/place components

Physical design analysis

Manufacturing outputs
check plots
aperture files
Gerber data
NC drill data
silkscreens
Assembly
   drawings
fabrications
   drawings
reports
Autorename
backannotation

Interactive and automatic route signals

Generate manufacturing output ← Define Power/ GND planes ← Gloss/auto cleanup for manufacturing

More Information

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the Arrange/place components box will now be discussed.

Prerequisites
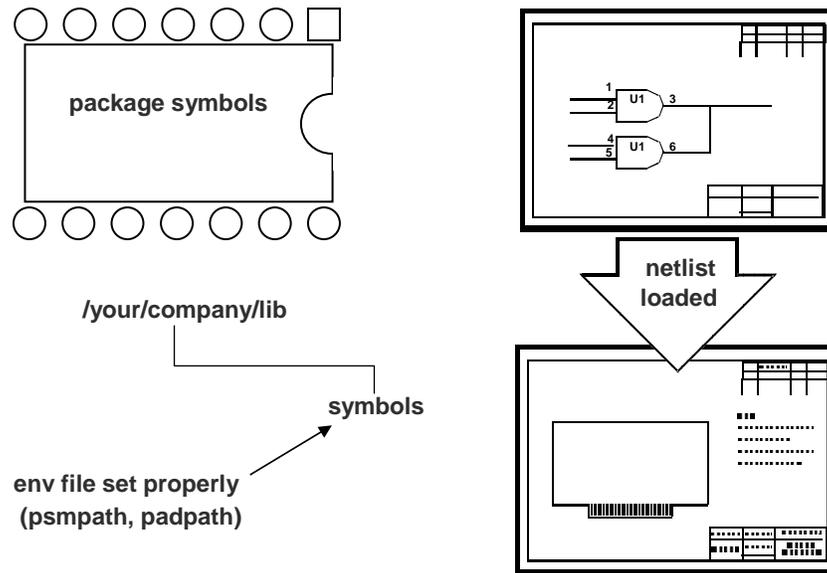
Summary

It is important to remember how Allegro determines where the footprints and padstacks are located on disk. The variables PSMPATH and PADPATH are used to determine the locations on disk of the footprints and padstacks, respectively. These variables are defined in the env file and can also be set and modified using the User Preferences Editor.

More Information

The prerequisites for manual placement are:

■ **Symbols**: The package symbols and padstacks required for parts in the netlist must exist. Point to the location of the package symbols in the library search path. You can define these paths in the env file.

■ **Netlist**: You must load a schematic database into an Allegro design file (*.brd*). See the lesson titled *Importing Logic Information into Allegro* for more details.

■ **Alternate Package Symbols**: If you plan to select alternative package symbols during manual placement, the alternate symbol definitions must be contained in the appropriate part definition files.

■ **Floorplanning**: You can create a "block diagram" of the logical functions that need to be arranged on the board by using Rooms. Specify this part property within the Concept or Capture schematics, or you can add it to a third-party netlist before the database is read in.

- ■ **Package Keepouts**: If your master design file did not contain package keepouts, add them before you begin placing components, by selecting **Setup > Areas > Package Keepout**.

Interactive Placement

Place > Manually
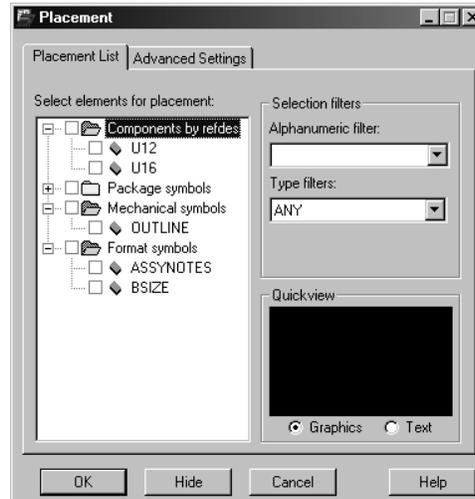
More Information

Manual placement can be used to place parts by reference designator, place all parts, place IC components, place IO components, and place discretes, as well as other options. Components are defined as IC, IO or discrete, using the CLASS property as defined in the device file for third-party netlists, or in the *chips.prt* file for Concept. For Capture, you will need to manually add the CLASS property to the parts in your library.

You also use the **Manual Placement** command to place package symbols (spare footprints), mechanical symbols (board outline or board mechanical) and format symbols (company formats).

Placement Grid

Setup > Grids
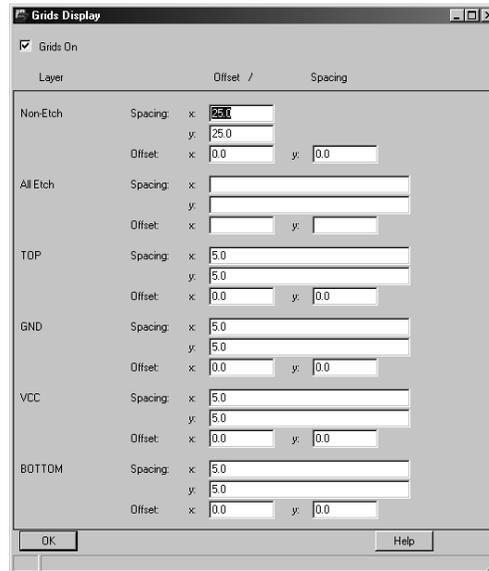
More Information

The placement grid is a Non-Etch grid (it is not the grid used for routing connections). The origin of the package symbol (defined during symbol creation) locks on to the Non-Etch grid.

Select **Setup > Grids** to set the spacing for manual placement on the Non-Etch grid. The origin of the placement grid is the origin of the Allegro design file (x 0, y 0). Use the Grid form to toggle the grid visibility ON or OFF.

You can use the **Grid Toggle** icon to turn the grid display ON or OFF.

It is not unusual to attempt to keep all through-hole components on a 100- or 50-mil placement grid (this facilitates bareboard and in-circuit testing). For dense or surface-mount designs, a 25-mil placement grid (or less) is not uncommon.

Also consider the route grid for completing pin-to-pin connections. Keeping the placement grid compatible with the route grid will reduce the number of "off-grid" pins.

Strategy

◆ Create rooms for floorplanning.

◆ Assign reference designators to "preplaced" devices.

◆ Place I/O bound devices.

◆ Place critical logic functions.

◆ Evaluate and revise placement.

◆ Place bulk decoupling and bypass caps.

◆ Use reports to aid placement process.
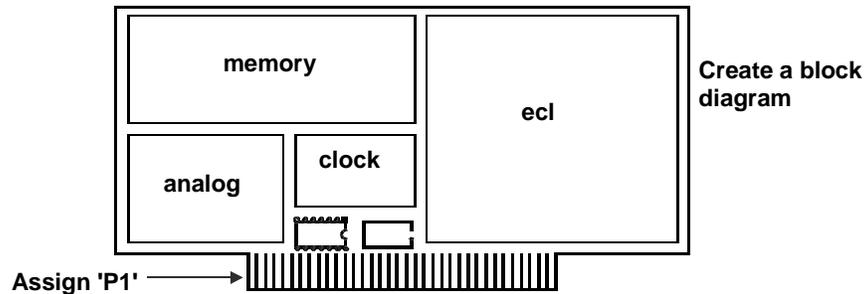
More Information

1. Floorplanning: You can create a "block diagram" of the logical functions through the use of Rooms.

2. Assign fixed IO devices: Use the **Assign** command to correlate any connector package symbols (mechanically placed within the master or template file) to reference designators in the database (such as P1, J2). This process also applies to any mechanically constrained devices preplaced in the master design file (such as LEDs).

3. Place IO bound devices: Place any parts that send or receive nets from backplane connectors to minimize overall net length.

4. Place critical logic functions: Place clock circuits, memory arrays, buffers, controllers, and address buses. (See Floorplanning on the next page.)

5. Place less critical circuits: Place data buses and random logic, interactively or automatically.

6. Evaluate and revise placement: Use ratsnest display, net highlighting, interactive or automatic gate and pin swapping, density evaluations, interactive net scheduling, DFA, and Signal Analysis tools.

7. Place bulk decoupling caps: Perform this step last. If embedded split planes are required for multiple voltages, group filter caps and associated ICs accordingly.

Note

Some database reports may be useful during the placement process (for example, nets list, components list, bill of materials, and placed or unplaced components list). Also, you can use ECL length reports to flag potential net length problems prior to routing.

Floorplanning with Rooms
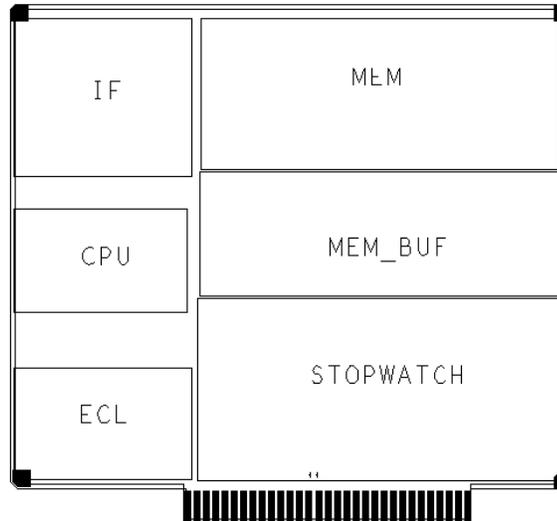
More Information

Rooms are confinement areas that provide a useful method of grouping components. You can force automatic placement to occur with specific components and cause them to be placed within specific rooms. You can attach a room property to components during schematic creation, netlist creation, or at any time while in the Allegro design. Room boundaries are recognized as being closed polygons on the TOP_ROOM, BOTTOM_ROOM, or BOTH_ROOMS subclasses of the BOARD GEOMETRY class.

Creating a Room

Rectangular   **Polygon**

Add

Line
Arc w/Radius
3pt Arc
Circle
Rectangle
Frectangle
Text
Shapes ▶

Solid Fill
UnFilled
Cross Hatch Fill

Options   Find   Visibility

Active Class and Subclass:

BOARD GEOMETRY

☐ TOP_ROOM

Line font: Solid
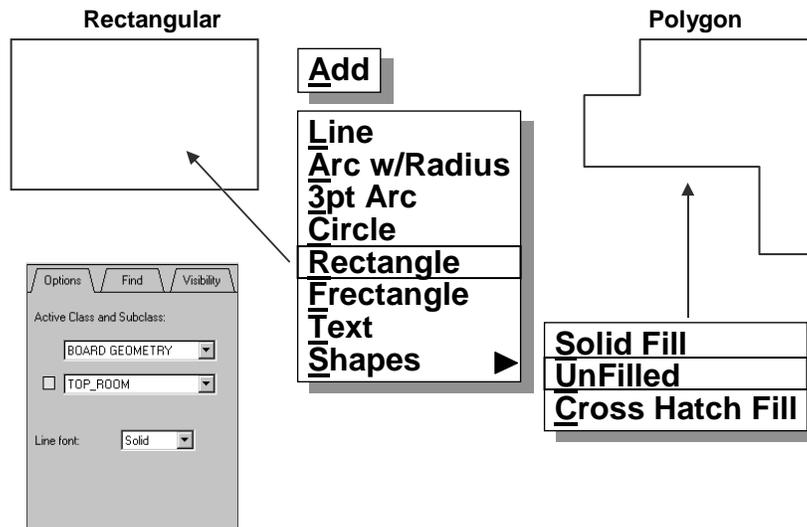
More Information

Rectangular Rooms

Select **Add > Rectangle**.

Make sure that the Options form reflects the following settings:

■   Class = BOARD GEOMETRY

■   Subclass = TOP_ROOM, BOTTOM_ROOM, or BOTH_ROOMS

Polygon-Shaped Rooms

To create a non-rectangular room boundary, select **Add > Shapes > Unfilled**. Use the same settings in the Options form as documented for Rectangular rooms.

Attaching Room Name Text

```
Add    (1)
┌──────────────┐
│ Line         │                              (2) Attach text to
│ Arc w/Radius │
│ 3pt Arc      │
│ Circle       │
│ Rectangle    │                          (4)
│ Frectangle   │      ┌ ─ ─ ─ ─ ─ ┐    ┌──────────┐
│ Text         │      │ MEM_BUF   │    │ Done     │
│ Shapes       │      │           │    │ Oops     │
└──────────────┘      └ ─ ─ ─ ─ ─ ┘    │ Cancel   │
                                        └──────────┘
                              (3) Pick location
```
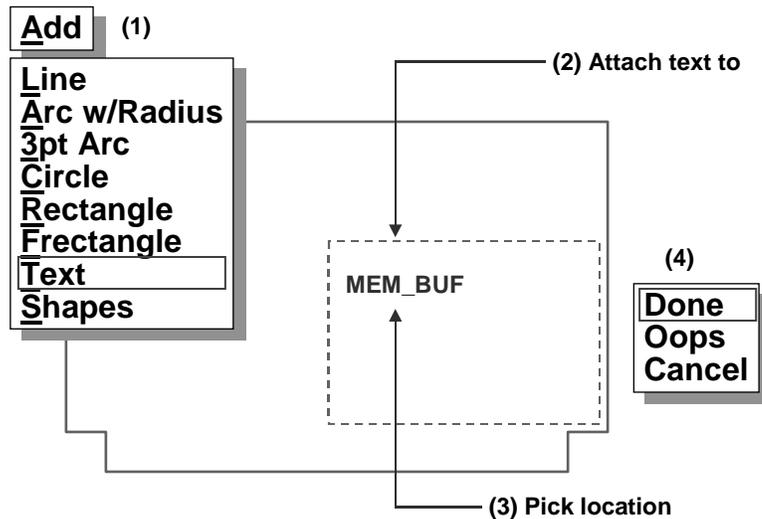
More Information

To add the room name to the polygon, use the **Add > Text** option from the top menu. Select the polygon you have drawn, select a point where the text should appear, and enter on the Allegro command line the name of the room. The room name you add must match the property you attached to your components. The room name is NOT case-sensitive. In order to have DRC's appear when the part is NOT placed inside the room, attach the property ROOM_TYPE with a value of HARD to the room.

Assign RefDes Command

Tools > Assign RefDes
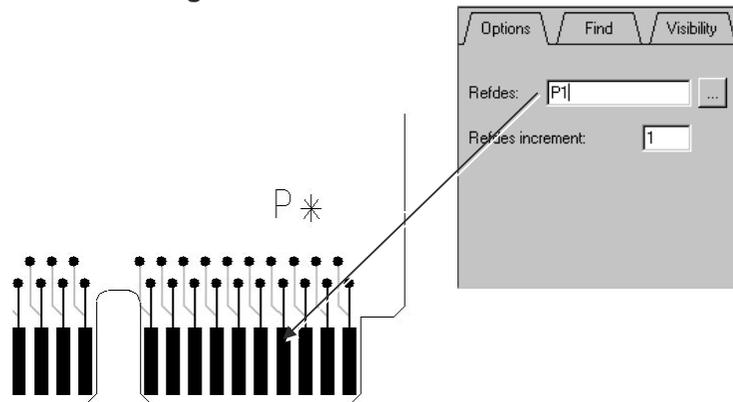
More Information

Use the **Tools > Assign RefDes** command to correlate any package symbols (mechanically constrained and preplaced within the master or template file) to reference designators in the database (for example, P1 and J2).

Enter the reference designator you want to assign into the Options form or select the "browser" button to bring up a list of all the Reference Designators that still require placement. Then select a part from the list, and select the corresponding package symbol. If you entered a reference designator that cannot be found within the database, an error message is output to the Allegro message area.

The specified reference designator is automatically incremented by 1 (default). For example, after you assign refdes 'J1', the next package symbol you select is assigned the refdes 'J2' designation (unless otherwise specified in the Options form).

Labs

◆ Lab: Floorplanning

■ Organize areas of the board to place component parts with the same ROOM property together on the board.

● Start in the work directory.

● Set the non-etch grid.

● Add rooms.

● Add room text.

◆ Lab: Assigning Preplaced Packages

■ Associate a preplaced component with a logical part from the netlisted database

More Information

The following labs will allow you to:

■ Familiarize yourself with the process required to create rooms within your design.

■ Familiarize yourself with the process required to assign reference designators to preplaced packages.

Lab 8-1:   Floorplanning

Objective: Create a floorplan for part placement.

Each design has unique placement requirements. For this reason, floorplanning is performed after the logic has been loaded into the master design file.

Starting in the Work Directory

Later in this module, you will perform pin and gate swapping. Pin and gate swapping is an operation that can change your design making it no longer synchronous with the original schematic. In this case, you will need to run backannotation. We cover backannotation later.

1. Start Allegro.

2. Choose **File > Open** and open the *constraints.brd* design (if it is not the current design).

3. Use the **View** command or strokes (**W**, **Z**) to fit the board to your work area.

Setting the Non-Etch Grid

During placement, components you move will lock to this grid.

1. Toggle the grid points to ON, if they are not currently displayed, by clicking the **Grid** icon in the top menu.
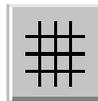
2. Choose **Setup > Grids** from the top menu.

   The Grids Display menu opens.

3. Locate the Non-Etch section at the top of the form and set the X and Y Spacing to **25** mils, as shown in the figure:
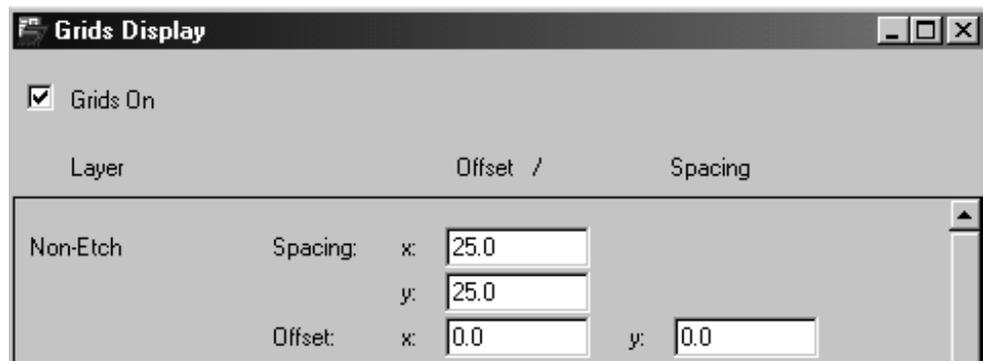
4. Click **OK** at the bottom of the form.

    You might see the following message:

    > "Grids are drawn at 100.0, 100.0 apart for enhanced
    > viewability."

    In this case you need to zoom in to actually see the 25-mil grid points.

Adding Rooms

In the following exercise, you first turn on the layers that display the room information. Once you have added four rectangular rooms, you will give them each a name. Each set of coordinate points you lay down becomes the diagonal corner of a rectangle.

1. Click the **Color** icon.

    The Color and Visibility form appears.

2. Select the **GEOMETRY** group.

    The Geometry group contains two classes, BOARD GEOMETRY and PACKAGE GEOMETRY.

3. Use the scroll bar on the right side of the form to find the **TOP_ROOM** subclass under the BOARD GEOMETRY column.

4. Toggle the TOP_ROOM layer ON. If you prefer a different color for this subclass, you can also set the color at this time.

5. Click **OK** to close the Color and Visibility form.

6. Click the **Options** tab to bring the Options form forward.

7. Choose **Add > Rectangle** from the top menu.

    The Options form displays two fields for Active Class and Subclass. The top box is the Class, and the lower box is the Subclass. Set the Class and Subclass fields as shown:
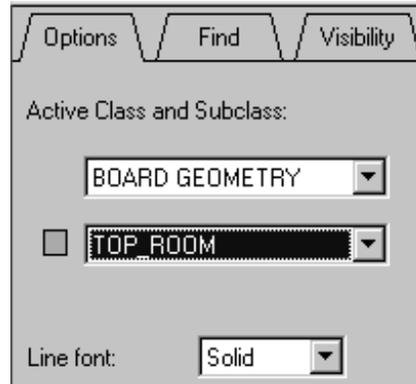
8. At the Allegro command line, enter:

   x 1900 4200

   x 3800 2200

   x 1400 2200

   x 3900 1500

   x 1300 1500

   x 3900 700

   x 1300 700

   x 3900 -100

   Four rectangles appear on the board.

9. Right-click and choose **Done** from the pop-up menu.

Adding Room Text

1. Choose **Add > Text** from the top menu.

   The Allegro message area prompts:

   ```
   Pick an element to attach text to.
   ```

2. Click someplace on the top most rectangle that you just created.

   The rectangle appears highlighted. The Allegro message area prompts:

   ```
   Pick text location.
   ```

3. Set the values in the Options form to match those in the figure:
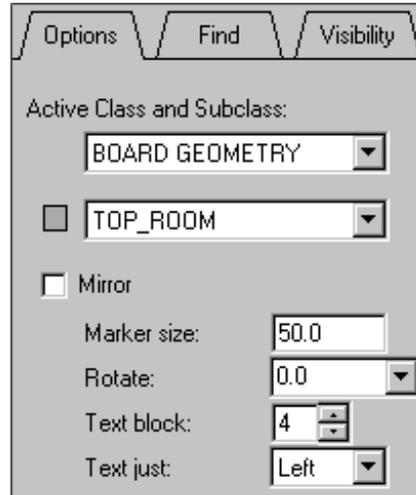
4. Click somewhere inside the highlighted rectangle, and enter:

MEM

You have attached the name for this room. Next you will attach the name for your other room.

5. Click the next lower rectangle and name it **LED**.

6. Name the next two rectangles **CHAN1** and **CHAN2**, as shown in the figure:
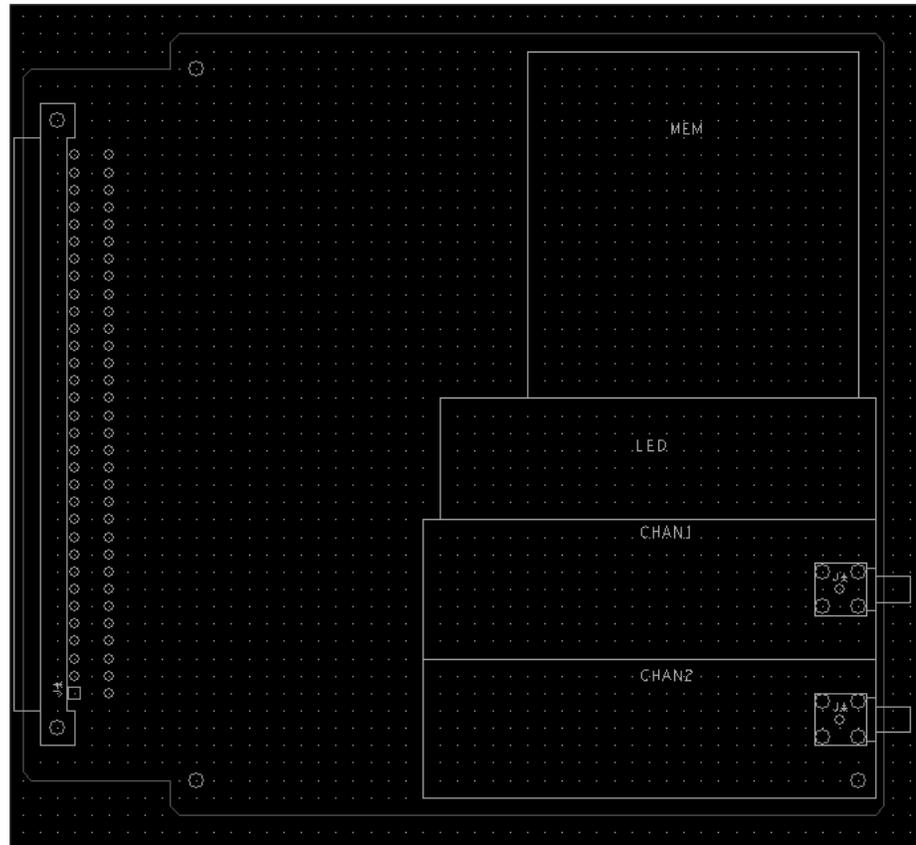
7. Right-click and choose **Done** from the pop-up menu.

   You have just created four rooms, the MEM, LED, CHAN1 and
   CHAN2 rooms. Parts that have an attached Room property equal to
   these name values be placed according to the room they belong in.

8. Choose **File > Save** from the top menu.

   A window appears and warns you that the *constraints.brd* file already
   exists. It asks if you want to overwrite the file.

9. Click **Yes** to confirm the overwrite.

   The file *constraints.brd* is written to disk.

STOP **End of Lab**

Lab 8-2: Assigning Preplaced Packages

Objective: Associate preplaced connectors to the logical database.

The mechanical template used to create this design file (*master.brd*) contained preplaced package symbols. In order for a preplaced part to have connectivity, it must be assigned a reference designator that exists in the design database.

1. From the top menu, choose **Tools > Assign RefDes**.

2. In the Options form, click in the **Refdes** field and enter:

   j1

3. Click on any graphics associated with the edge connector symbol. You may want to zoom in on J1.

   J* has changed to J1.

4. Click on the upper BNC connector at the right side of the board.

   J* has changed to J2.

5. Click on the lower BNC connector at the right side of the board.

   J* has changed to J3. Both BNC connectors now have reference designators assigned, as shown in the figure:
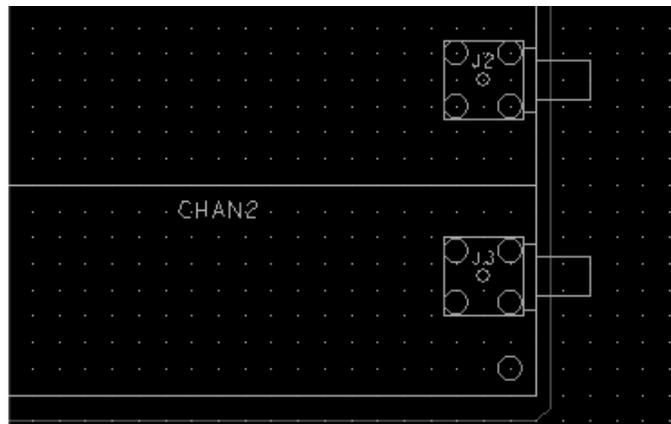
6. Right click and choose **Done** from the pop-up menu.

7. Choose **File > Save** from the top menu.

   A window appears and warns you that the *constraints.brd* file already exists, asking you whether you want to overwrite the file.

8. Click **Yes** to confirm the overwrite.

   The file *constraints.brd* is written to disk.

⬣STOP End of Lab

Placement-Related Properties

- ◆ PLACE_TAG
- ◆ ROOM
- ◆ NO_SWAP_GATE
- ◆ NO_SWAP_GATE_EXT
- ◆ NO_SWAP_PIN
- ◆ FIX_ALL
- ◆ FIXED

More Information

- ◆ **PLACE_TAG** — Indicates the component is to be placed during the next automatic or interactive placement session.

- ◆ **ROOM** — Indicates the component is to be located in a particular location, identified by the room name, during automatic placement.

- ◆ **NO_SWAP_GATE** — Indicates functions within components cannot be swapped.

- ◆ **NO_SWAP_GATE_EXT** — This function cannot be swapped with a function from another component (only swapped among slots within its current component).

- ◆ **NO_SWAP_PIN** — Indicates that pins on this component or function cannot be swapped, either interactively or automatically.

- ◆ **FIX_ALL** — Declares that components having this property will not be eligible for any pin or gate swapping.

- ◆ **FIXED** — Component cannot be moved or deleted.

Tagging Parts for Placement

filename = cpu.lst

u15
u65

name or list toggle
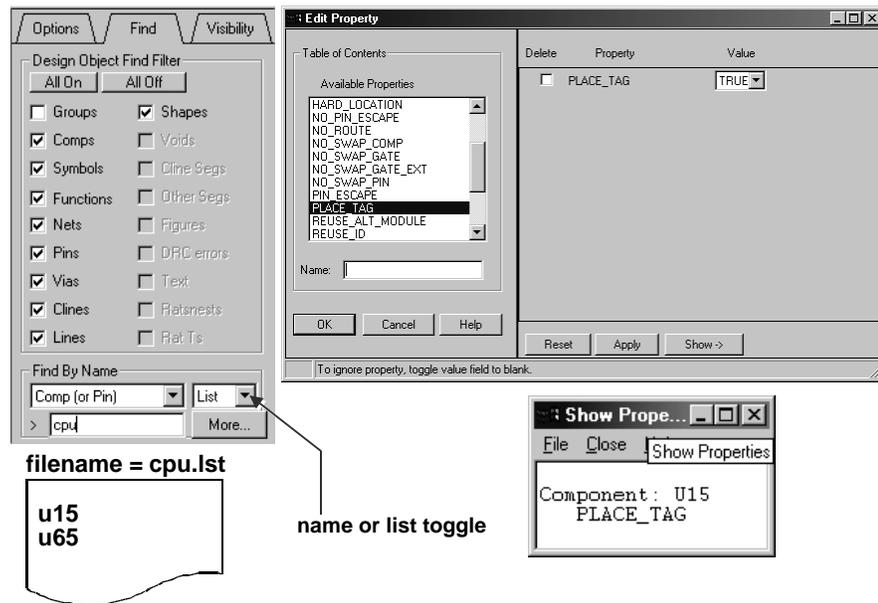
More Information

The PLACE_TAG property lets you create a special group of critical parts for placement. Once you have attached the PLACE_TAG property to the preferred parts, you can request parts from this group using the **Place > Manually** command and setting the Type Filters to Place_tag.

To use the PLACE_TAG property in manual placement, you attach the property using the same methods available for attaching any properties. In the example shown, the name of an ASCII file containing the preferred parts is specified (create multiple files, each representing a different group or function). Note that if you don't specify an extension, the *.lst* extension is assumed.

Placement Commands

Place > …

Manual placement → Manually…
Quickplace

SPECCTRA
Automatic placement → Autoplace

Swap
Autoswap…

Placement utilities → Update Symbols…
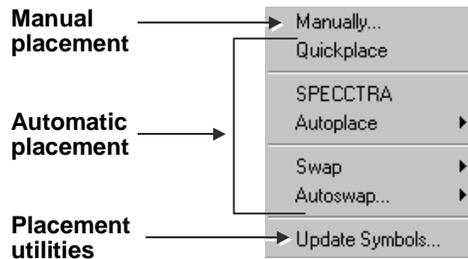
More Information

Allegro placement commands include the following types:

■ Manual placement commands are used to select components individually or by groups, and interactively determine their location. The Quickplace command will place parts outside the board outline, whereby the parts can then be placed interactively to determine their final location.

■ Automatic placement commands include both Allegro and SPECCTRA automatic tools.

■ A placement analysis tool is used to determine areas of high density and high signal crossing counts.

■ Component symbol utilities include methods of accessing new library data to update your design.

Manual Placement Commands
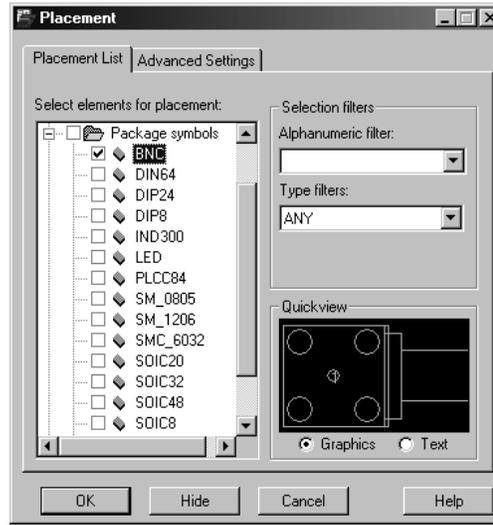
Right mouse button pop-up menu
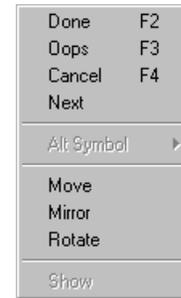
More Information

The **Manual Placement** command lets you specify a component or a group of components. Allegro attaches a component from that group to your cursor. Click to place the attached part to a point on the placement grid. The following options are available when you select **Place > Manually** from the top menu.

- **Components by RefDes** lets you specify one or more reference designators.

- **Package Symbols** lets you place package symbols in the design WITHOUT containing any logical information.

- **Mechanical Symbols** lets you place mechanical symbols in the design.

- **Format Symbols** lets you place format symbols in the design.

The Selection Filters section lets you further refine the elements that are available for selection. The following two sections are available:

- **Alphanumeric Filter** lets you select the elements that match the name you enter. You may use the wildcard character of "*" to select a group of components, such as "U*.

- **Type Filters** lets you select the elements that match a certain CLASS as defined in the device file, part(s) that have the Place Tag property, or parts of a certain device type.

While a part is attached to the cursor, click right to access options for rotating the part, or mirroring the part to the opposite side.

By default, the Manual Placement form will be displayed at all times. This may take up too much space in your work area. To hide this form, you can either select the **Hide** button, or enable the **AutoHide** option available in the Advanced Settings folder tab. In either case, make sure you select the components to place first before hiding the form.

Changing the Default Orientation

Setup > Drawing Options

Orientation for
back of board
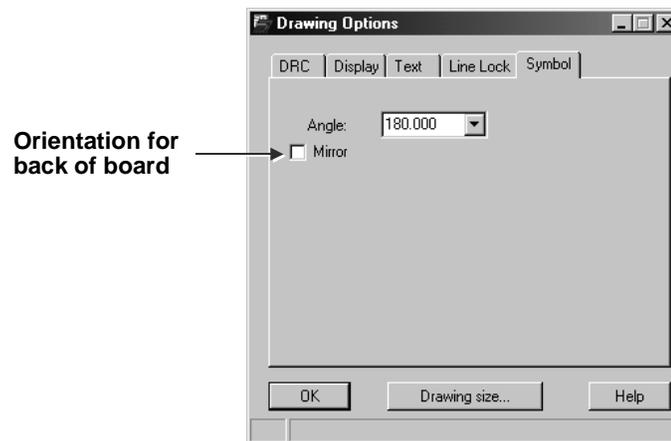
More Information

When you place parts manually, they are by default placed on the top side of the board (this is the default when you create your package symbols). However, certain times you may want to place a series of parts on the bottom or back side of the design (such as standard surface-mount decoupling capacitors). To have Allegro place each part on the bottom side of the board, WITHOUT manually using the right mouse button pop-up "mirror" option, set the Mirror toggle in the Symbol Folder tab under **Setup > Drawing Options**. After setting this toggle, all parts that are manually placed will by default be placed on the bottom side of the board.

Lab

◆ Lab: Manual Placement

■ Learn to use interactive commands to place components on the board.

● Place parts by reference designator.
● Change default orientation.
● Use the Move and Rotate commands.
● Move groups of parts.
● Place groups of components in a room.
● Place a component by type.

More Information

The following lab will allow you to familiarize yourself with the process required to manually place parts on the board. You will learn how to rotate parts, mirror parts, move parts and other manual placement options.

Lab 8-3:   Manual Placement

Objective: Select, place, and move components interactively.

Placing Parts by Reference Designator

1. From the top menu, choose **Place > Manually**.

    The Placement browser window appears.

2. Click the **Placement List** tab to bring it forward if it is not visible.

3. Click on the + icon to expand the Components by refdes folder.

4. Scroll through the list and enable the check box to the left of **U5**.

    An outline view of the footprint is displayed in the Quickview window, and the Allegro message area states:

    ```
    Placing U5 / EPF8282A_LCC / PLCC84.
    ```

5. Move the cursor into the main Allegro window.

    U5 is attached to your cursor. Before placing U5, you need to rotate it.

    ### Note

    When a part is attached to your cursor for manual placement, it is not rotated (0-degree rotation by default). This is the orientation of the part when it was created.

6. Right click and choose **Rotate** from the pop-up menu.

    A "handlebar" extends between the part and your cursor.

7. Use the handlebar to spin the component.

    Notice that the angle of rotation appears in the status area at the lower right of your window.

8. Spin **U5** to 180 degrees.

    Notice the angle reading in the Status area of your screen (lower right corner).

9. When the Status area shows that U5 is in a 180-degree rotation, click left to accept the current orientation.

    You are no longer in rotate mode, but you are still in move mode. U5 is still attached to your cursor.

10. Click to place **U5** in the design at the location shown in the figure. You will probably have to move the Placement browser window to see the board location.
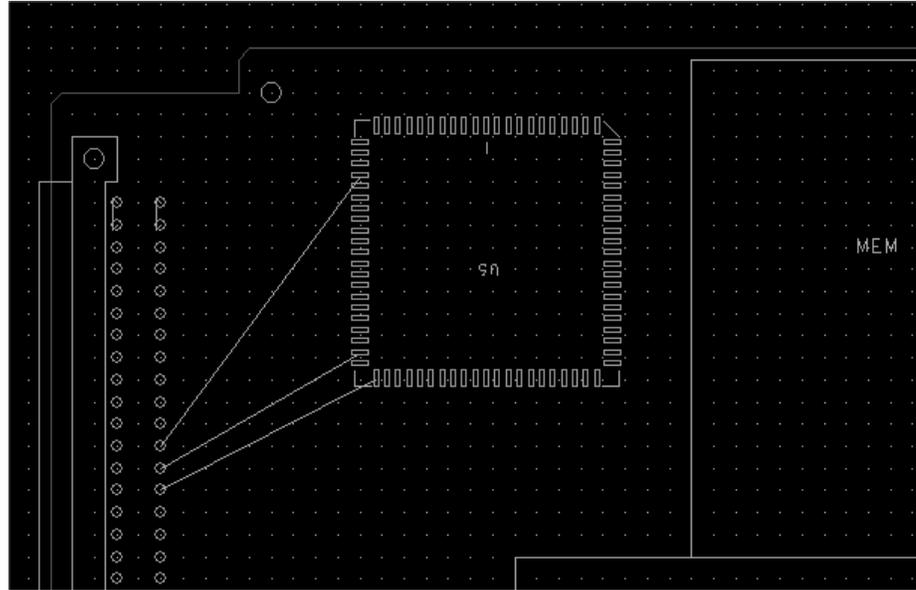
11. Right click and choose **Done** from the pop-up menu.

# Changing the Default Orientation

Rather than using the **Rotate** command from the pop-up menu, you can override the default orientation using the Drawing Options form.

1. Choose **Setup > Drawing Options** in the top menu.

The Drawing Options form appears. In the upper right is a tab labeled Symbol.

2. Click the **Symbol** tab to bring it forward.

3. Set the Angle field to **180**, as shown:
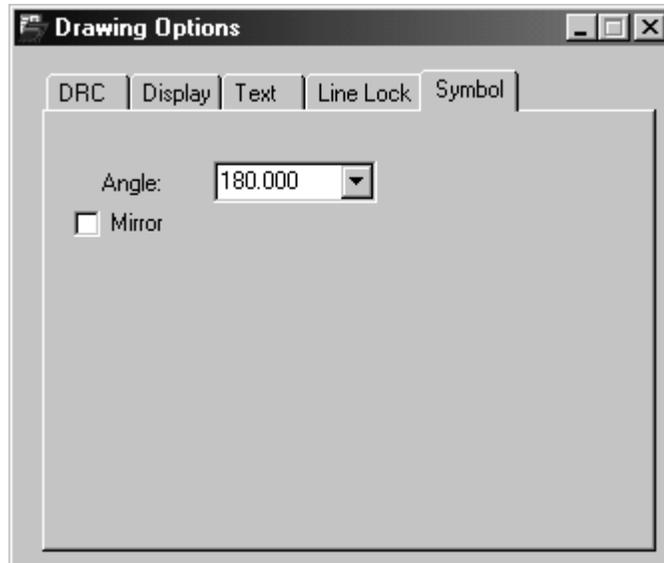
4. Click **OK** to exit from the Drawing Options form.

   Now the default orientation is 180 degrees (instead of zero).

5. Choose **Place > Manually** from the top menu.

   The Placement form appears.

6. Select the **Placement List** tab to bring it forward if it is not visible.

7. Expand the **Components by refdes** folder.

8. Scroll through the list and enable the check box to the left of **U1**.

   U1 appears in the Quickview window.

9. Move your cursor into the Allegro window.

   U1 attaches to your cursor in a 180-degree rotation. The dynamic ratsnest lines between the two components appear.

10. Click to place the **U1** component on the board at the location indicated in the next figure.

Place **U4** here.

Place **U3** here.

Place **U2** here.

Place **U1** here.
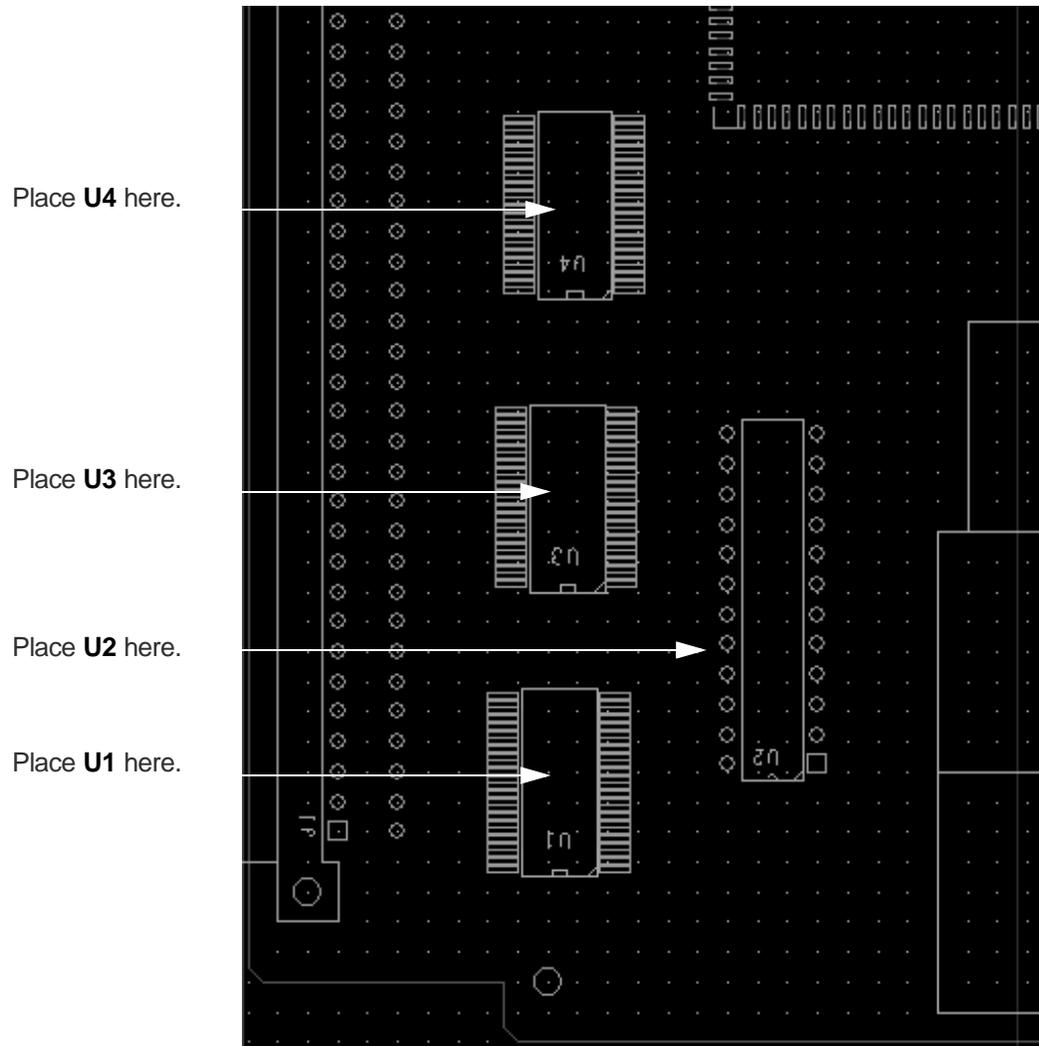
11. Place components **U3**, **U4**, and **U2** using the method you just tried. Refer to the above figure for where to place the components.

12. Right click and choose **Done** from the pop-up menu to complete the command.

Moving Parts

When you are using the **Place Manually** command and no part is selected in the Placement form, you are by default in the Move mode. You can also at any time initiate the Move mode by using the right mouse button and choosing Move.

1. Choose **Edit > Move** from the main menu.

2. Click to select a part to move, and click to place it in a new location.

3. Practice this command with other parts.

4. Right click and choose **Done** from the pop-up menu.

Moving Groups of Parts

1. Choose **Edit > Move**.

2. Click the **Find** tab to bring the Find Filter to the front.

3. In the Find Filter, toggle everything OFF except **Symbols**.

4. Click and hold the left mouse button as you drag the mouse to stretch a frame around the desired group of components you want to move.

    ### 📝 Note

    The parts do not need to be entirely within the window to be selected. Do not include any part of the board outline in your selection window. The board outline, keepins, and keepouts were created as one board symbol, so this symbol should NOT be moved.

    If you make a mistake creating the selection window, right-click and choose **Oops** from the pop-up menu. Then use the left mouse button to stretch a frame around the desired components.

5. When the parts you want to move are highlighted, click left (but do not hold) to define an origin, or reference point, for the group to move.

    The group is attached to the cursor.

6. Move the group around and click on a new grid location to place the group.

7. Right-click and choose **Done** from the pop-up menu.

Assigning the PLACE_TAG Property

You can specify a group of parts you want to place by attaching a PLACE_TAG property to them.

1. Choose **Edit > Properties** from the top menu.

2. In the Find filter, select **All Off**, then enable **Comps**. Make sure the Find by Name field is set as shown in the figure:

3. Click the **More...** button.

    A Find By Name/Property window appears.

4. Select **ROOM = MEM**, then click **Apply**.

   The Edit Property dialog box and a Show Properties report appear.

5. Scroll down the Show Properties report and identify which ICs (those with a U reference designator prefix) have the ROOM = MEM property. You should see eight components: U10, U11, U12, U13, U14, U15, U16, and U17.

6. Close the Show Properties form, the Edit Property dialog box, and the Find By Name/Property window.

7. In the Find Filter, make sure the **Comps** check box is enabled and the first field under the Find by Name section is set to **Comp (or Pin)**, as shown in the figure:

8. Click the **More...** button.

   A Find By Name/Property window appears.

9. Scroll through the list and select all of the U components you identified in step 5: U10, U11, U12, U13, U14, U15, U16, and U17.

   As you click each name, it moves to the list on the right. You are forming a group of selected parts.

10. Click **OK**. in the Edit Property form.

    The Edit Property form appears.

11. In the Edit Property form, select the **PLACE_TAG** property, and click **Apply**.

    The PLACE_TAG property is now attached to all the parts in the group you defined.

12. Click **OK** to close the Edit Property form.

13. Right-click and choose **Done** from the pop-up menu.

Placing Groups of Components in a Room

1. Choose **Place > Manually** from the top menu.

2. In the Type Filters field of the Selection filters area, select the **Place tag** option, as shown in the figure.
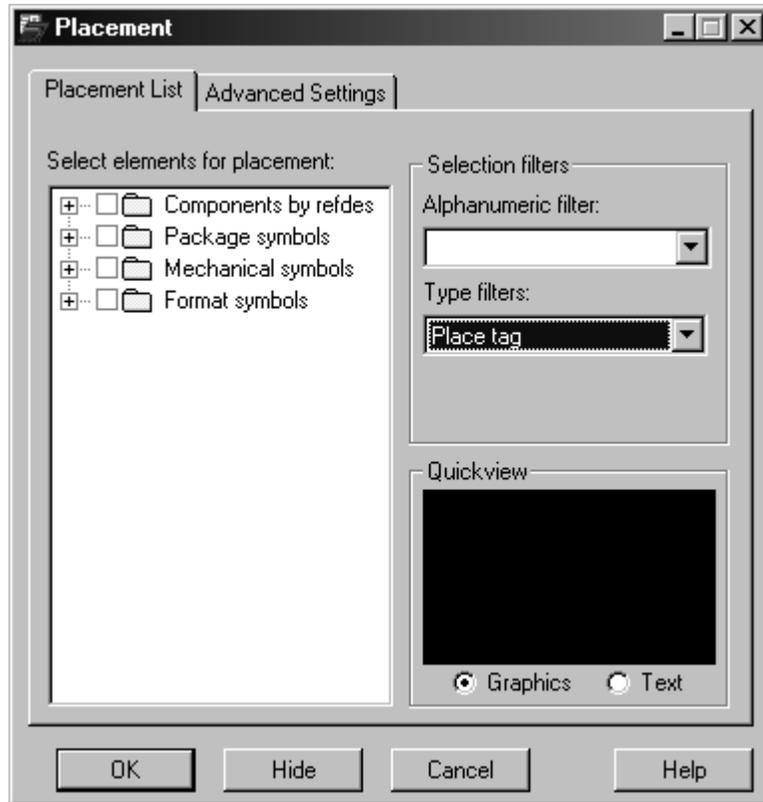
Part U10 is attached to your cursor.

3. Place parts **U10** through **U17** in the MEM room, using the **Rotate** and **Move** commands to arrange all the parts in 4 x 2 row-column matrix, as shown in the next figure:
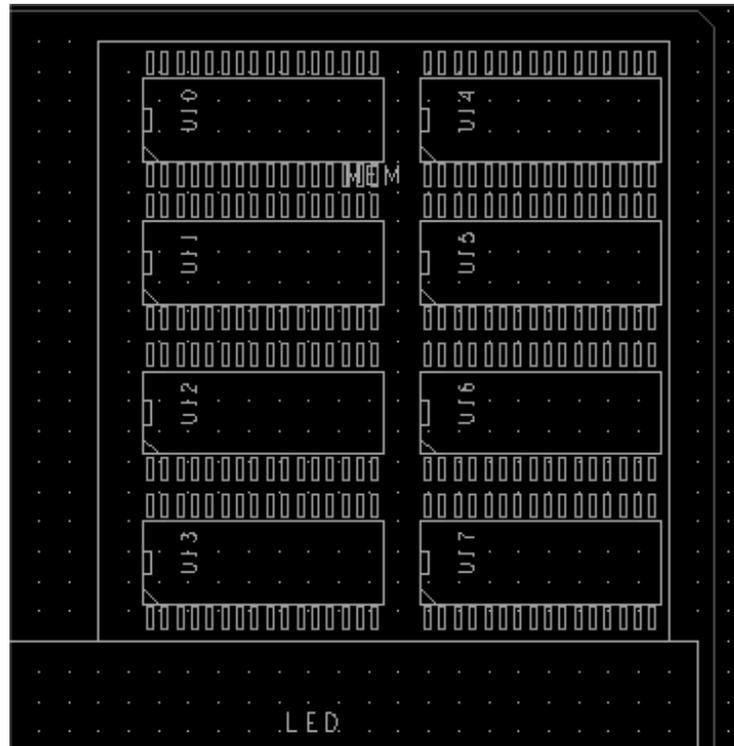
4. Click **OK** in the Placement form to end the manual placement command.

Placing a Component by Type

1. Choose **Place** > **Manually** from the top menu.

   The Placement form appears.

2. Select the **Placement List** tab to bring it forward if it is not visible.

3. Under Selection Filters/Type Filters, select **IC**.

4. Do not click or select anything, but move your cursor into the Allegro window.

   An IC component appears, attached to your cursor as you move it.

5. Move your cursor into the Allegro window and place the IC attached to your cursor. Continue to place the IC components. The figure below shows a suggested placement for these.

Note

You can use the **Move**, **group Move**, and **Rotate** commands to rearrange the locations and orientation of the ICs as needed.
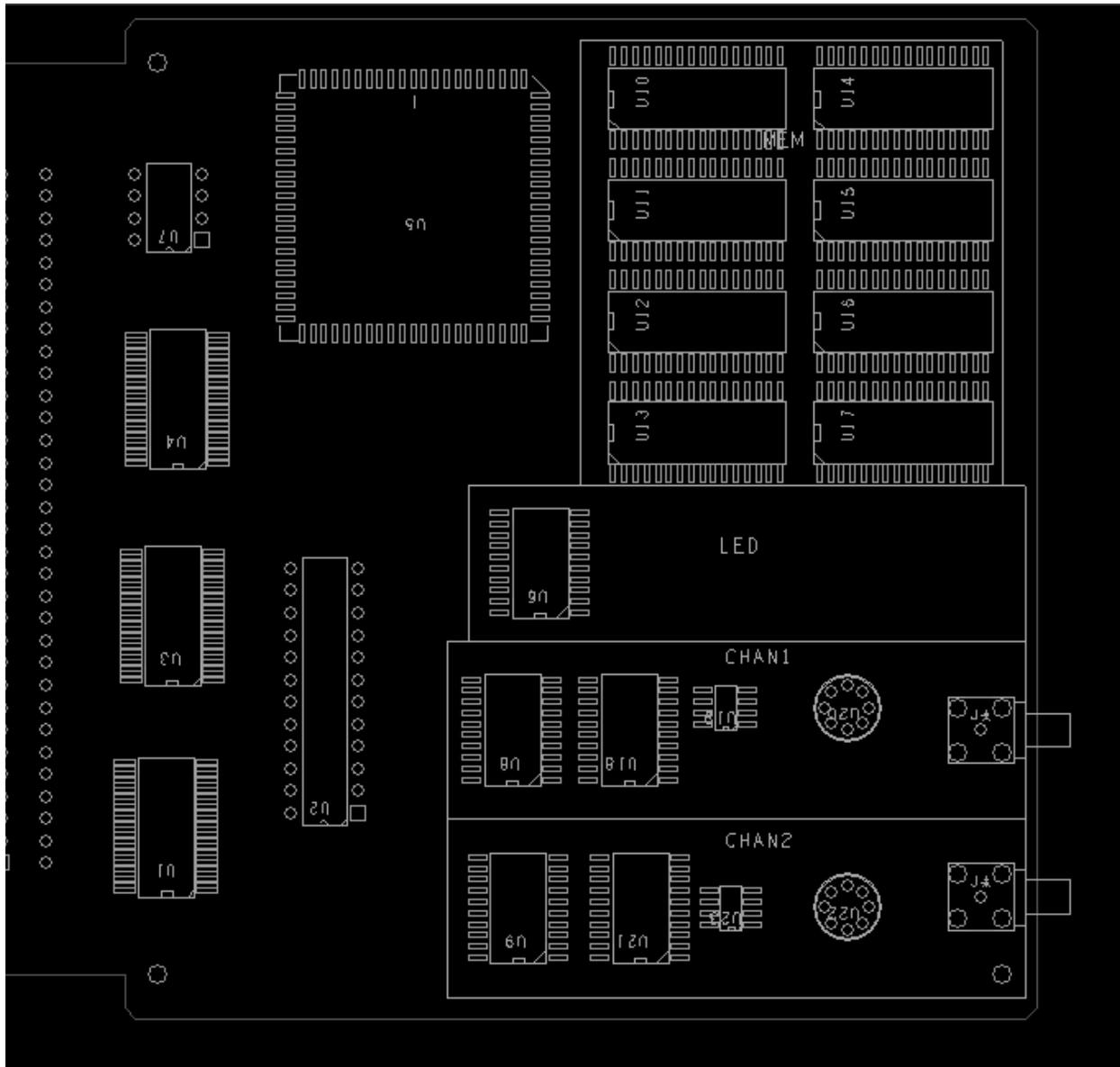
6. When you are finished placing all the IC components, choose **Done** to end the placement command.

STOP **End of Lab**

Quickplace
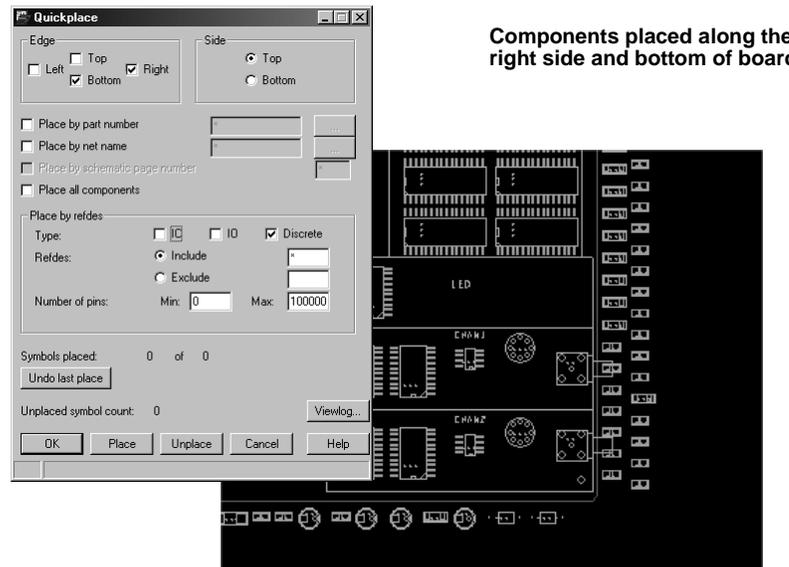
**Components placed along the
right side and bottom of board**

More Information

The **Quickplace** command will place unplaced parts outside the board outline, but will not place any parts outside the drawing extents. Parts that are already placed in the design will not be affected by the **Quickplace** command.

By using the **Edge** section and **Side** section of the form, you can control whether parts are placed outside the left, right, top or bottom of the board outline and whether the parts are placed on the top or bottom side of the design. The options can be changed at any time and the command rerun multiple times to achieve almost any desired placement pattern.

The **Place all components** option will attempt to place all currently unplaced parts in the next execution of the command. If this option is not set, the Filters section of the form is enabled.

You use the **Place by refdes** section to refine the parts for placement. You can specify only IC, IO or Discrete components or any combination of the three. Remember, these three classifications of parts are controlled by the library definition in Concept or Capture and by the device files for third-party netlists.

The **Undo last place** button will remove only the most recent parts placed as specified by the Filters setting. The Unplace button will repeatedly remove parts placed for as many times as a place option was run during the current session.

The **Symbols placed** field displays the number of components placed, as well as the number of available components for placement, as determined by the Filters settings.

The **Unplaced symbol count** field displays the current number of parts remaining to be placed.

Lab

◆ Lab: Using Quickplace

- Use the **Quickplace** command to place parts outside the board outline so they can be viewed before placement

More Information

The following lab will allow you to familiarize yourself with the process required to use Quickplace. You will also use the placement skills you have already learned to place the design.

Lab 8-4:   Using Quickplace

Objective: Use the Quickplace command to place parts outside the board outline so they can be viewed before placement.

The Quickplace command can be used to place parts outside the board outline. You can then start moving parts onto the design to create your final placement. You will place all Discrete components to the right of the board outline so you can see them all at once.

1. Choose **View > Zoom World** to display the entire extents of the drawing.

2. If the grids are displayed, turn them off by clicking the **Grid Toggle** icon.

3. Choose **Place > Quickplace** from the top menu.

   The Quickplace form is displayed.

4. Set your options as shown in the figure below. You will have to change several of the default settings.

   Notice you set Bottom for the Side the components will be placed on. Most of the capacitors and resistors belong on the back side of the board. You will have to use the **Edit > Mirror** command to flip the inductors over to the top of the board.
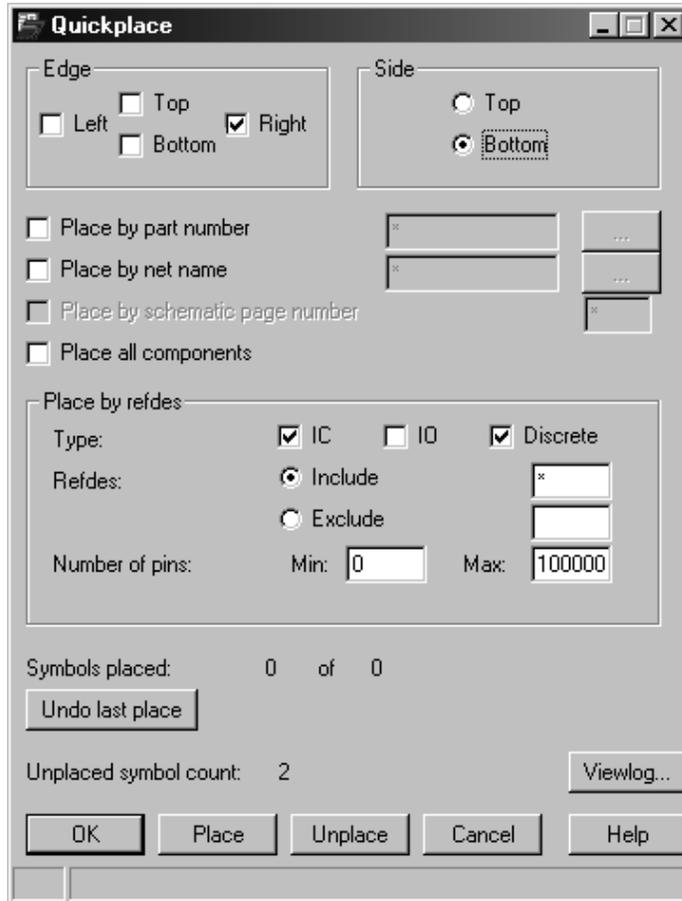
5. Click **Place** at the bottom of the form.

   All of the parts defined as Discrete are placed to the right of the board outline.

6. Click **OK** at the bottom of the form to close the Quickplace form.

7. Choose **Edit > Spin** in the top menu.

8. Select all the components, except for the inductors and LEDs, you have just placed (at the right of the board) and spin them 90 degrees, so they are oriented vertically, which is how you want them placed.

9. Complete the placement of components on the board, using all the commands you have already practiced, including: **Edit > Move**, **Edit > Spin**, **Edit > Mirror**, **Place > Manually**, and **Edit > Delete**.

Note

View the information in the Status window above the command line to see which component is attached to your cursor.

To see which refdes values go with which component, you can open the *placed_con.brd* file in the *solutions* directory for reference.

    a. Click the **Show Element** icon to select a component and determine which room, if any, the component may be assigned to.

    b. Use the **Edit > Mirror** command to move the three round LEDs to the top of the board and place them in the LED room.

    c. Use the **Edit > Mirror** command to move the six round inductors to the top of the board and place them, three each, in their respective CHAN1 and CHAN2 rooms.

Below is a table of the rooms defined and the parts that should be placed in each room:

Room	List of components (by RefDes)
MEM	U10, U11, U12, U13, U14, U15, U16, U17, C15, C16, C17, C18, C19, C20, C21, C22
LED	U6, D1, D2, D3, D4, R1, R2, R3, R4
CHAN1	U8, U18, U19, U20, J2, L1, L3, L4, C5, C23, C24, C25, R15, R16
CHAN2	U9, U21, U22, U23, J3, L2, L5, L6, C6, C26, C27, C28, R14, R17, R18

10. When you have completed manual placement, choose **File > Save As** from the top menu.

11. Rename this drawing by entering the following in the File Name field:

    placed

12. Click **Save** to save the *placed.brd* file.

Generating Reports

1. To create a report of placed components, choose **Tools > Reports**.

A Reports form appears.
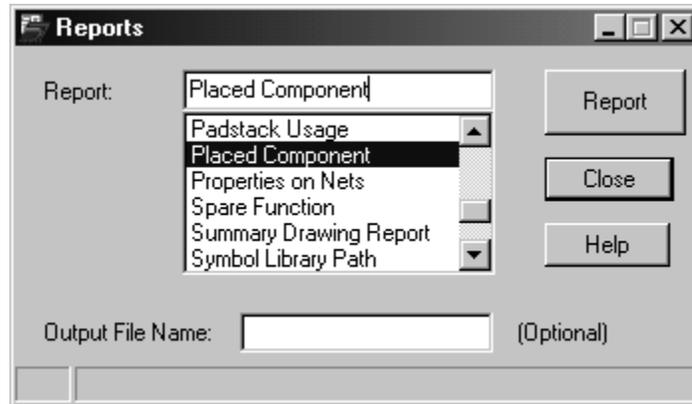
2. Use the scroll bar in the Report field to view all the available types of reports that you can generate.

3. Select the **Placed Component** report, then click **Report**.

   A Report window appears with a list of all placed components. In this case, the report should show you have placed all 82 components.

4. Click **Close** to exit from the Report window.

5. To create a report of unplaced components, select **Unplaced Components** from the scroll list.

6. Click **Report**.

   The Unplaced Component Report form appears.

7. Exit from the Report window by clicking on **Close**.

8. Exit the Reports form by clicking on **Close**.

   If there were any components that appeared in the Unplaced Components report, make sure to place them before continuing.

9. Choose **File > Save** from the top menu.

   A window appears and warns you that the *placed.brd* file already exists, and asks you whether you want to overwrite the file.

10. Click **Yes** to confirm the overwrite.

   The file *placed.brd* is written to disk.

STOP **End of Lab**

Deleting Components
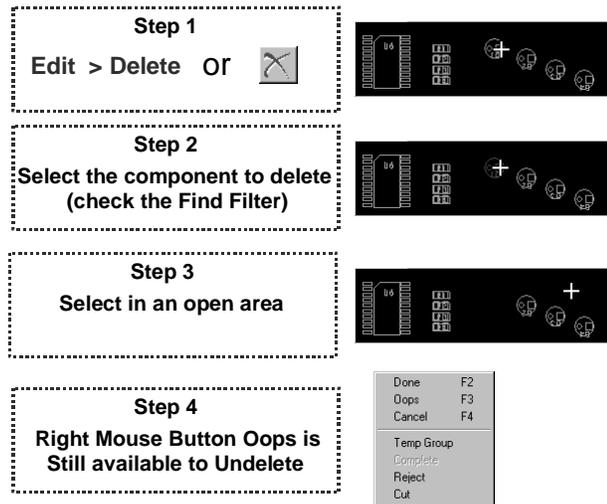
More Information

You use the standard **Edit > Delete** command to delete components from the board. However, components are not really deleted, but merely unplaced in the design. You can never delete logical parts from within Allegro.

You can delete individual parts from the board or delete a group of components by dragging the mouse and forming a rectangle around a series of parts. Also remember that parts that have the **FIXED** property will not be deleted.

Note

Make sure to check your Find Filter when attempting to delete parts from your design. If Symbols is not checked, you will not be able to delete the parts desired.

Lab

◆ Lab: Removing Components from the Board

■ Learn how to use the **Delete** command to remove and replace board components.

More Information

The following lab will allow you to familiarize yourself with the process required to remove and then replace parts in your design.

Lab 8-5: Removing Components from the Board

Objective: Learn how to use the **Delete** command to remove and replace board components.

To give you an idea of how easily components may be placed, you're going to first delete a component, then place it back again onto the board.

1. Choose **Edit > Delete** from the top menu.

2. Click on one of the ICs you have already placed.

   The component is highlighted, giving you a chance to verify that this is a component you really want to delete. If you made a mistake, at this point you could choose **Oops** from the pop-up menu.

3. Click again on this component to delete it.

   The component is deleted from the board, but *not* from the component database.

4. Choose **Done** from the pop-up menu to end the Delete mode.

5. Use the **Place > Manually** command to place the part back in its original location. Once you have completed the replacement, choose **Done** from the pop-up menu.

6. Choose **File > Exit** from the top menu.

7. When asked whether you want to save changes, click **NO** to exit your design.

STOP **End of Lab**

Lesson 9:   Advanced Placement

Learning Objectives

- ◆ Turn ratsnests on and off to selectively place nets and components.

- ◆ Use interactive and auto swapping for pins and gates.

- ◆ Apply advanced placement techniques to place components.

- ◆ Update symbols and padstacks that have changed.

- ◆ Perform cross selection or cross placement between Allegro and Concept or Capture.

Summary

In this section you will learn some advanced placement techniques that can be used to aid you in the placement and ultimately the routing of your design. These techniques include controlling the display of ratsnests, swapping pins, components and gates, and cross probing between Concept or Capture and Allegro. You will also learn what steps are required when a physical library part is modified.

Ratsnest

Display > Show Rats >	→	**All** **Components** **Nets**
Display > Blank Rats >		
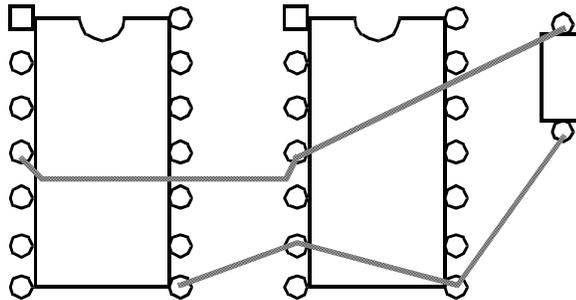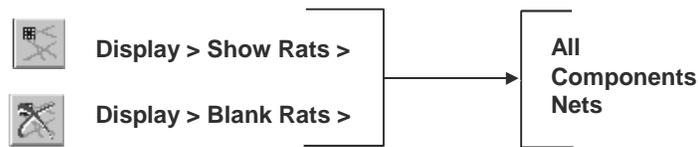
More Information

Ratsnests are lines displayed between the pins of an unconnected net. They show a relationship between pins having the same netname.

Ratsnest lines can be very useful placement aids. Displaying ratsnests can help identify congested areas. Ratsnests can also help evaluate the 'flow' within and between functional blocks of logic.

To display ratsnests, select **Display** from the top menu. The following sub-menus are available:

■ Show Rats

- ● **All** displays ratsnest lines for all nets, except those nets having a NO_RAT property attached (such as VCC, GND).
- ● **Components** displays all ratsnest lines to pins on the part(s) you select. Select the part(s) with your left mouse button, or use the Find by Name section of the Find Filter to enter a reference designator or a file of reference designators.
- ● **Net** displays all ratsnest lines to pins on the net(s) you select. Select a pin(s) with your left mouse button, or use the Find by Name section of the Find Filter to enter a netname or a file of netnames.

■ Blank Rats

- ● **All** blanks all ratsnest lines currently displayed.
- ● **Components** removes ratsnest display for specified part(s).
- ● **Net** removes ratsnest display for specified net(s).

Lab

◆ Lab: Displaying Ratsnests

■ Turn ratsnests on and off to view and hide selected nets and components.

More Information

The following lab will allow you to familiarize yourself with the process required to display and blank ratsnests in your design.

Lab 9-1:   Displaying Ratsnests

Objective: Turn ratsnests on and off to selectively view and hide nets.

1. Start Allegro and open the *placed.brd* file if it is the current design.

2. To blank all ratsnest lines, choose **Display > Blank Rats > All**.

3. To display rats by component, choose **Display > Show Rats > Components**.

4. Click on a component.

    Ratsnest lines appear for all signals that exist on the component you picked. The appearance of the ratsnests is cumulative as you select more components.

5. Choose **Display > Blank Rats > All** from the top menu.

> ## Note
>
> You can also use the **Unrats All** and **Rats All** icons for turning ratsnests on and off.

Unrats All ⟶ [icons] ⟵ Rats All

6. To display ratsnest lines for a particular signal, choose **Display > Show Rats > Net**.

7. If necessary, click the **Find** tab to bring the Find Filter to the front.

8. In the Find By Name section, select **NET** from the drop-down list, and enter **aen** in the **>** field, as shown in the figure:

    ```
    ┌─ Find By Name ──────────────┐
    │ Net            ▼   Name ▼   │
    │ >  aen             More...  │
    └─────────────────────────────┘
    ```

    The AEN rat is displayed.

9. Right click and choose **Done**.

10. Choose **Display > Blank Rats > All** from the top menu.

Automatic Swapping of Functions and Pins

Gate swapping **Pin swapping**
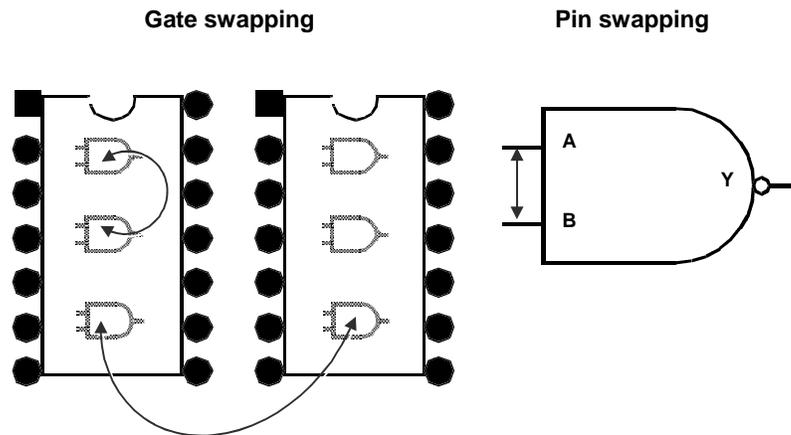
More Information

After component packages are placed on your board design, you can use the Allegro tool's automatic pin and gate swapping features to further reduce signal lengths and improve connectivity. By allowing these swapping processes to occur, you improve the chances for a 100% complete automatic route.

As shown, swapping features include the following possibilities:

■ Gates and functions can be swapped within a package.

■ Gates and functions can be swapped between packages of like type.

■ Swappable pins within a gate or function can be swapped.

You can perform pin and gate swapping on devices that meet at least one of the following requirements:

■ The device is described in Concept or Capture and contains pin and/or gate information.

■ An associated device file has been used that contains pin and/or gate information.

Note

Devices that have been loaded into your design through a third-party netlist must use device files that contain pin and/or gate information, or else swapping will not be available for these devices. You can find more information in the online Help files.

Using Automatic Swap

Place > Autoswap > Parameters

Click OK to start autoswapping
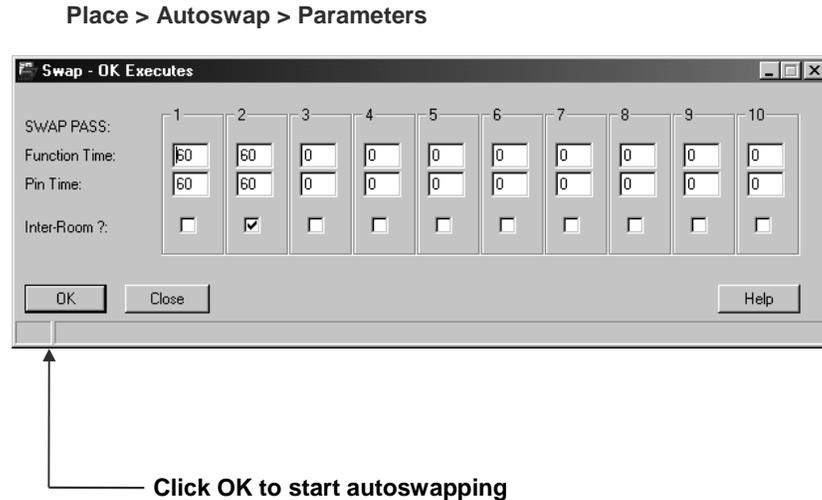
More Information

Before running automatic swap you must set the swap parameters. You access the swap parameter by selecting **Place > Autoswap > Parameters** from the top menu. The Swap form lets you define parameters for ten swapping passes. For each pass, you can set the time limit and indicate whether inter-room swaps are permitted. Both function and pin swaps can occur in each pass. By default, the Allegro tool allows two passes with a time limit of 60 minutes each, although it is likely that most passes will not require 60 minutes.

Allegro completes each swap pass by running the function swap first, then the pin swap. It is recommended that you set a high number for each swap time so the Allegro tool will have enough time to perform the necessary swaps. Allegro automatically moves to the next pass when it has completed all appropriate swaps for the given pass.

There are several component and net properties that affect how functions are swapped and how swappable pins are changed. These properties are explained later in the chapter.

Note

Function or gate information, as well as swappable pin information, must be present in order for swapping to occur. You can enter this information in your design through the schematic or through device files.

Note

The **OK** button starts execution. If you want to close the form without running automatic swap, use the **Close** button.

Running Automatic Swap

1. Define the area to considered:
- Design
- Room
- Window

2. Click **OK** in the Parameters menu to run automatic swap.

3. View changes to the ratsnest display.

4. Use **File > Viewlog** to view the *swap.log* file for information on swapping improvements.

5. Choose **Tools > Reports** to generate and view the following swap-related information:
- Function report
- Function pin report
- Spare function report

More Information

Execute

> When you click **OK** in the Swap parameter window, the Allegro tool examines all function pairs that can be swapped, then all pin pairs that can be swapped. The program tool continues to search for eligible swaps that shorten the total design wire length until it either runs out of time or finds no more suitable swap candidates. When swapping pins on ECL nets, automatic swap maintains the correct ECL scheduling.

Evaluate

- View the *swap.log* file for information on swapping improvements. (Use **File > Viewlog**.)

- Select **Tools > Reports** for the following swap-related placement reports:
  - Function report
  - Function Pin report
 - Spare Function report

Interactive Swap

Place > Swap > … | Pins
                   | Functions
                   | Components

Component   **Pins and Functions**
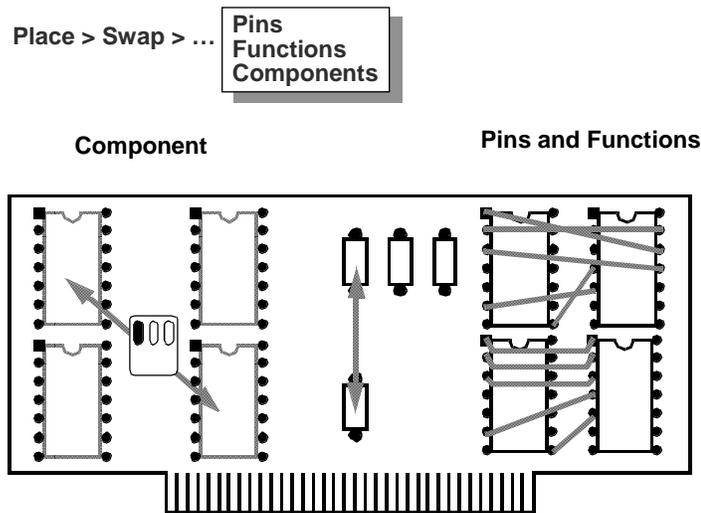
More Information

When displaying ratsnests, you may discover gate-to-slot or pin-to-net assignments that create unnecessary congestion. Manual gate and pin swapping can reduce such congestion and allow the ratsnests to flow in a more organized manner, which helps routing. See the lesson titled *Importing Logic Information into Allegro* for more details on which part definition statements are required in order to support gate and pin swapping.

■   **Pins** lets you select two equivalent pins for swapping (for example, inputs on a nand2, or inputs on a resistor pack).

A

B

Y
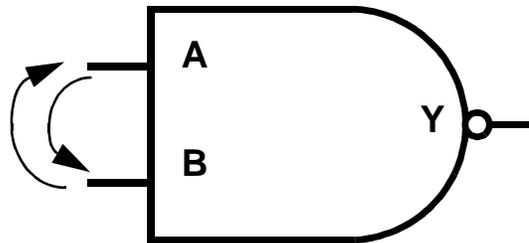
■   **Functions** lets you select two equivalent gates for swapping.
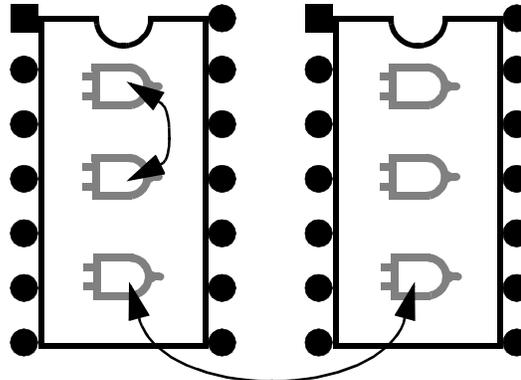
■ **Components** trades locations of two entire packages.

Lab

◆ Lab: Swapping Components, Pins, and Functions

■ Use manual and automatic swapping to exchange components, pins, functions.

More Information

The following lab will allow you to familiarize yourself with the process required to swap components, pins and functions (or gates) in your design.

Lab 9-2:   Swapping Components, Pins, and Functions

Objective: Use manual and automatic component, pin, and gate swapping to improve routing.

When placing components, you can achieve better routing results downstream by minimizing signal crossings, roughly indicated by the ratsnest lines between pins. You can always swap placed components, which is especially effective when the components are of similar size and shape. On some designs you have the option of swapping permutable pins and gates. By swapping pins and gates you can have a cleaner arrangement of conductors.

Swapping Components

At this point, you can turn on the ratsnests to see how the pins for each net are arranged.

1. Turn all the ratsnests on by choosing **Display > Show Rats > All** from the top menu.

2. Choose **Place > Swap > Components** from the main menu.

3. Click two parts for swapping, such as adjacent ICs in the MEM room at the upper right of the board.

    The two parts are swapped.

4. Try swapping several other pairs of components and see whether you can reduce the complexity of the ratsnest.

5. When you are through swapping, right-click and choose **Done** from the pop-up menu.

6. Practice this command with other pairs of parts.

Note

ICs U10 through U17 have a ROOM property of MEM and should therefore be placed in the MEM room. Check the room properties of the ICs you place to verify they are in their proper rooms.

Swapping Pins or Functions (Gates)

After swapping physical package locations, you can further optimize your placement through gate and pin swapping. To demonstrate this, you will work with U4, an SOIC48 designated with a FCT16245 function. Not all components are defined for pin or gate swapping, but U4—a component you have already placed—does have definitions for function (gate) swapping.

1. Zoom in to the area of your design where U4 has been placed.

2. Click the **Rats All** icon to display all ratsnest lines.

3. Choose **Place > Swap > Functions** from the top menu.

Note

You can also choose **Place > Swap > Pins** if you want to swap pins.

4. Select a pin on **U4** that has a ratsnest line.

   If the pin you selected belongs to a function that can be swapped, the pins of other functions that can also be swapped are highlighted.

5. Select a second pin from the highlighted choices.

Before function swapping.   **After function swapping.**
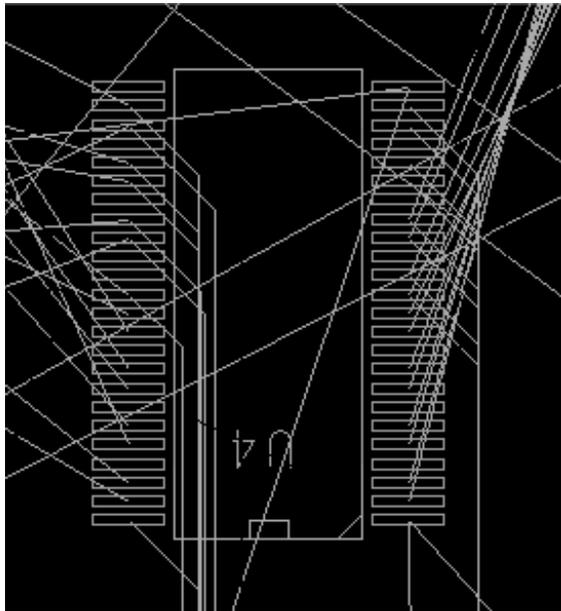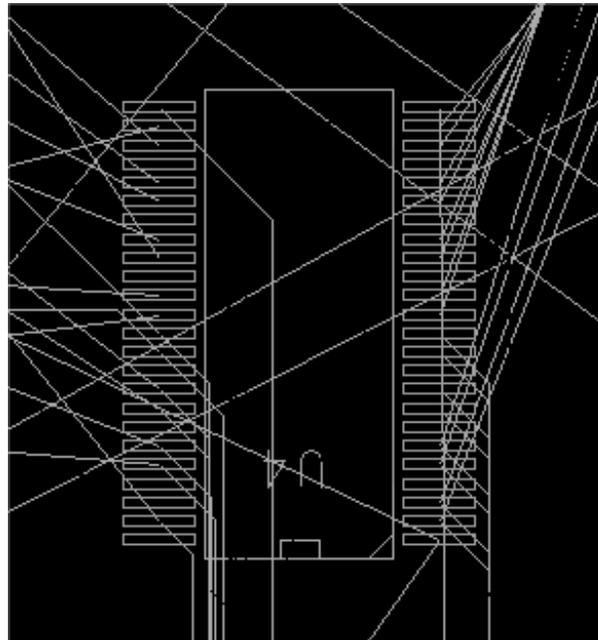
6. Right click and choose **Done** from the pop-up menu.

   The ratsnest lines for the two gates are swapped.

Using Autoswap

1. To access the automatic swap commands, choose **Place > Autoswap > Parameters**.

    The Swap parameters form appears.

2. Use the settings shown below in the Swap parameters form:

3. Click **Swap** to close the form and begin execution.

    You see ratsnest lines changing as pin and gate swapping occurs.

4. Choose **File > Viewlog** to read the log file report.

5. Click **Close** to exit the log file window.

6. Choose **File > Save** from the top menu.

    A window appears and warns you that the *placed.brd* file already exists. It asks if you want to overwrite the file.

7. Click **Yes** to confirm the overwrite.

    The file *placed.brd* is written to disk.

[STOP] **End of Lab**

Selecting alternate packages

ALT_SYMBOLS = '(TOP: SOIC14; BOTTOM: SOIC14_PE)'
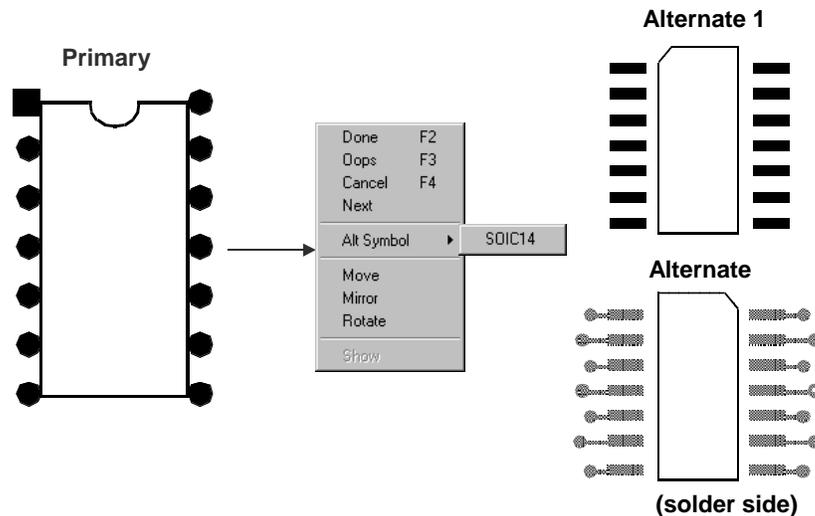
Summary

It is important to remember that you will only be able to use Alternate symbols when they are defined by your schematic capture tool. You cannot add the ALTERNATE_SYMBOL property inside Allegro. If this property is not defined as part of the schematic part, you will not be able to use Alternate symbols when placing your parts.

More Information

When you place a part, the primary package symbol is attached to your cursor by default. This primary package symbol is contained in the part definition file (*pstchip.dat* for Concept or Capture, or a device file for Third Party).

To select an alternate package symbol for the part being placed, click the right mouse button and move to the **Alt Symbol** option. All available Alternate symbols will be displayed in a separate pop-up menu for the side of the board currently active. (If no alternate symbol statement exists in the part definition file, the **Alt Symbol** option will appear "greyed out" in the right mouse pop-up menu.)

You can specify alternate packages for the top and bottom of the board (see example). When placing a part on the top side, the **Alt Symbol** option displays the package symbols listed for the top. When alternate symbols are defined for the bottom side, the **Mirror** command also changes the package symbol popup accordingly (else the current package is mirrored). Setting the **Mirror** switch in the Drawing Options form also allows access to any alternate symbols for bottom side placement.

Alternate symbol functionality lets you toggle between through-hole and surface-mount package styles. It also lets you adjust pad sizes for surface-mount discretes to accommodate different assembly processes for the top (vapor phase or infrared reflow) or bottom (wave solder). To specify multiple alternate symbols per side, use a comma to separate them. For example:

```
alt_symbols='(T:soic14,soic14_pe; B:soic14_pe)'
```

Updating Symbols in a Design

Place > Update Symbols…

**Reads padstack data
from the library**
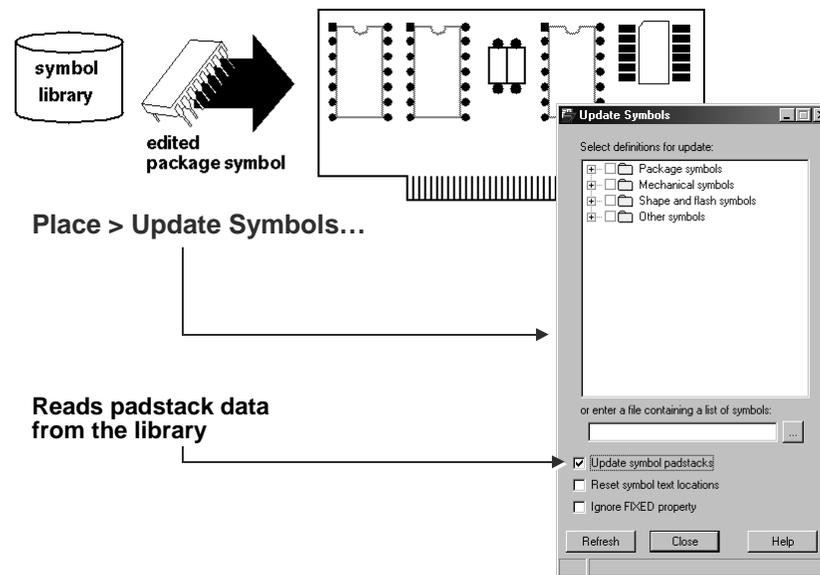
Summary

When you place a part in your design, a copy of the package symbol is stored in the Allegro database. This means that any changes made to the footprint library after placement are NOT reflected in the design. When you execute the **Update Symbols** command, the shown form is displayed. You specify through the different symbol folders which type of symbols need to be updated, such as package symbols, mechanical symbols, and so forth.

When you select the **Refresh** button, the update symbol routine is run. This routine will update the requested symbols from the library into your current design, resulting in the board design now matching the library.

More Information

After placing parts in a design, you might discover an error in a package symbol (for example, wrong pin spacing, wrong padstack name assigned to pins, inaccurate device outline, and so forth). The following method is recommended for correcting the problem:

- Use the Symbol Editor to edit the package symbol, and fix the mistake at the library level (so the same problem will not be experienced by other users).

- Move pins to the proper location.

- Use **Replace Padstack** to reassign the proper padstack name to symbol pins.

- Edit the assembly and/or silkscreen outline, refdes label location, and so forth.

Correcting the package symbol in the library has no effect on the design file (the design still contains copies of the incorrect package symbols). You must "swap" the package symbols in your design with the newer versions stored in the library.

- Use **Place > Update Symbols** to replace the package symbols in your design with updated copies from the library. This method ensures that the parts in your design match the library parts. Various options let you control which symbols get updated.

Use the **Update Symbol Padstacks** option to replace padstacks in your design with padstacks found in the library.

Updating Padstacks

Tools > Padstack > Refresh
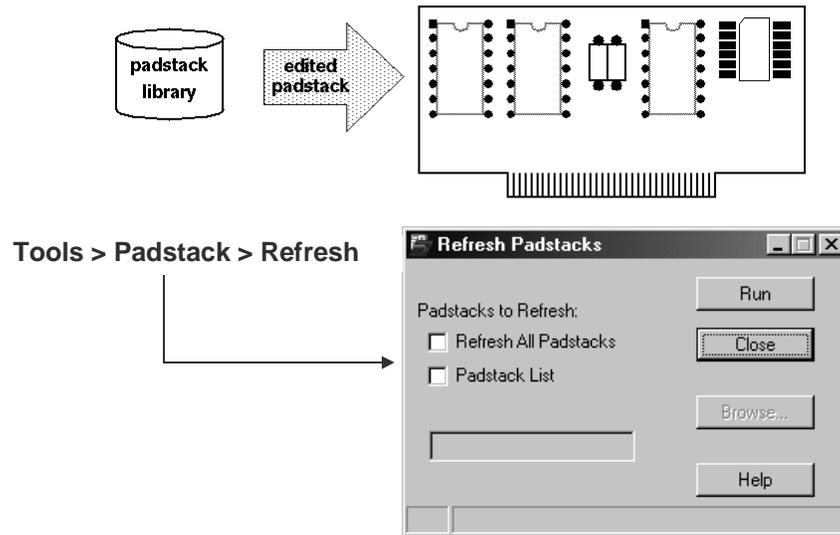
Summary

When you place a part in your design, a copy of the padstack is also stored in the Allegro database. This means that any changes made to the padstack library after placement are NOT reflected in the design. By using the Refresh Padstack option from the top menu, the shown form is displayed. You specify to update all padstacks in the design, or only padstacks whose names appear in a disk file you must create. When you select the **Run** button, the Refresh Padstack routine is run. This routine will update the requested padstacks from the library into your current design, resulting in the board design now matching the library.

More Information

Use the Refresh Padstacks dialog box to update any or all padstacks in a design to agree with the library padstacks.

Refresh All Padstacks indicates you want to update all padstacks in the design to agree with the library padstacks.

Padstack List indicates you want to update only the padstacks in the named list to agree with the library padstacks. The padstack list can be stored in an ASCII text file that has a *.lst* file extension.

Modifying Padstacks

Tools > Padstack > Modify Design Padstack
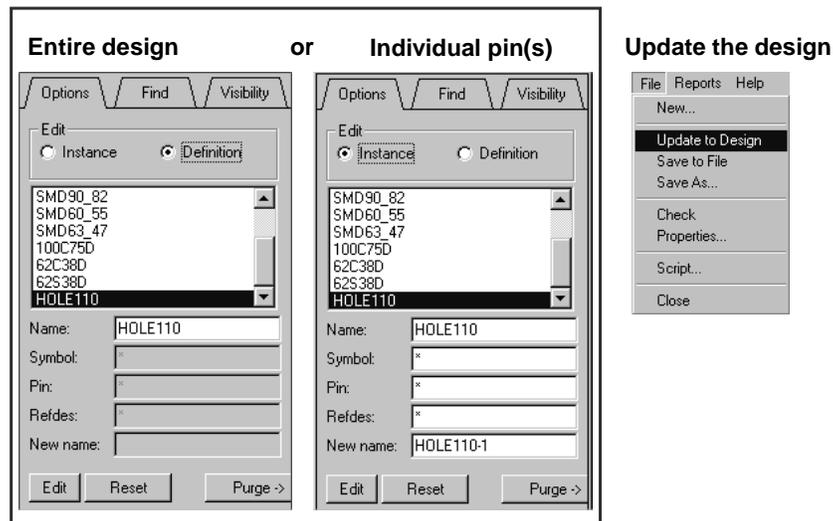
More Information

When you create a library padstack, you can specifically define internal layers (SIG2), or interpret them from any wildcard (SIG*) or DEFAULT_INTERNAL layers. Once the padstack is used in a design file, the layers in the library padstack are mapped to the cross section of the design. For example, BEGIN_LAYER and END_LAYER become Top and Bottom. (If layers in the library padstack have no match in the design cross section, they are not used.). You can modify the padstack within the design if the original values need to be modified/changed for any reason. The standard Padstack Designer forms are used to update the padstack within the design.

Definition - You edit the padstack description within the context of the entire design. Every occurrence of this padstack found in the design is modified.

Instance - You edit the padstack description for a certain pin(s) within the design. Wildcards may be used in any/all of the Symbol/Pin/Ref Des fields. The New Name field will contain a new padstack name automatically generated by the software. This is to differentiate the new padstack definition from the original padstack definition.

After modifying the padstack, you save the changes. Use the **File > Update to Design** command from the top menu in the Padstack Designer form. This saves the modified padstack "inside" the design only. To save the modified padstack to disk, use the **File > Save** or **File > Save As** command from the Padstack Designer form.

The **Tools > Padstack > Modify Library Padstack** command is used to update the library padstack. A browser is presented for choosing which padstack to be modified. You must have write permissions for the library in order to update the padstack.

Creating a Library from a Design

File > Export > Libraries
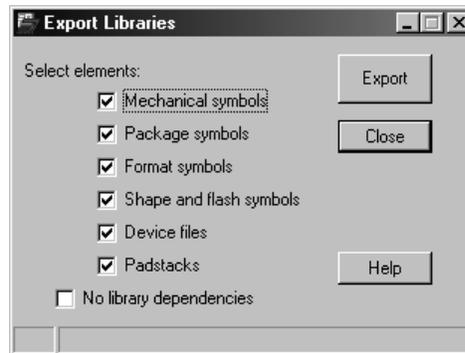
More Information

Select **File > Export > Libraries** to create library definitions from a layout drawing.

The Export Libraries feature creates mechanical symbols, package symbols, format symbols, shape symbols, flash symbols, device files, and padstack files. It also creates all symbol-related drawing files.

⚠ Caution

All files are written into your current working directory; therefore, it is to your advantage to move to an empty directory just prior to invoking this command. To change your current working directory, type **cd directory_name** on the Allegro command line.

Lab

◆ Lab: Advanced Placement with ALT_SYMBOL

  ■ Use the ALT_SYMBOL property to place alternate versions of a component.

More Information

The following lab will allow you to familiarize yourself with the process required to use alternate symbols when placing parts in your design. Remember, you can only use alternate symbols if they have been set up correctly in your front end library.

Lab 9-3:   Advanced Placement with ALT_SYMBOL

Objective: Learn how to use ALT_SYMBOL for placing alternative parts.

This exercise shows how you can use the ALT_SYMBOL property to select alternate package styles during interactive placement. This lab also shows you how to "tag" parts for interactive placement.

Note

This lab is optional. *DO NOT SAVE* the results.

Opening a Previous Design

1. Choose **File > Open** from the Allegro top menu.

    A browser form appears.

2. Enter or click on the name of an unpopulated version of this design:

    unplaced

3. Click **Open** to close the browser form.

Using the ALT_SYMBOL Property

The component specified in this exercise has an ALT_SYMBOL property attached to it. First let's make sure that the bottom-side objects will be visible.

1. Click the **Color** icon and use the Color and Visibility form to turn ON the following classes and subclasses. (You can also change the bottom-side colors if you wish.)

GROUP	CLASS	SUBCLASS
Components	REF DES	ASSEMBLY_BOTTOM
Geometry	PACKAGE GEOMETRY	ASSEMBLY_BOTTOM
Stackup	ETCH	BOTTOM
Stackup	PIN	BOTTOM

2. Click **OK** to close the Color and Visibility form.

3. From the top menu, choose **Place > Manually**.

    The Placement form appears.

4. Select the **Placement List** tab to bring it forward if is not already there.

5. Expand the **Components by refdes** folder.

6. Scroll through the list and click the box to the left of **U2**.

    An outline view of the footprint is displayed in the Quickview window. The Allegro message area states:

    ```
    Placing U22 / 20L10_DIP-BASE / DIP24
    ```

    This part currently appears as a 24-pin DIP. The physical package is attached to your cursor for placement. Before placing U2, you must first change the package type.

7. Right click and choose **Alt Symbol** and **SOIC24** from the pop-up menu.

    The package style changes to a through-hole SOIC24.

8. Right click and choose **Mirror** from the pop-up menu.

    The part is mirrored to the bottom side of the design and the package style changes to a SOIC24_PE, a surface-mount part with pin escapes built into the footprint.

9. Click left to place **U2** on the bottom side of the board.

10. Right click and choose **Done** from the pop-up menu.

11. Choose **Display > Property** from the top menu.

    The Show Property form appears.

12. Select the **ALT_SYMBOLS** property from the scroll list.

13. Click **Show Val**.

    The Show window displays a list of part types that have alternate package styles defined.

14. Click **Close** in the Show window.

15. Click **OK** in the Show Property form.

16. Select **File > Exit** from the Allegro menu.

17. Select **No** to NOT save the design.

STOP **End of Lab**

Cross Placement with Concept

Place > Manually

Place the part in Allegro

Select the part in Concept
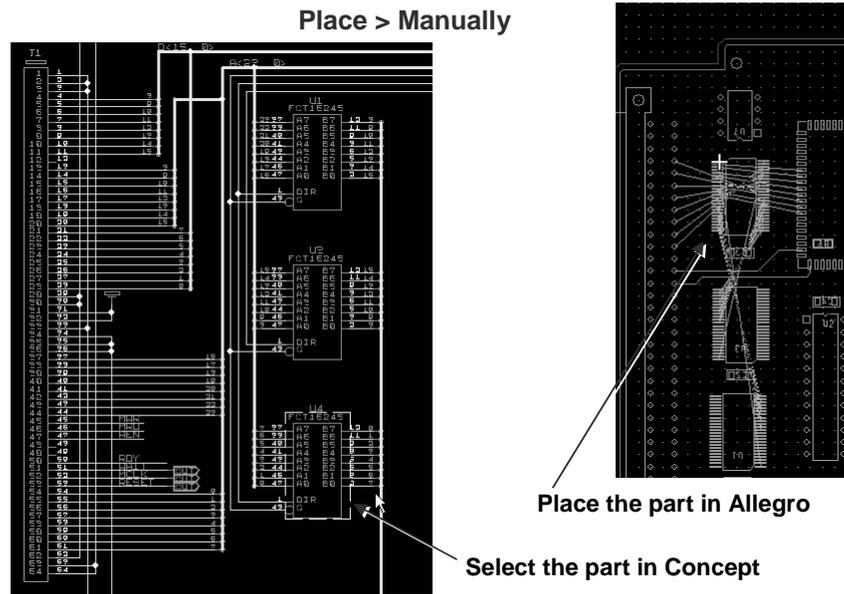
More Information

You can cross probe between Concept and Allegro at any time. In order to have this ability, you must initiate BOTH Concept and Allegro from within the Project Manager. You can place a part in Allegro by selecting the part in Concept, you can highlight parts in both Allegro and Concept by selecting the part in either system, and so on. Make sure you execute the Allegro command first (such as **Place > Manually** or **Display > Highlight**) before selecting the parts, nets, and so on in Concept.

Cross Selection with Capture

Have Allegro open after netlisting

Options > Preferences
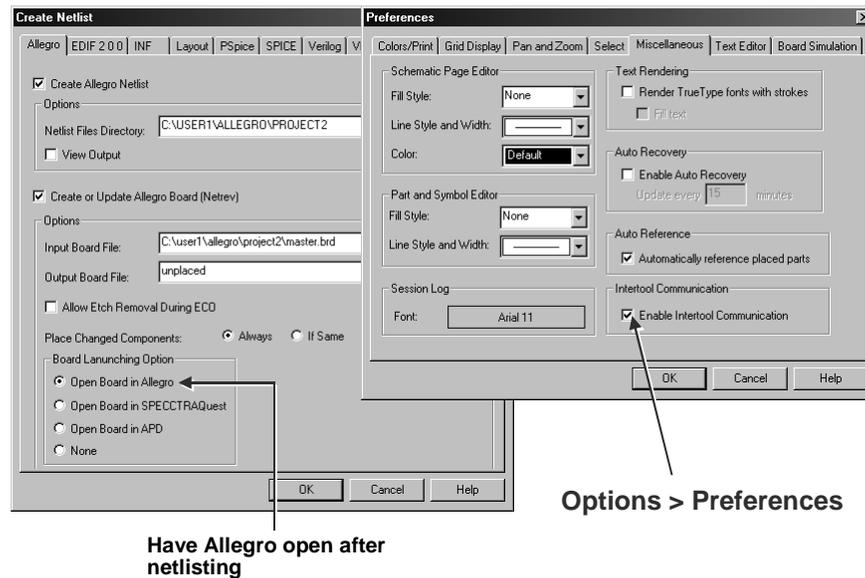
More Information

If you use Capture to create your schematics, you have the ability to cross-probe with Allegro. There are two methods by which you can perform cross-probing between the two systems.

First, when you run the Capture netlist program, you enable the Open Board in Allegro option. After the netlist has been successfully created, Allegro will automatically be launched and you can perform the cross-probing commands such as placement, highlighting, and so forth.

The second method to perform cross-probing is to use Intertool Communication. You can launch both Allegro and Capture manually using this mode. To enable Intertool Communication, from Capture, select **Options > Preferences**, select the **Miscellaneous** tab, and check the **Enable Intertool Communication** option.

Important

Remember that you must first start an Allegro command, such as place, delete and so forth, BEFORE selecting the object in the Capture schematic. If no Allegro command is active, and you select an object in Capture, the default command is the Allegro "highlight" command. If the object selected is not yet available, you will get an error message on the Allegro command line.

Labs

- ◆ Lab: Using the Concept Schematic for Manual Pplacement
  - ■ Use cross placement to place components between Concept and Allegro.
- ◆ Lab: Using the Capture Schematic for Manual Placement
  - ■ Move parts using cross selection and cross highlighting between Capture and Allegro.

More Information

The following lab will allow you to familiarize yourself with the process and steps required to cross probe between either Concept or Capture and Allegro. Remember, you can only perform these steps if you used Concept or Capture as the front-end tool when you imported your schematics into Allegro.

Lab 9-4:   Using the Concept Schematic for Manual Placement

Objective: Use the Concept schematic to select and place components in the physical layout.

This section requires that you have loaded logic data from a Concept schematic. You will move components from the Concept schematic window to the Allegro design window. To assure communication between Concept and Allegro schematics, both software tools should be opened from the Project Manager.

Note

If you have loaded your data from the Capture schematic tool, you should skip this lab and move to the next lab, *Using the Capture Schematic for Manual Placement.* If you have loaded your data as a third-party netlist, skip this lab and move on to the next lesson, *Routing*.

Starting the Project Manager

A project configuration has been set up for you that defines schematic files, libraries, and layout files associated with your project. Use one of the following methods to start the Project Manager on your platform.

1. To start the Project Manager, do one of the following:

    a. From Windows, choose **Start > Programs > Cadence PSD 14.2 > Project Manager**.

    b. In UNIX enter the following command in a UNIX shell:

    projmgr

    The Project Manager form opens or the Project Manager Product Choices dialog box displays.

2. If the Project Manager Product Choices dialog box displays, select **PCB Design Studio** and click **OK**.

3. Click the **Open Project** button in the middle of the Project Manager.

Opening the Project

When you click Open in the Project Manager form, a file browser window appears.

1. Navigate to the *project1* directory. Select ***project1.cpm***, then click **Open**, as shown in the figure:
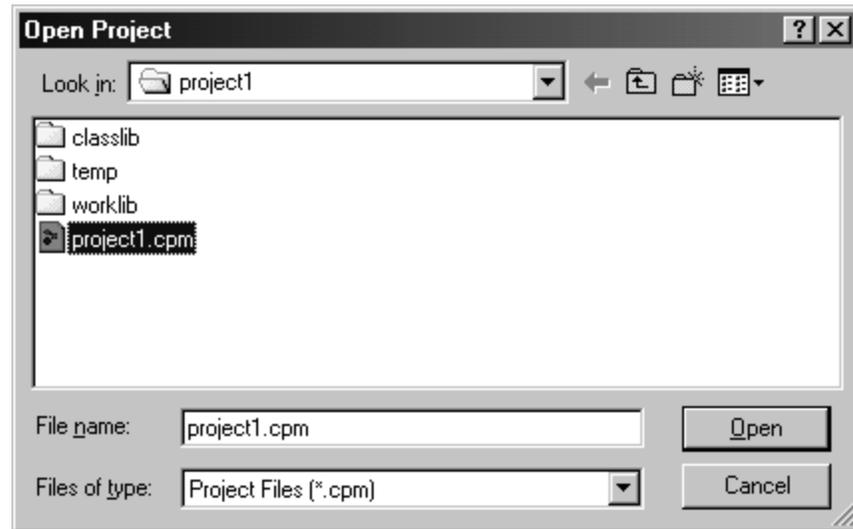
The Project Manager form changes and other large buttons appear.

2. Click **Design Entry**.

   The Concept program starts and a schematic appears.

3. Resize the Concept schematic window to fill most of the left half of your screen.

4. In the Project Manager form, click **Layout**.

   The Allegro program starts and your most recent design, *placed.brd*, appears.

5. Resize the Allegro window to fill the right half of your screen.

   You are ready to use both the Concept and Allegro windows from the same screen.

Placing Components Between Concept and Allegro

1. In the Allegro window, choose **Place > Manually**.

   The Placement form appears.

2. Move the cursor to the Concept window and click on one of the components.

   The Concept tool acknowledges your selection by drawing a dashed-line rectangle around the component.

3. Move your cursor back to the Allegro window and notice that you are dragging a physical component package.

4. Click anywhere in the Allegro design window to place the component.

5. Repeat the previous three steps to place a few more components.

6. Click **Cancel** from the Placement form in the Allegro window.

7. In preparation for the next lab, you can free some system resources by using the following steps:

   a. Choose **File > Exit** to close the Concept window.

   b. Choose **File > Exit** to close the Allegro window.

   c. Choose **File > Exit** to close the Project Manager window.

STOP **End of Lab**

Lab 9-5:   Using the Capture Schematic for Manual Placement

Objective: Use the Capture schematic to select and place components in the physical layout.

In this lab, you will use the Capture schematic to place and move components in the Allegro design.

Opening Capture

1. To start the Capture tool, choose **Start > Programs > Cadence PSD 14.2 > Capture**.

   The Capture window displays with no projects open.

2. Choose **File > Open > Project**.

   A file browser window opens.

3. Navigate to the *project2* working directory, select *release.opj*, and click **Open**.
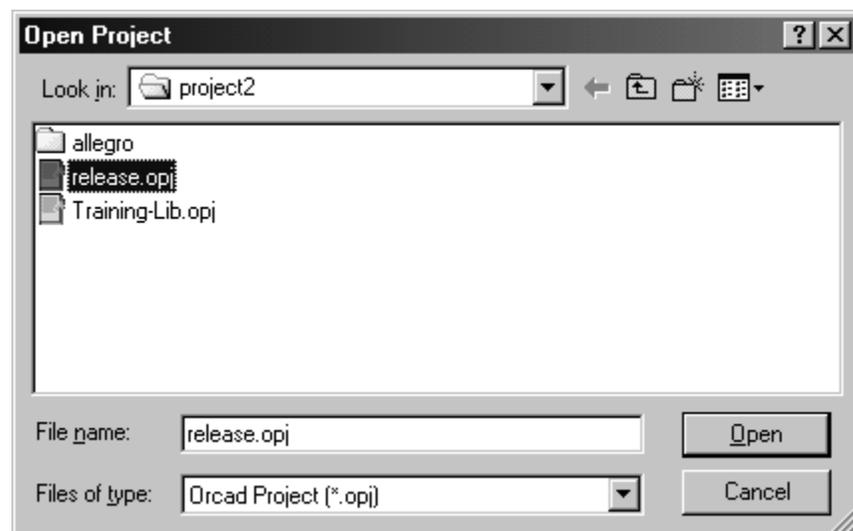
4. Choose **Options > Preferences**.

5. In the Miscellaneous tab, make sure the **Enable Intertool Communication** option is checked, then click **OK**.

6. Open Page 1 of the Root Schematic.

Cross Selecting Between Capture and Allegro

1. Start Allegro and open the *placed.brd* file if it is not the active design.

2. Arrange Capture and Allegro so that they each occupy half of your screen, one on the left side, the other on the right.

3. In the Allegro window, choose **View > Zoom Fit** to see all of the
    Allegro board.

4. In the Allegro window, choose **Edit > Move**.

5. Move the cursor into the Capture Page 1 schematic window and select
    one of the FCT components.

    The component you selected in Capture is attached to your cursor in
    Allegro.

6. Practice cross selecting components in Capture and moving them in
    Allegro. When you are finished, right-click and choose **Done** from the
    pop-up menu in Allegro.

Cross Highlighting and Dehighlighting Between Allegro and Capture

1. In Allegro, choose **Display > Highlight**.

2. Click on a part in Allegro.

    The corresponding component in Capture is selected.

3. Click on several more parts in Allegro.

    The corresponding components in Capture are selected. The selection
    in Capture is cumulative. If a different schematic page contains the
    component you've selected in Allegro, the page opens in Capture.

4. In Allegro, choose **Display > Dehighlight**.

5. Click one of the previously highlighted parts in Allegro.

    The corresponding component in Capture is unselected.

6. Continue dehighlighting parts in Allegro until you have unselected all
    the selected components in Capture.

7. Exit Capture and exit Allegro. You do not need to save these designs.

STOP **End of Lab**

Lesson 10: Routing and Glossing

Learning Objectives

- Define and display etch grids used for routing.

- Add and delete connect lines (*clines*) and vias.

- Prepare for autorouting by creating preliminary embedded planes.

- Route net connections with SPECCTRA.

- Use **Slide** and **Replace Etch** to improve routing.

- Learn techniques for replacing etch and how to use the **Cut** option in conjunction with other etch editing commands.

- Gloss the routing in the design

Summary

In this module you will learn how to interactively route your printed circuit board. You will learn how to add etch to make signal connections and will also learn the commands used to edit existing etch on the board.

You will use the SPECCTRA router to autoroute your design. However, this is not meant to be a course on how to use SPECCTRA. If you wish to learn the details of SPECCTRA, you should take the SPECCTRA courses available which are:

- SPECCTRA AutoRoute Basics

- Advanced SPECCTRA Autorouting Techniques

Design Layout Process

```
┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│ HDL/schematic│→  │ Define board │→  │ Load logic   │→  │ Set/check CBD│
│ design capture│   │ mechanical   │   │ data         │   │ rules and    │
│              │   │ stackup      │   │              │   │ constraints  │
└──────────────┘   └──────────────┘   └──────────────┘   └──────────────┘
                                                                   │
                                                                   ↓
                                                          ┌──────────────┐
                                                          │ Arrange/place│
                                                          │ components   │
                                                          └──────────────┘
┌──────────────┐        ┌──────────────┐                        │
│ Manufacturing│        │ Physical     │ ←──────────────────────┤
│ outputs      │        │ design       │                        ↓
│ check plots  │        │ analysis     │              ┌──────────────┐
│ aperture files│       └──────────────┘              │ Interactive  │
│ Gerber data  │                                      │ and automatic│
│ NC drill data│      YOU ARE ☞                       │ route signals│
│ silkscreens  │      HERE                            └──────────────┘
│ Assembly     │                                             │
│    drawings  │                                             ↓
│ fabrications │   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│    drawings  │ ← │ Generate     │ ← │ Define Power/│ ← │ Gloss/auto   │
│ reports      │   │ manufacturing│   │ GND planes   │   │ cleanup for  │
│ Autorename   │   │ output       │   │              │   │ manufacturing│
│ backannotation│  └──────────────┘   └──────────────┘   └──────────────┘
└──────────────┘
```

More Information

At this point in the design process, the logic has been loaded, the board mechanical has been defined, the design rules or constraints have been set, and the components have been placed. You will now route the design using both interactive and automatic techniques.

# Accessing interactive routing modes

More Information

Use a **route** command to access interactive route mode simply. When you use routing commands, the etch grid is displayed.

Icons associated with routing are:

- ■   **UnRats All** turns off all ratsnest lines.

- ■   **Rats All** turns on all ratsnest lines.

- ■   **Route Connect** is used to make electrical connections between pins.

- ■   **Slide** is used to move existing traces.

- ■   **Custom Smooth** is used to smooth or gloss individual nets while interactively routing traces.

- ■   **Edit Vertex** is used to add or remove vertices from existing traces.

- ■   **AutoRoute** opens an autorouting parameter form and lets you evoke the SPECCTRA router, but it does not access the SPECCTRA interactive user interface.

- ■   **SPECCTRA GUI** translates the current Allegro design and opens it in the SPECCTRA interactive user interface. By default, this icon is NOT part of the route toolbar. It must be added manually.

Routing Grids: Fixed
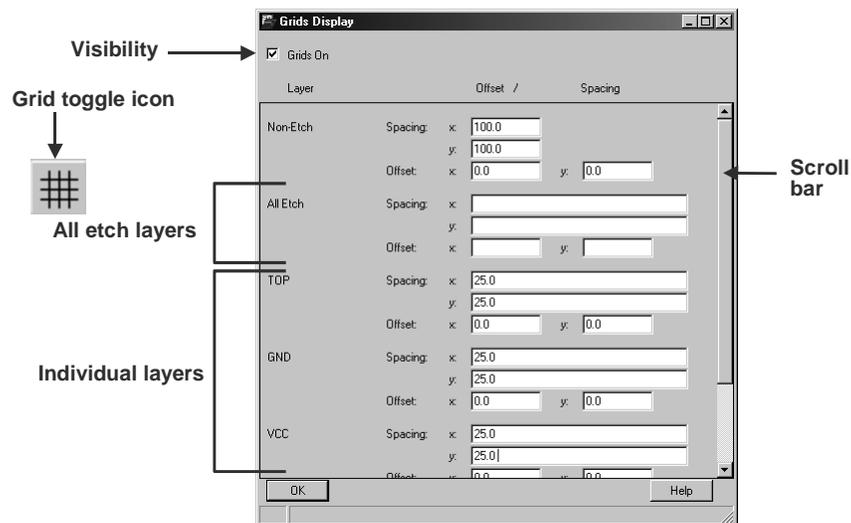
Summary

The etch grid is automatically displayed, if grids are visible, whenever a route command such as **Route Connect** is executed. This is the snap grid that is used when you graphically add route into your design using the left mouse button to select point. If you set the routing grid and your grid is displayed, but you still cannot see the routing grid, set the Class in the Options folder tab to Etch.

Remember to use the **Tab** key to move from one line of the form to another, not the **Return** key. The **Return** key will close the form.

More Information

Select **Setup > Grids** from the top menu to access the Grids Display form.

The form shows a fixed routing grid on all layers. A fixed grid system uses a consistent increment or spacing between grid lines in the x and y direction (usually defined with a single number, such as 25). This grid starts from the origin (0,0) of the layout drawing.

- ■ The **Grids** button at the top left of the form controls the visibility of the grid point display.

- ■ The **All Etch** section of the form is always blank. Entering the route grid here defines all the etch layers at once (so you don't have to enter a grid for each individual layer).

- ■ If you want to use a different route grid on a certain layer, enter it into the individual layer's section.

- ■ Use the scroll bar on the right side of the form to see all the individual layers.

# Routing Grids: Variable
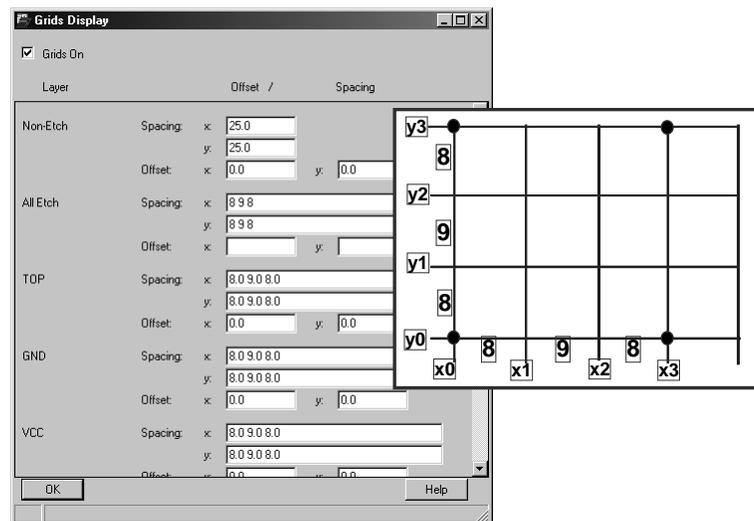
Summary

A variable grid is noticeable by the series of large and small grid points in the display area. Each large dot represents where the variable grid starts. In the example, notice there is a large dot, followed by an 8-mil space, a 9-mil space, and another 8-mil space. Then another large dot appears, representing where the pattern starts again.

More Information

The form shown depicts a variable 8, 9, 8 routing grid. A variable grid system uses a repetitive sequence of increments to define the grid spacing in the x or y direction.

■   Variable routing grids help to maximize available "real estate" by optimizing the number of potential routing channels.

■   Variable routing grids adapt well in mixed technology designs (boards with through-hole, surface-mount, and fine-pitch components).

■   Try to create a variable grid that will keep most of your component pins on a route grid. (For example, your grid should accommodate parts with 100-, 50-, and 25-mil pin pitch.)

Finding Nets or Reviewing Rats
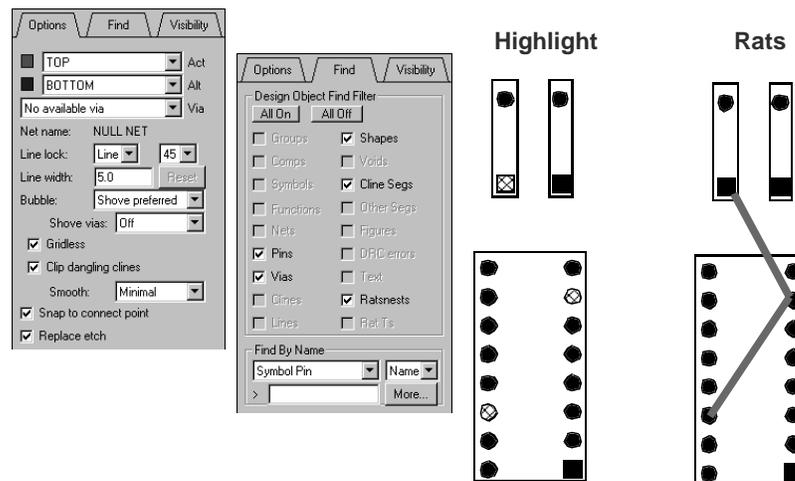
Use highlighting or ratsnest lines to find missing connections.

More Information

Highlighting Nets

To select elements to be displayed in the permanent highlight color, choose **Display > Highlight**. To dehighlight elements that are currently highlighted, use **Display > DeHighlight**.

Viewing Ratsnests

Rats are imaginary lines drawn between the unconnected pins of a net. Use the **Display** command to display or blank (remove from display) ratsnest lines.

To display or blank (remove from display) all rats, or only by component or net, choose **Display > Show Rats** or **Display > Blank Rats**.

When a net contains dangling trace endpoints, the ratsnest lines are drawn to the end of the dangling connection and not to the pins.

Adding Signal Connections

1 Route > Connect *or*

2 Check "active" layer

3 Select start point

4 Click left to enter the projected wire path

5 Click left to continue path to target

6 To exit Connect mode, choose the Done command

Summary

It is very important to check the settings of the **Act**ive and **Alt**ernate layers in the Options Folder tab when adding etch. If the routing does not appear on the etch subclass that you expected, it is probably due to an incorrect **Act**ive layer setting. However, with the Allegro Smart Start feature, this problem is eliminated. If you select on a surface-mount pin, or a piece of etch, and the **Act**ive layer does not match the subclass of the element selected, the **Act**ive layer will be automatically changed to match the selected element.

More Information

To add signal connections, first select **Route > Connect** from the top menu, or use the icon. This puts you into connect mode, ready to add connect-lines (or clines). Clines differ from other graphic lines in that they have signal name intelligence and adhere to design rules for width and spacing.

Next, verify that all settings are correct in the Options and Visibility forms. We will give a detailed description of these settings later in this lesson.

When you are sure that all Options form settings are appropriate, you can begin selecting points, or drawing the line.

Once you have selected a start point, a projected wire path follows your cursor. This is the wire segment or connection that will be added to the design.

Between your cursor and the target pin is a target line that acts as a directional guide that shows you where you must go to complete the connection.

If you turn rats on, a ratsnest line stretches from the start point to the target pin. (This ratsnest line dynamically repositions itself between the wire endpoint and the target pin for each segment that you add.)

Inserting Vias

1 Route > Connect *or*

2 Check "active" layer

3 Add etch on TOP layer

4 Double click to insert a via

5 Add etch on BOTTOM layer

6 Right-click to select menu options

Done
Oops
Cancel
Next
Temp Group
Complete
Reject
Add Via
Finish
Snap Rat T
Neck
New Target
No Target
Swap Layers
Toggle
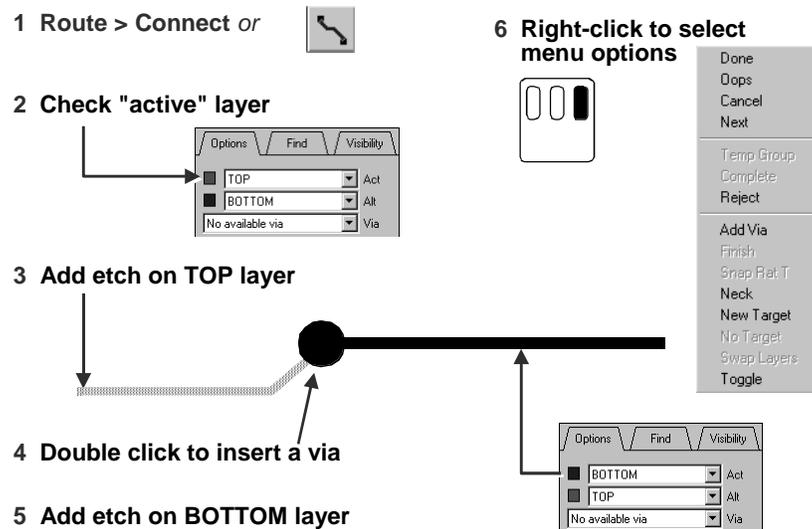
More Information

This section explains how to use the **Connect** option to add vias to a design.

1. Select **Route > Connect** from the top menu. Notice that the Options form changes.

2. Verify all settings in the Options form, and be sure that your desired etch layer is Active.

3. Begin adding the connection by picking vertex points, using the left mouse button in your Allegro work area.

4. To add a via, check the Alternate layer in the Options form (and change if necessary). Then, double click the left mouse button.

5. Notice that the **Act**ive and **Alt**ernate layers have swapped. You can continue adding your connection on the currently active layer.

6. Click right and select **Done** to complete the **Connect** command.

Remember that the via padstack that is used will be the via you defined as the default via in the Physical Constraints form or the Default Rules.

Selecting Via Types
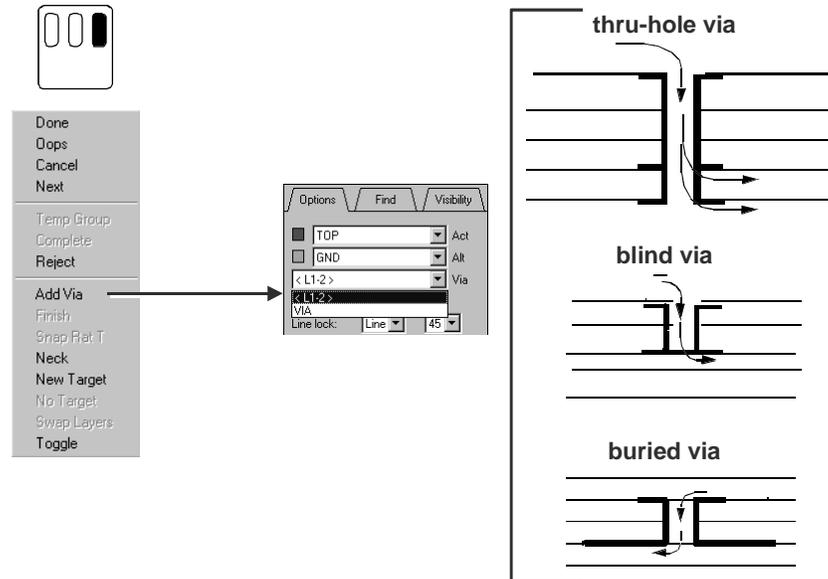
Summary

When adding vias, Allegro attempts to use the most "conservative" via. When using blind and buried vias, this means Allegro will attempt to use the blind or buried via before using a through-hole via. In the case shown, since the Active layer was set to TOP and the Alternate layer was set to GND and there was a buried via defined between these two layers, Allegro will by default select this via. However, you can always override the selected via by selecting in the Via pull-down section and choosing a different via.

More Information

There are two types of vias: through-hole or blind/buried. You can add either type as part of a connection.

A **through-hole** via is a plated hole that passes through all layers of your design. It provides a means of connection from one etch layer to any other. Through-hole vias are the most common. They are easier and cheaper to manufacture than blind or buried vias, but they block routing grid channels on all layers each time one is used.

In order to add vias that differ from the default via padstack you defined, you must add them to the list of available vias in the physical constraint rules.

A **blind** via is a plated hole that starts from an external layer but is not drilled through all layers. This provides a means of connection between an external layer and one or more internal layers. A **buried via** is a plated hole that starts from an internal layer and extends to another internal layer but never reaches the external surface of the fabricated board. Blind and buried vias do not block routing channels on all layers and thus allow more connections to be made on very compact designs. These types of vias require separate drilling files for the various drill stages required by manufacturing, and are therefore more expensive to produce.

In order to use blind or buried vias, you must define the layer pairs by selecting **Setup > Define B/B Via** from the top menu.

Choose from the list of available vias you can use in the Options folder tab.

Pop-Up Menu Options

Before you select a start point

Done
Oops
Cancel
Next
Temp Group
Complete
Reject
Add Via
Finish
Snap Rat T
Neck
New Target
No Target
Swap Layers
Toggle

After you select a start point

Done
Oops
Cancel
Next
Temp Group
Complete
Reject
Add Via
Finish
Snap Rat T
Neck
New Target
No Target
Swap Layers
Toggle

More Information

Immediately after selecting **Route > Connect**, you view a pop-up menu:

Swap Layers interchanges the **Act**ive and **Alt**ernate layers in the Options form.

During the process of adding segments, different options are available:

Done exits the **Route > Connect** command.

Oops lets you undo or take back the last added point in the wire path (can be used to repetitively remove all wire segments and vias for the current connection).

Cancel cancels all selections and exits from the command.

Next lets you start on a new connection without exiting from connect mode.

Reject applies if multiple objects are stacked on top of each other. It lets you reject a currently selected object and select another object from a window.

Add Via is used to add through-hole, blind, or buried routing vias.

Finish completes the connection using an automatic router. This routing is performed on the active layer only. No autorouting licensing is needed for this feature.

Snap Rat T enables you to move a Rat T connection to the last pick. Note that this option is not available with PCB Studio.

Neck means that the next segment will neck down and ensures the segment complies to the Physical Rule Set for the Minimum Neck Width and Length constraints.

New Target lets you select a new rubberband target pin (defaults to closest pin).

No Target eliminates the rubberband line from the cursor to the target pin.

Toggle lets you switch the initial direction of the projected wire path.

Options Form
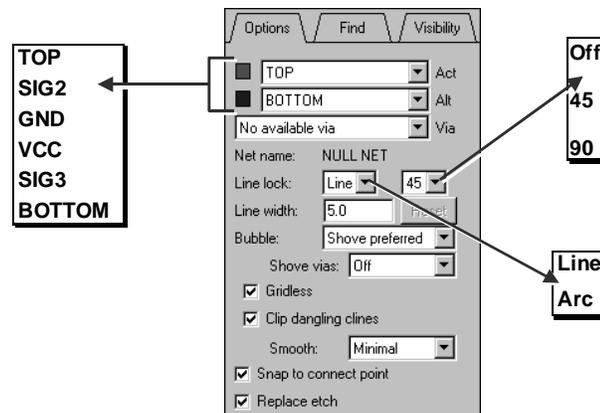
More Information

When you select **Route > Connect**, the Options form changes. You can change the data in most fields by moving the cursor into the field and pressing the left mouse button. The diagram shows the choices available through the various pop-up menus.

Act and Alt

The **Act**ive and **Alt**ernate subclass fields determine which layer will be used for the current connection. The **Act**ive and **Alt**ernate layers are interchanged if you select **Swap** or add a via. Remember, when selecting a surface-mount pin or a piece of existing etch, the **Act**ive layer will automatically switch to the appropriate subclass.

Line Lock

These settings control the type of line, either **Line** or **Arc**, and the angles allowed for turns. Off implies that "any-angle routing" is allowed.

Line Width

The line width value is based on the Design Rules. When you select a pin for routing, the Allegro program recognizes the net, and automatically loads the Net Name field and required line size into the Options form. You can also type a value into this field. If you type in a value, the **Reset** button becomes available which, when selected, will change the value back to what Allegro determines should be the width.

Options Form—Smooth
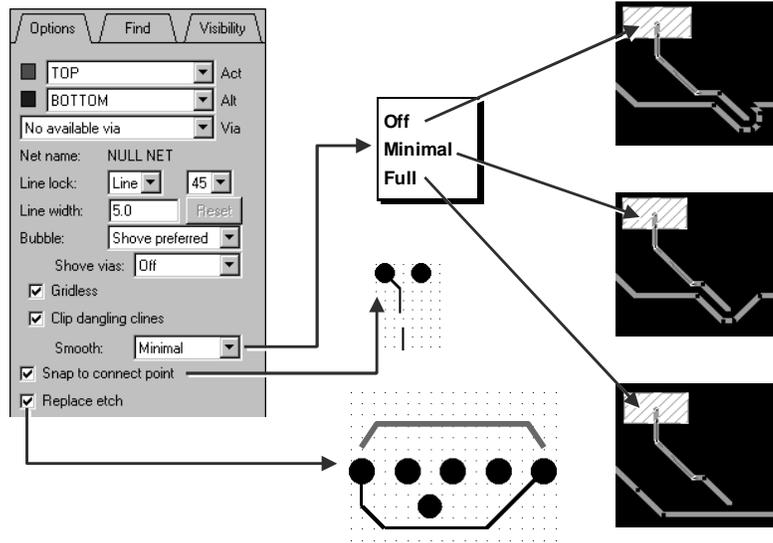
More Information

Smooth

> This feature automatically smooths or cleans routing as it is being added. This is required, since the interactive router performs real-time push and shove of existing etch. Smooth is only available if Hug Preferred or Shove Preferred is enabled. The Smooth option offers three choices:

> **Off** means this feature is disabled. Existing etch affected by the current route may end up with undesirable angles and bubbles. Using this option is a method for creating shielded etch.

> **Minimal** will eliminate only a few short and/or extra segments.

> **Full** will eliminate more segments similar to the Custom Smooth command.

Snap to Connect

> This option lets you connect to the center of off-grid pads, vias, or dangling endpoint etch.

Replace Etch

> Replace Etch lets you change the path of an existing trace, without extra delete and add steps. When you add a loop into an existing trace, the older portion of the loop is recognized and automatically deleted.

Options Form—Bubble/Gridless

gridded

gridless

Off

Hug preferred

Shove
preferred

Off
Hug Preferred
Shove Preferred
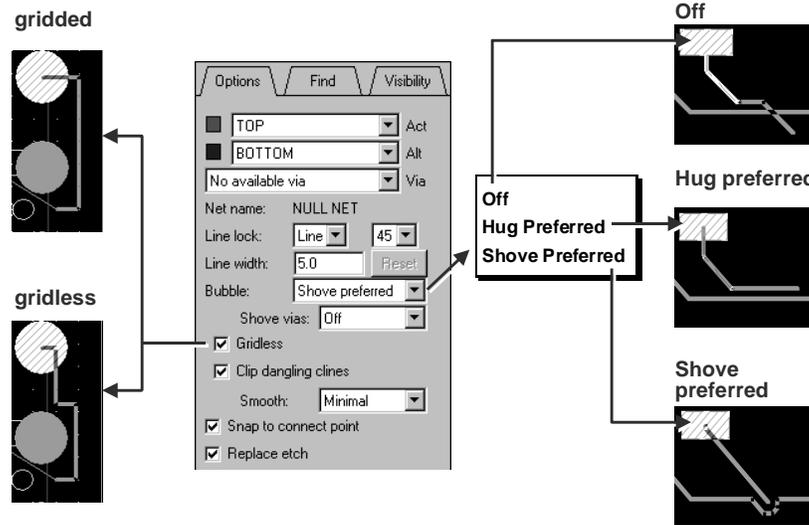
More Information

Bubble

> The Bubble field provides three choices:

>> **Off** means the route follows your cursor picks in the x and y direction absolutely. It does exactly what you ask it to, regardless of potential DRC errors.

>> **Hug Preferred** means the new route hugs around existing etch objects. The existing objects are not modified.

>> **Shove Preferred** means other etch objects are shoved and moved out of the way, if possible, to correct for spacing violations.

Gridless

> This feature determines whether the added etch is snapped to the routing grid or not. Gridless is only available if Hug Preferred or Shove Preferred is enabled. This option offers two choices:

>> **Off** pushes etch to the next available free grid.

>> **On** pushes etch away from pads and vias just enough to reach a legal minimum DRC clearance.

Labs

◆ Lab: Defining Etch Grids

■ Define and display a grid suitable for adding traces.

◆ Lab: Adding and Deleting Connect Lines and Vias

■ Learn how to add and complete a signal connection.

● Add a connect line (cline).

● Delete etch.

● Insert vias.

● Use the bubble option.

More Information

The following lab will allow you to:

■ Familiarize yourself with the process and steps required to set the interactive routing grid.

■ Familiarize yourself with the process and steps required to interactively add routing and vias. You will also learn how to delete routing and vias.

Lab 10-1:   Defining Etch Grids

Objective: Define and display a grid suitable for adding traces.

In this lab you will edit the Grids Display form to define etch grids.

1. Start Allegro if you don't already have it running, and open *placed.brd* if it is not the current design.

2. If required, resize Allegro to fit your screen.

3. Choose **Setup > Grids** from the top menu.

    The Grids Display form appears.

    You will change the x and y spacing values for all routing layers.

4. Check the **Grids On** option in the upper left corner of the form and make sure that it is toggled ON.

5. Scroll the form to examine the entire list of etch layers, then return to the top of the displayed list.

Note

Before you proceed to the next step, please note: To advance to the next field in any Allegro menu, use the **Tab** key. DO NOT press the **Enter** key to advance fields. The **Enter** key has the same result as clicking the **OK** button, closing and executing the form.

6. Locate the section marked **All Etch** in the column labeled Layer, and set the X and Y values as shown in the figure: Make sure the values you type are separated by spaces:

All Etch	Spacing:	x:	5
		y:	5
	Offset:	x:		y:	

The settings automatically change for all other etch layers.

7. Click **OK** at the bottom of the Grids Display form.

    Depending on your last active command, the Allegro work area window may or may not display the 5-mil grid pattern.

8. In order to ensure that the Etch grid is being displayed, you must activate a routing command. Click the **Add Connect** icon (same as choosing the **Route > Connect** menu item).

The Etch grid displays.

Note

If you had set the grid to alternating 8-, 9-, 8-mil intervals instead of a straight 5 mils, you would see a distinct repeating grid pattern display, showing a larger dot every 25 mils, with smaller dots at 8-, 9-, 8-mil intervals.

9. Right click and choose **Cancel** from the pop-up menu.

End of Lab

Lab 10-2: Adding and Deleting Connect Lines and Vias

Objective: Learn how to add and complete a signal connection.

Later in the labs, you will use the SPECCTRA autorouter to route the design. When adding the routes manually, keep in mind that by default SPECCTRA routes the TOP layer mainly in a horizontal direction, and the BOTTOM layer mainly in a vertical direction.

In this lab you will be manually routing portions of the MCLK net.

Adding a Connect Line

1. Click the **Zoom Fit** icon to fit the entire design in your view.

2. If ratsnests are currently displayed, choose **Display > Blank Rats > All** from the top menu to turn off all ratsnests.

3. Choose **Display > Show Rats > Net** from the top menu.

4. Click the **Find** tab to bring the Find Filter to the front.

5. In the Find By Name section, select **NET** from the Find By Name drop-down menu.

6. In the value field, enter the following net name:

    mclk

    The ratsnest line for the MCLK signal is displayed.

7. Either use the "Z" stroke or choose **View > Zoom by Points** to zoom in on the connector J1, which has one connection on the MCLK net if the display has not been automatically zoomed around the MCLK net.

    ### 🗒 Note

    To use the "Z" stroke, press the **Ctrl** key and click and drag with the right mouse button.

8. Look at the ratsnest for the **MCLK** net. Click the **Add Connect** icon.

    The Find Filter and the Options forms change. Notice the Options form. Before you select a pin to start from, all settings should match the following illustration:

9. Click on the pin of the J1 connector, which is the endpoint of the MCLK ratsnest line.

Since the TOP layer is active and the pin is a through-hole pin, you are adding a connection on the top layer of the board. If this were a surface-mount pin, the connection would be added to the layer on which the pin was defined.

After you select the start point, you see a ratsnest line stretching from the cursor to the nearest destination pin. As you move your cursor, the route appears.

Notice also that the net name and the correct line width for MCLK are now displayed in the Options form.

10. Continue to click points for the line until you reach the destination pin. You can make your trace look similar to the figure:
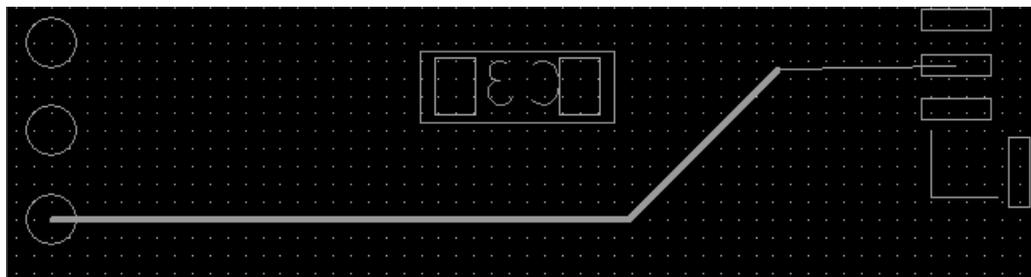
If you make mistakes while picking points, back up, right click and choose the **Oops** option.

When you reach the destination pin, the ratsnest line disappears, denoting the completion of that connection.

If the destination pin is on the bottom side of the board, you need to add a via in order to connect to the pin. Since you will learn to add vias later, stop routing at a point close to the destination pin.

11. Right click and choose **Done** from the pop-up menu.

Deleting Etch

The Allegro program provides several ways to delete etch lines. You can delete lines, segments of lines, and sections within segments. Be sure that you set the Find Filter and Options forms so that only the desired items are deleted.

1. Click on the **Delete** icon in the toolbar.

The Options form and the Find Filter change.

Note

Default settings in the Find Filter may show all items toggled ON. This can be dangerous while in delete mode. As a general rule, you should turn all items OFF, then select only the items you want to delete.

2. Click the **Find** tab to bring the Find Filter to the front if it is not visible.

3. Click the **All Off** button in the Find Filter.

4. Check the **Clines** box to ON in the Find Filter.

5. Click on the **MCLK** net.

The connection becomes highlighted.

6. Right click and choose **Done** from the pop-up menu.

The previous etch you added disappears. Using Clines in the Find Filter lets you delete the entire connect line (all segments from pin to pin).

7. Click the **Add Connect** icon to add the connection back in, the same as you did in the previous part of this lab.

8. Click on the **Delete** icon in the top menu.

9. In the Find Filter, set the check box options as follows:

    a. Toggle **Clines** OFF.

    b. Toggle **Cline Segs** ON.

10. Click on the **MCLK** net.

A segment becomes highlighted.

You can delete individual segments of a connect line by using Cline Segs in the Find Filter.

11. Click another segment.

The first segment disappears. The ratsnest line reappears because the pin-to-pin connection has been broken.

12. If any segments of the MCLK signal still remain, delete them.

13. Right click and choose **Done** from the pop-up menu.

Note

You can delete lines, segments, vias and shapes individually, in groups, or by selection window using other Options, Find Filter, and pop-up menu choices. While in **Delete** mode, be careful when changing these settings to avoid "unexpected" results.

Inserting vias

1. Click the **Add Connect** icon in the toolbar.

2. If necessary, click the tab for the **Options** form to bring it forward.

3. In the Options form, Set the active and alternate layers as shown in the figure:
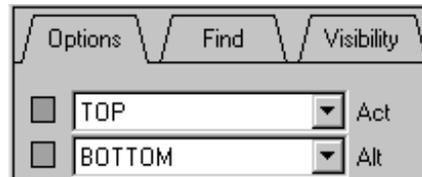

4. Click on the pin of the MCLK net in the **J1** connector, the pin connected to one end of the ratsnest.

5. Once again, begin adding segments from that pin toward its destination.

6. When you have reached a point where you would like to add a via, double click with the left mouse button. See the figure.

Add a via here
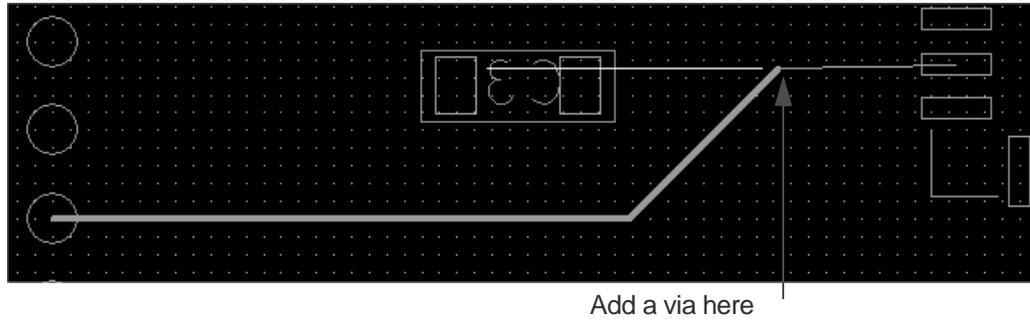
You have just added a via, and the Active and Alternate layers in the Options form have been swapped. You are now adding on the BOTTOM layer.

7. Finish the connection all the way to the pin of the **U5** component.

Since the destination pin is on a surface-mount device on the top side of the design, you will need to add another via to finish the route on the TOP layer. However, you can't add the via under the pad, so you have to put it a little to the left of the pad. See the figure.

Add a via here   ..and another one here
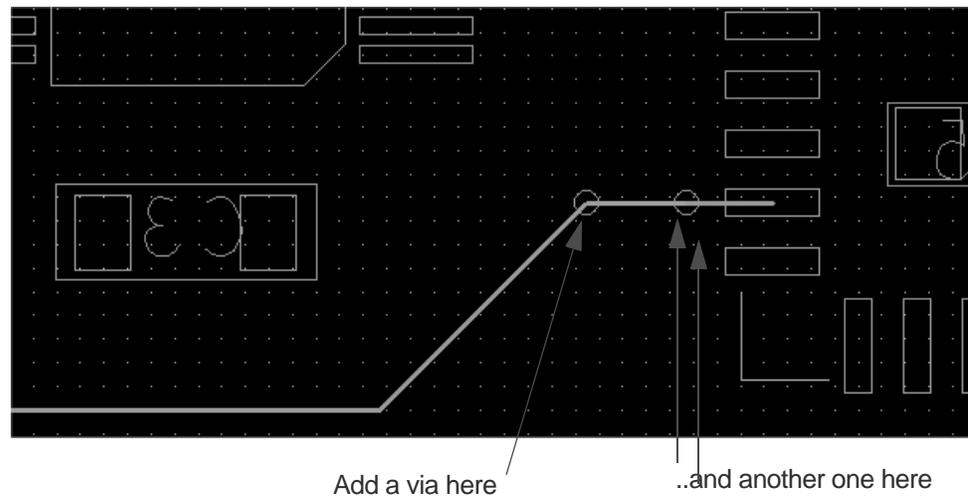
8. Right click and choose **Done** from the pop-up menu.

Look at how the connection you just added uses two different etch layers and routing vias. Sometimes using a via to go from TOP to BOTTOM, then from BOTTOM to TOP again, is referred to as *stitching* because of the similarity to sewing.

Using the Bubble Options

1. Click the **Add Connect** icon in the top menu.

    The Find Filter and the Options forms change.

2. Move the cursor into the Bubble field of the Options form. Select **Shove Preferred** in the drop-down list if this option is not already selected. Under Smooth, set the option to **Full**.

3. Click the **Rats All** icon to turn on all ratsnests. Zoom into an area to view one end of a ratsnest on the pin just below the MCLK pin of the **J1** connector, and the other ratsnest connection on the **U5** component in view. See the figure.

Note

Your view may differ slightly, depending on how your components are placed.
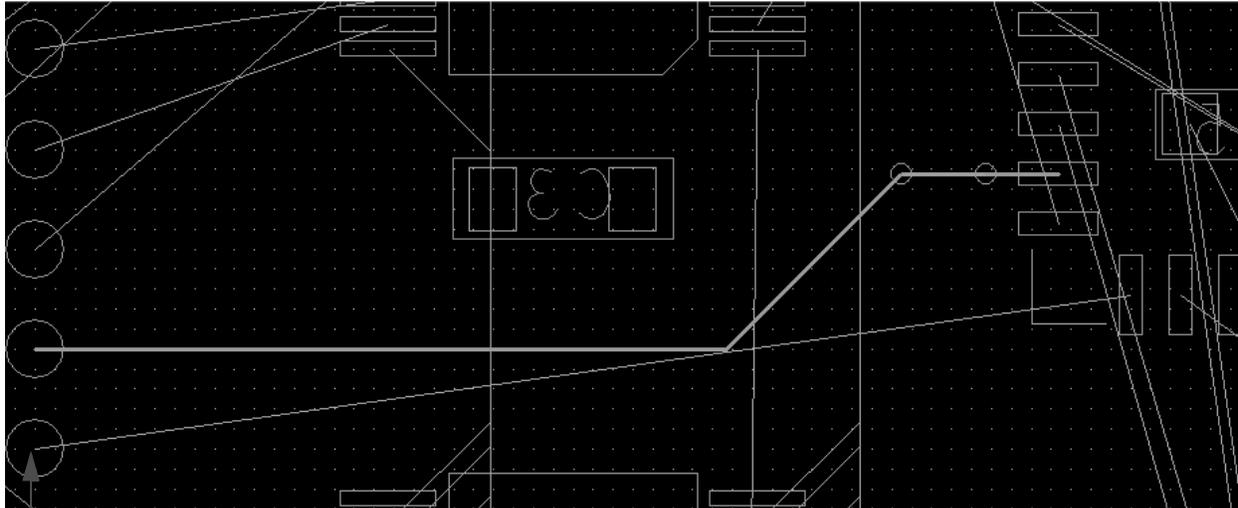
Start a new etch path here.

4. Click on the pin just below the MLK pin of the **J1** connector. This is the WAIT net. See figure above.

    Make sure the active layer is set to TOP.

5. Start moving your cursor toward the existing etch of the MCLK net. The existing etch will be "shoved", or moved, as the new etch becomes closer than the DRC "line to line" value.

6. Experiment with the different Smooth options of Off, Minimal and Full that are available in the Options folder tab, and with the different Bubble options of Off and Hug Preferred. Also experiment with the Shove vias option.

Note

While you are in this mode, there may be some instances when the trace to be added will create a DRC. When this happens, your cursor will appear as a DRC marker.

Shove preferred, Minimal
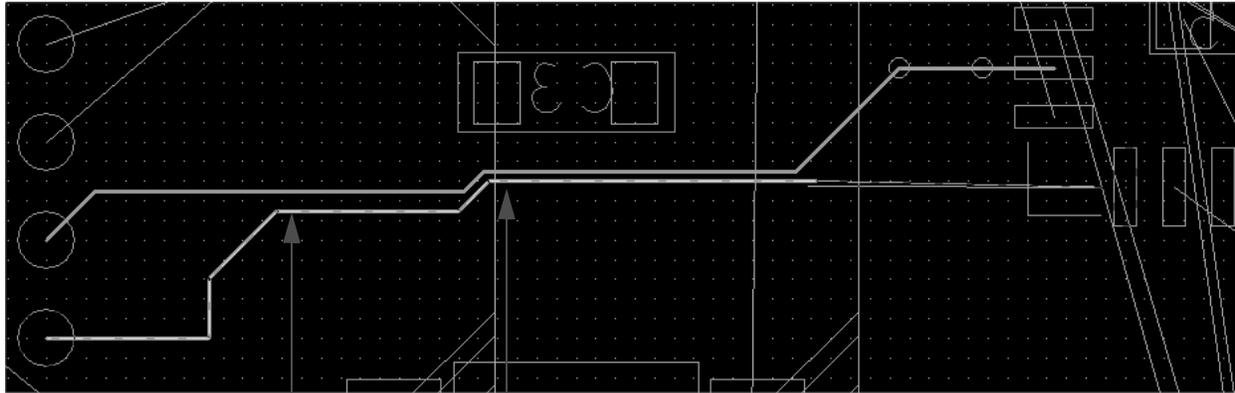
Shove preferred, Full

7. Finish routing the WAIT net.

8. Right click and choose **Done** from the pop-up menu.

9. Choose **File > Save As** from the top menu.

A browser form appears.

10. In the File Name field, enter:

routed

11. Choose **Save**.

The file *routed.brd* has been saved to disk. Throughout the remainder of this lesson you will be writing over the *routed.brd* file.

STOP End of Lab

Accessing the SPECCTRA Router

SPECCTRA interface ————————→

File > Export > SPECCTRA

File > Import > SPECCTRA

More Information

Shown are three ways to access SPECCTRA.

1. The SPECCTRA interface icon is found in the top of the Allegro window.

2. You can select **File > Export > SPECCTRA** to generate a *.dsn* file from Allegro.

3. You can select **File > Import > SPECCTRA** to read a session or routes file into Allegro.

Autoroute Prerequisites

◆ A netlist is loaded to give conductor intelligence
  ▪ A partial netlist is acceptable
◆ Placement reflects the arrangement logic
  ▪ A partial placement is acceptable
◆ A user-defined route keepin
  ▪ This is **mandatory!**

More Information

Autorouting normally occurs after placement is complete and you have made some minor preparations, such as the addition of critical nets. You have defined constraints by this point, as well as any route-related properties.

Autorouting can be carried out with either a complete or a partial netlist and a complete or partial placement. The Allegro tool will attempt to connect any nets belonging to placed components in your design.

You SHOULD define a Route Keepin in the design. Define the keepin area through a board symbol, or add it directly to the design. If no Route Keepin is defined, the SPECCTRA translator will make the routing area in SPECCTRA match the entire drawing extents.

Preparing for Automatic Routing

- ◆ Check/define etch grids if required.

- ◆ Check/define cross section (layer stackup).

- ◆ Check/define appropriate constraints and properties.

- ◆ Check for NO_RIPUP, NOROUTE, FIXED, and NO_GLOSS properties.

- ◆ Define internal plane layers as negative in the cross section (layer stackup).

- ◆ **Save** your design before starting any automatic routing.

More Information

You should always complete a check of the conditions and parameters set in your design before committing to an execution of any autorouters. Perform the following actions:

■ Define Cross Section (layer stackup). You might want to add routing layers prior to automatic routing.

■ Define appropriate Constraints and Properties. Check constraint rules and routing-related properties (discussed in more detail later in this chapter).

■ Check existing etch for NO_RIPUP, NOROUTE, FIXED, and NO_GLOSS properties, and add these properties if needed.

■ Internal plane layers need to be defined as negative. The SPIF translator and the router will take a long time to process the plane if you treat it as a positive at this point. If you have a split plane on a layer, now is the time to define that as a negative.

■ It is important to SAVE your work up until this point so you won't lose all the settings that you have added thus far.

The Allegro-SPECCTRA Process

SPECCTRA interface

route.dsn

route.ses

route.brd

route.brd
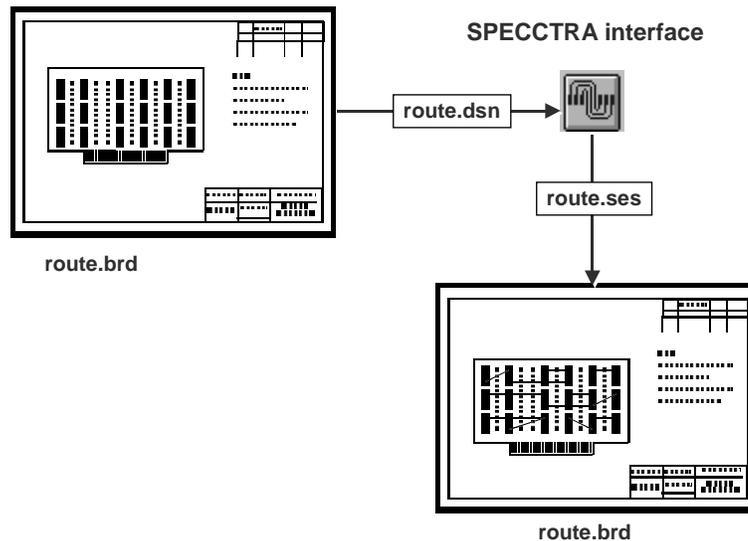
More Information

When you click the SPECCTRA icon, Allegro writes a filename.dsn (design file) that SPECCTRA uses as input. The SPECCTRA user interface then starts automatically.

After selecting parameters or importing custom parameters (.do files), you can start SPECCTRA routing from the SPECCTRA user interface.

When routing is complete, you are prompted to write a filename.ses (session file) that can be imported into Allegro. If you used the SPECCTRA interface icon to start this process, the Allegro software will expect to import a file with a similar name. For example, if you started with an Allegro file named *route.brd*, the SPECCTRA interface would create a *route.dsn* file and expect to read back a *route.ses* file after routing.

Upon quitting from the SPECCTRA interface you are returned to the Allegro Editor, and connections are updated automatically.

Labs

◆ Lab: Preparing for Autorouting
  ■ Create embedded power planes.
    ● Make the plane layers visible.
    ● Create the shape for the VCC power layer.
    ● Assign the VCC net to the new shape.
    ● Copy the VCC shape to the GND ground layer and assigning the GND net.
    ● Save your work.
◆ Lab: Using the SPECCTRA Autorouter
  ■ Complete all net connections with SPECCTRA.
    ● Preserve pre-routes into SPECCTRA.
    ● Run the SPECCTRA router.

More Information

The following labs will allow you to familiarize yourself with the process and steps required to create temporary planes. You will learn how to create a plane, assign a net name to the plane, and finish the plane. It is important to have all planes created before transferring to SPECCTRA so the autorouter can recognize the power/ground nets for pin-escaping. You will also become familiar with the process and steps required to do a simple route using the SPECCTRA autorouter.

Lab 10-3:   Preparing for Autorouting

Objective: Create preliminary embedded power planes.

At this stage of the design process it is advisable to check the following items before committing your design to any autorouter:

- Check/define etch grids (if gridded routing is to be used).
- Check/define cross section (layer stackup).
- Check/define appropriate constraints and properties.
- Check for NO_RIPUP, FIXED, and NO_GLOSS properties.
- Add preliminary embedded planes if VCC and GND connections are to be autorouted.

In order for the SPECCTRA router to add VCC and GND connections, these planes must exist prior to routing. You will add embedded *negative* planes in the following steps. (Embedded planes are discussed in further detail later.)

Making the Plane Layers Visible

1. Start Allegro if the software is not already running, and open the *routed.brd* file.

2. In the Control Panel, activate the **Visibility** tab.

3. Set the check box options to match the figure by first checking the **Planes** option, then checking **All** for Planes and making sure only **GND** and **VCC** are checked:
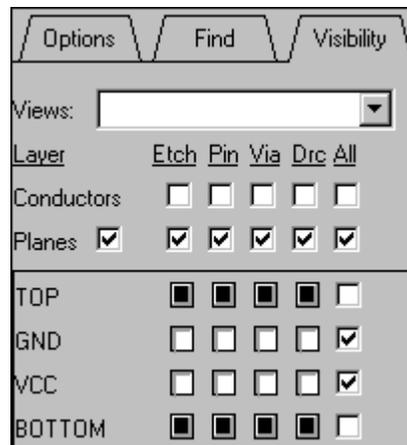
4. Choose **Display > Color/Visibility** from the top menu.

5. Select the **Stack-Up** group and set the color for Pin/Via/Etch to green for the GND subclass and set the color for Pin/Via/Etch to red for the VCC subclass.

6. Select the **Areas** group from the drop-down list.

7. Toggle the **Route KI** (Route keepin) class to ON.

8. Click **OK** to confirm your settings.

   The Color and Visibility form closes.

Creating the Shape for the VCC Power Layer

1. Choose **Add > Shapes > Solid Fill** from the main menu.

2. In the Options form, set the Active Class to **ETCH** and the Active Subclass to **VCC**.

   Next you will define a polygon.

3. Zoom into the upper left area of the board, with enough magnification that you can clearly distinguish the board outline and the route keepin.

4. Begin laying down a polygon, 10 mils inside the border of the route keepin. Use the zoom and pan commands to maintain your view so you can see where the polygon vertices are being placed.

   If you make a mistake, you can back up vertex-by-vertex by choosing the **Oops** command from the pop-up menu. You can also use the **Edit > Vertex, Edit > Delete Vertex, and Edit > Boundary** commands to change a vertex location. See the figure for an example of how your polygon might look. Make sure your starting point and ending point are the same so the shape is a closed polygon. Once you have completed your shape outline, you change into the "Edit Shape" mode (this will be discussed later)

Route keepin

Board outline   Polygon shape offset by 10 mils
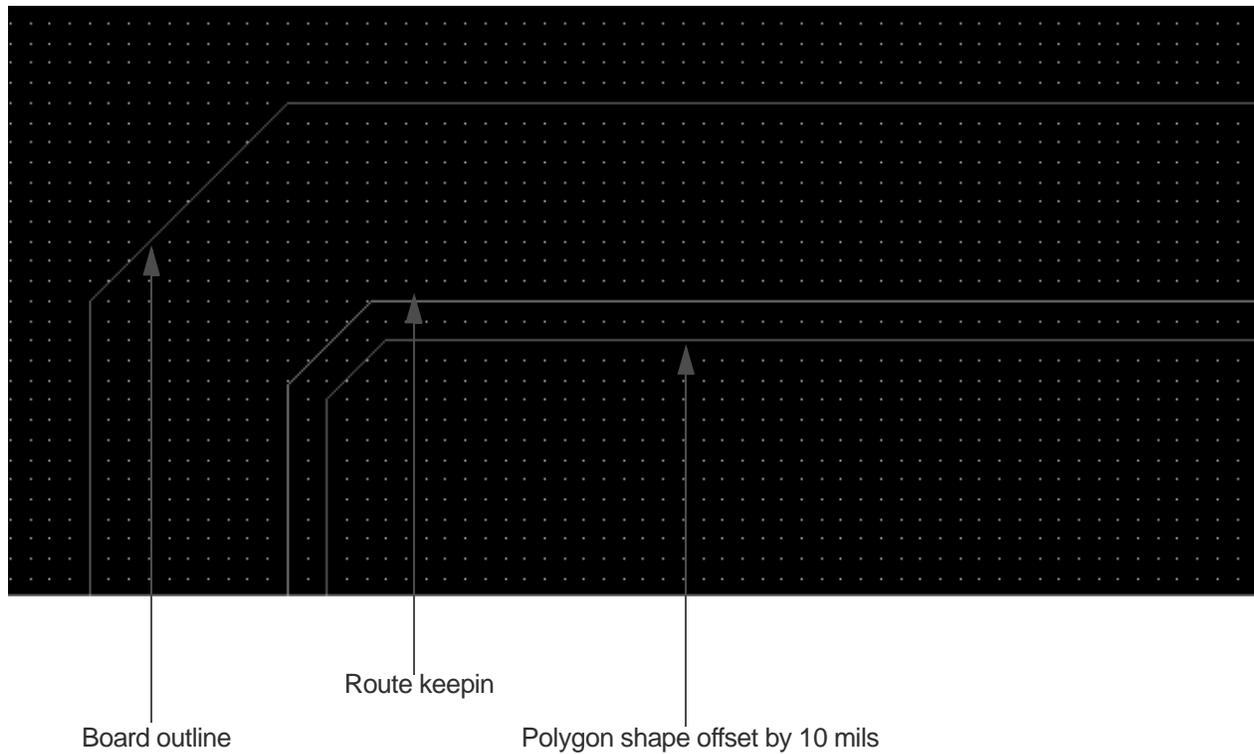
Assigning the VCC Net to the New Shape

1. Choose **Edit > Change Net (Name)** from the main menu.

   A browser window opens, displaying all the nets in the design.

2. Scroll the list, select **VCC**, and click **OK**
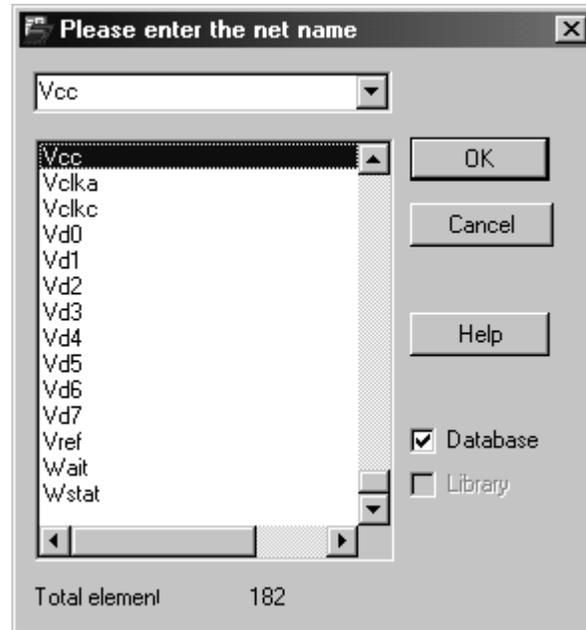
The shape you are editing is now attached to the VCC net. The Allegro message area reports that the shape moved from the null set to VCC.

3. To fill in this polygon, choose **Shape > Fill**.

   The polygon you just created is filled in with the color you have assigned in the Stack-Up group for VCC.

Creating the Shape for the GND Ground Layer and Assigning the GND Net

Next you will create the GND plane. These steps will show you how to use the Z Copy command. This is an alternative method to creating a shape by manually "drawing in" the outline.

1. Select **Edit > Z-Copy** from the main menu.

2. Change the Subclass to **GND**.

   Change the offset to 0.00 if required.

3. Select on the **VCC** shape.

   The VCC shape is copied to the GND layer. The outline matches exactly what you entered for the VCC shape

4. Select **Done** from the right mouse button pop-up menu.

5. Using the Visibility folder tab, turn off the VCC layer.

6. Select **Edit > Shape** from the main menu.

7. Select the **GND** shape.

   The GND shape highlights.

8. Select **Done** from the right mouse button pop-up menu.

    The GND shape becomes "unfilled".

9. Choose **Edit > Change Net (Name)** from the main menu.

    A browser window opens, displaying all the nets in the design.

10. Scroll the list, select **GND**, and click **OK**

11. To fill in this polygon, choose **Shape > Fill**.

Saving Your Work

1. Choose **File > Save** from the top menu.

    A window appears and warns you that the *routed.brd* file already exists. It asks if you want to overwrite the file.

2. Click **Yes** to confirm the overwrite.

    The *routed.brd* file is saved to disk.

STOP **End of Lab**

Lab 10-4:   Using the SPECCTRA Autorouter

Objective: Complete all net connections with SPECCTRA.

In this lab you will use the SPECCTRA router and the SPECCTRA interface that is built into Allegro software.

Preserving Pre-Routes into SPECCTRA

By default, all routing that exists in the Allegro design gets "protected" when transferred into SPECCTRA. This means that the SPECCTRA router cannot move any of the transferred routing. Therefore, if you want to keep any of your existing routes, you need to make sure your routing "matches" the route in SPECCTRA.

By default, the routing directions in SPECCTRA are TOP as a horizontal routing layer, and BOTTOM as a vertical routing layer. Make sure your routing matches these layer directions.

1. Open the *routed.brd* file if it is not already opened.

2. Using the Visibility folder tab, make visible only the **TOP** and **BOTTOM** layers.

3. If you want the SPECCTRA router to route the entire design, delete *all* of the existing etch you might have created, especially the routes for the MCLK and WAIT nets. Use the techniques you learned earlier to delete all of the current Clines/Vias.

## Running the SPECCTRA Router

1. Click the **SPECCTRA** icon that you did not previously add into your menu bar. This is the icon with the gray background, not the blue background.

    The SPECCTRA Automatic Router dialog box appears.

2. Set your options to match those in the figure below. You can leave the settings in the Routing Passes, Smart Router, and Selections tabs as they are.
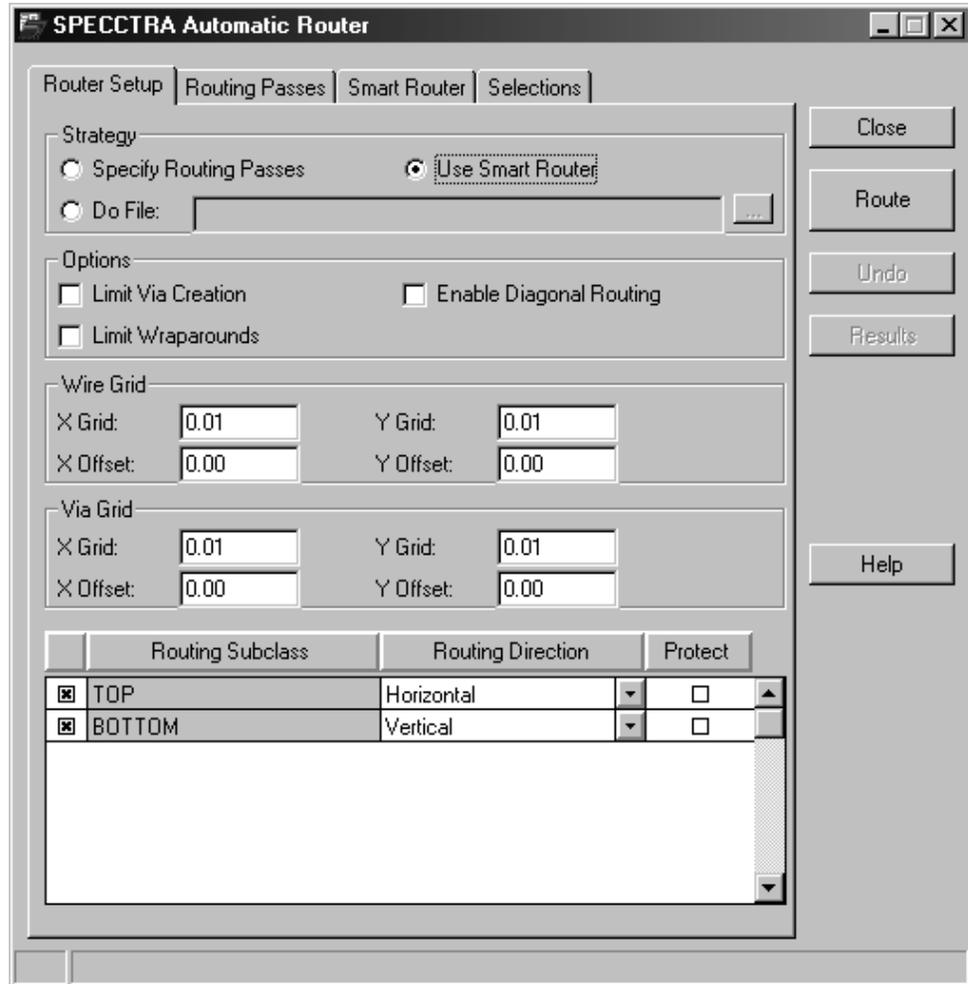
3. Click **Route** to begin routing.

    The SPECCTRA routing begins. Your current board design is being written into a SPECCTRA format *.dsn* file. During routing, you see the SPECCTRA Automatic Router Progress report.
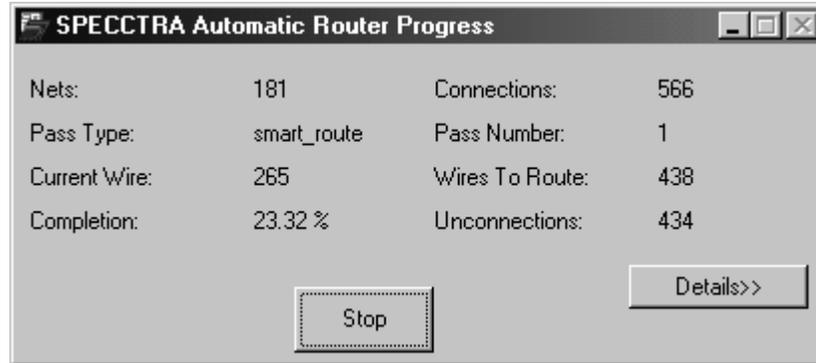
If you want to discontinue routing you can click **Stop**. If you would like to view details about the routing passes, such as the total number of crossovers or how many vias are in place, then click **Details**.

4. When autorouting is complete, click **Close** in the SPECCTRA Automatic Router dialog box.

   The SPECCTRA results are read into the Allegro design.

5. In Allegro, choose **File > Save** from the top menu.

   A window appears and warns you that the *routed.brd* file already exists. It asks if you want to overwrite the file.

6. Click **Yes** to confirm the overwrite.

   The *routed.brd* file is saved to disk.

STOP **End of Lab**

Editing Existing Etch

◆ Sliding connections and vias

◆ Editing vertices

◆ Moving a connection to another layer

◆ Deleting connections

More Information

This section explains various editing options available while in **Edit Etch** mode. The Options form plays a very important role during etch editing. The Options form changes to match different types of editing needs and is an integral part of editing control.

◆ Moving etch lines with the **Slide** option results in etch that conforms to current Options settings. Another way to change the path of existing etch is to use the **Replace Etch** option within the **Route Connect** command.

◆ Creating or moving vertices of existing etch is a fast method of moving etch segments. The number of jogs in an etch connection can also be reduced by deleting vertices.

◆ You change the layer of an etch line by designating the new layer in the Options form.

◆ Deleting etch lines and vias is also controlled to a large extent by selections in the Options form.

Moving Etch with the Slide Option
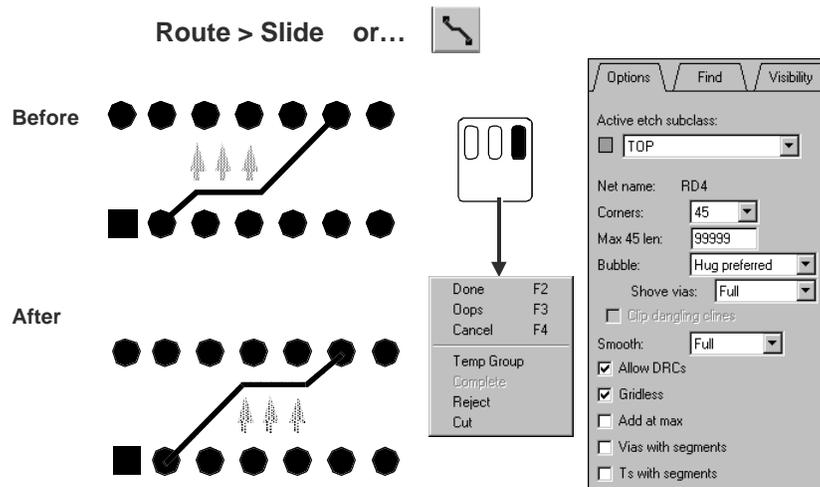
More Information

Slide lets you move a connection with or without moving associated vias. The moved segments do not become disconnected. Follow these steps to slide a segment of etch:

1. Select the **Slide** command on the top menu.

2. Pick the etch line with the left mouse button, and drag the line in the desired direction.

3. Position the line and press the left mouse button once more.

   Settings in the Options form affect the resulting etch:

   - **Corners**: 45, 90, or Arc

   - **Max 45 Len**: You type in the desired length for diagonals

   - **Bubble**: Shove Preferred, Hug Preferred, or Off. The same rules apply as to the **Route Connect** command

   - **Shove Vias**: There are three options to specify the effect of moving existing etch "into" an existing Via:

     - **Off**: Existing Vias are not moved. The shoved etch is moved around the via

     - **Minimal**: Vias are moved only if there is no way to draw a connect line around them

     - **Full**: Vias are always shoved out of the way

   - **Smooth**: Full, Minimal or Off. These options work the same as in the **Route Connect** command

   - **Gridless**: Options are On or Off. These options work the same as in the **Route Connect** command

   - **Allow DRCs**: When turned on, allows DRCs

- **Add at Max**: Do/Do not limit the length of diagonals
- **Vias w/Segs**: Allow/disallow vias to slide with etch segments

Note

Use the **Slide** command in conjunction with the **Cut** option to move a section within a single segment. The **Cut** option is available using the right mouse button pop-up.

Editing Vertices

Use *Vertex* to move vertices.
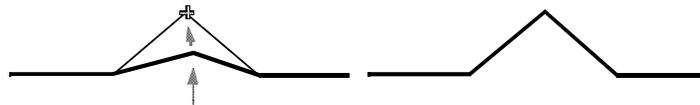
Use *Vertex* to add new vertices.

Right-click and select *Delete Vertex* to remove existing vertices.

More Information

A vertex in an etch line is a point at which the line changes direction or creates a corner. Move and change these corners by selecting **Edit > Vertex** from the top menu. While you are in this mode, a pop-up menu is available that lets you access the **Delete Vertex** command. You can perform the following operations with the **Edit > Vertex** command:

- Move Vertices
- Add New Vertices
- Delete Existing Vertices

Changing the Layer or Width of a Connection

Edit > Change

More Information

Use the **Edit > Change** command from the top menu to change the layer of an existing connect line. The Options form changes. By pressing the left mouse button while the cursor is in the New Subclass field of the Options form, you can choose from a menu of all available etch layers in your design.

When you select any visible connect line in your work area, it immediately changes to the layer that you designated in the New Subclass field.

Note

Vias are added or deleted automatically if the layer change dictates a need for vias.

You can also use the **Edit > Change** command and associated Options form to change the width of an existing connect line.

To change line width, select **Edit > Change** from the top menu. Type a new value in the Line Width field of the Options form and select any visible connect line in your work area. It immediately changes to the width that you designated in the Line Width field.

Deleting Etch

Edit > Delete   or…

Multiple layer ripup (used with Clines)
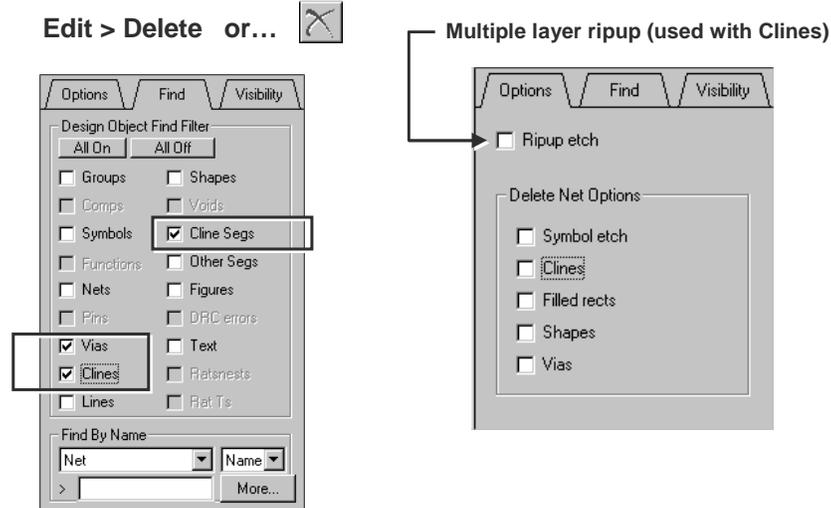
More Information

To delete etch lines and vias:

Select **Edit > Delete** from the top menu. The Find Filter and the Options forms change. Turn all items in the Find Filter **Off**, then toggle **On** only the items you want to delete. Most often this would include Clines or Cline Segs and Vias. Select the desired options in the Options form next and specify which types of etch you want to delete.

By manipulating the Find Filter and the Options form, you can define which portions of a net to delete. You can choose the following combinations:

Use **Cline Segs** to delete a single segment of a net.

Use **Clines** to delete all segments, excluding vias.

Use **Vias** to delete vias.

Use **Clines** and **Ripup Etch** to delete all segments and vias between pins (multiple layer ripup).

Use **Nets** (and **Delete Net** Options—**Delete Clines** and **Delete Vias**) to perform a multiple layer ripup for all pins in a net.

Optionally, you can use the pop-up menu available during the Delete-Etch process to **Group** several pieces of etch or select a window area to delete. You can use the **Cut** option from the pop-up menu to delete a section out of a single segment.

Select **Done** from the pop-up menu to complete the deletion process.

Using the Cut Option

Edit > Delete

Route > Slide

Edit > Change (width)
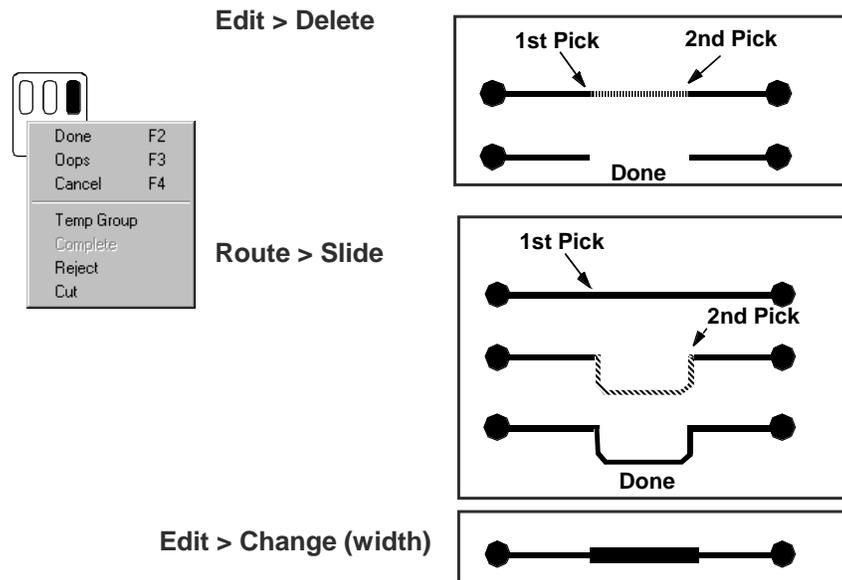
More Information

You can use the **Cut** option to edit specific sections within line segments. Use the **Cut** option with the **Delete**, **Slide**, and **Change** commands.

Access the **Cut** option through a pop-up menu available in all three of these commands. By selecting the **Cut** option with the right mouse button you can define a start and end point within a single line segment. Once you define this section of line, you can delete, slide, or change its width, depending on which command you started with.

Interactive Routing Properties

- ◆ Net properties affect not only autorouter actions but also DRC checking while in interactive route mode.
- ◆ Define net properties before adding etch.
- ◆ Common net properties used with interactive route are:
  - ■ MIN_LINE_WIDTH
  - ■ MIN_NECK_WIDTH
  - ■ NO_RAT
  - ■ FIXED

More Information

You should attach most net properties prior to routing. Attaching correct properties to certain nets can facilitate online DRC checking while you edit etch.

The **MIN_LINE_WIDTH** and **MIN_NECK_WIDTH** properties determine default trace widths for specific signals (default DRC Mode = Always).

The **NO_RAT** property prevents the display of ratsnest lines. This is useful in keeping VCC and GND signals from cluttering the display with ratsnest lines.

The **FIXED** property can be attached to nets immediately after adding etch. This property prevents future modification.

To attach any of these properties, use the procedures discussed in the lesson titled *Setting Design Constraints*. Find out more about properties by from **Programs > Cadence PSD 14.2 > Online Documentation**. Select Allegro, then PCB Systems Properties Reference.

Labs

◆ Lab: Checking for Unconnected Pins
  ■ Confirm whether you have completed all connections.
    ● Using rats.
    ● Using the Report command.
    ● Final editing before gloss.

◆ Lab: Improving Routed Connections
  ■ Learn how to improve etch paths using the Slide function, the Replace Etch function, and other techniques for adding, deleting, and moving vertex points on existing etch.
    ● Using Slide.
    ● Moving, creating, and deleting vertices.

◆ Lab: Replacing Etch and Using the Cut Option
  ■ Learn how to replace segments of etch and use the Cut option in conjunction with other editing commands.
    ● Using the Replace Etch option.
    ● Using Cut with Delete.
    ● Using Cut with Slide.
    ●

More Information

The following labs will allow you to familiarize yourself with the process and steps required to:

■ Check for unconnected pins. You will use both ratsnests and the **Report** command in this exercise.

■ Familiarize yourself with the process and steps required to update existing etch in your design. You will use both the **Slide** command and **Edit Vertex**.

■   Familiarize yourself with the process and steps required to again update etch in your design. You will learn several techniques to remove existing etch, including removing existing etch by replacing it with new etch.

Lab 10-5:   Checking for Unconnected Pins

Objective: Learn how to confirm whether you have completed all connections.

Both ratsnests and the Unconnected Pins report can show unrouted signals.

Using rats

1. Choose **View > Zoom Fit** or press **F9**.

2. Choose **Display > Show Rats > All** from the top menu.

   Any unconnected nets display as ratsnest lines.

   ### 📝 Note

   Although this option is a quick method of finding unconnected pins, it is not always effective with large designs because ratsnest lines become lost or are not easily visible.

Using the Report Command

1. Choose **Tools > Reports**.

2. Scroll through the list of reports and select the **Unconnected Pins** report.

3. Click **Report**.

   A report window appears with a list of all unconnected pins. Since all nets have been routed, your report states:

   ```
   total unconnected pin pairs 0
   ```

4. Click **Close** to close the Unconnected Pins report.

5. Click **Close** to close the report control window.

Final Editing Before Gloss

1. Experiment further with routing, or make any interactive edits you wish.

2. Choose **File > Save** from the top menu.

   A window appears and warns you that the *routed.brd* file already exists. It asks if you want to overwrite the file.

3. Click **Yes** to confirm the overwrite.

   The file *routed.brd* is written to disk.

   ### 🛑 End of Lab

Lab 10-6:   Improving Routed Connections

Objective: Learn how to improve etch paths using the **Slide** command, the **Replace Etch** function, and other techniques for adding, deleting, and moving vertex points on existing etch.

Using Slide

So far you have been adding new etch. The next lab exercise focuses on editing or moving existing etch.

1. Open the *routed.brd* file if it is not already opened.

2. Zoom in to a close-up view of a portion of your board.

3. Click the **Slide** icon in the top menu.

4. In the Find Filter, select **Vias** and **Cline Segs**. Set your options in the **Visibility** tab as follows

5. Click any segment of etch in your display.

The segment you picked travels with the cursor.

Before slide
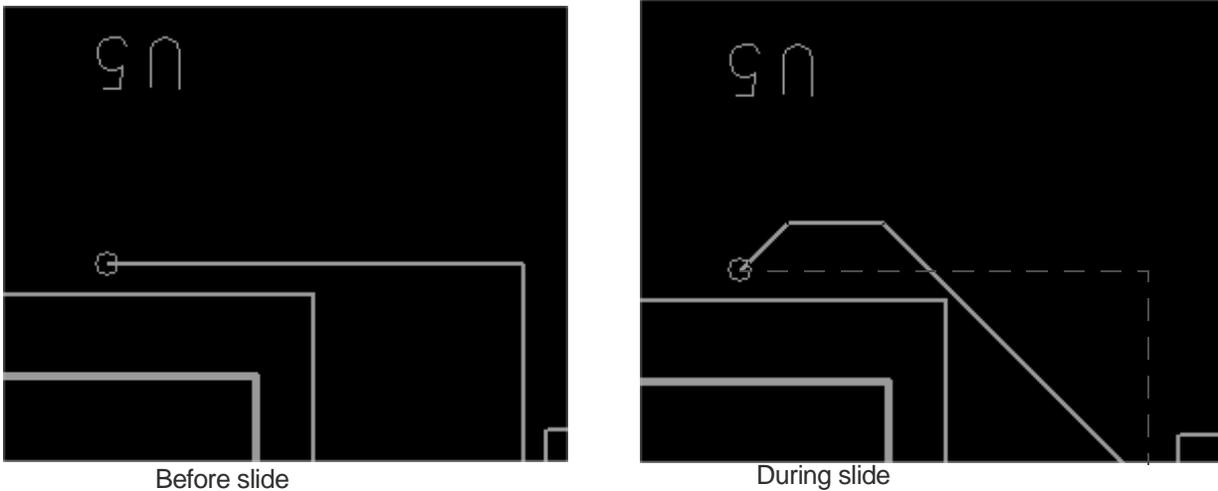
During slide

6. Choose a location for the moveable etch and click to define the new location.

The Options form controls corners that result after using **Slide**.

7. Experiment by changing the Options Corners, Max arc rad, Bubble, Shove Vias and Smooth settings and sliding other etch segments. The default setting is for 45-degree corners. This may produce some undesirable results when used with orthogonal routing. You may want to set the Corners option in the Options tab to **90**.

8. Also try combinations with the Gridless, Allow DRCs, Add at Max and Vias w/Segs options checked and unchecked to get a feel for how these choices restrict or open up sliding.

9. Right click and choose **Done** from the pop-up menu.

Moving, Creating, and Deleting Vertices

You can move vertex points or create new vertices to quickly edit existing etch.

1. Choose **Edit > Vertex** from the top menu.

2. Click a corner or vertex on an etch line.

The corner of the etch line is now attached to the cursor, and can be moved to a new location.

3. Choose a new location and click at that point.

4. Right click and choose **Next** from the pop-up menu.

The Next option lets you signify the completion of editing an etch line, but does not exit from Vertex mode. It assumes that you are about to start editing the vertex of a new line.

5. Select a point anywhere between the ends of an etch segment.

   This causes a new vertex point to be added.

6. Click a new location for the vertex.

7. Right click and choose **Done** from the pop-up menu.

8. Choose **Edit > Vertex** from the top menu.

9. Click on a corner or existing vertex point of an etch line.

10. Right click and choose **Delete Vertex**.

    The vertex is deleted, and the new trace path is shown.

11. Right click and choose **Done** from the pop-up menu.

STOP **End of Lab**

Lab 10-7: Replacing Etch and Using the Cut Option

Objective: Learn how to replace segments of etch and use the **Cut** option in conjunction with other editing commands.

Replace Etch lets you add an alternate path to an existing etch line. This new path forms a loop. The Allegro tool recognizes the older section of the loop and automatically deletes it.

You can use the **Cut** feature to define specific sections within line segments. You can use **Cut** with the **Delete**, **Slide**, and **Change** commands.

Using the Replace Etch Option

1. Open the *routed.brd* file if it is not already opened.

2. Either use the "**Z**" stroke or choose **View > Zoom by Points** to zoom in to any area of the design so that only two or three components fill the Allegro display.

3. Find an existing etch line that you want to alter, then click the **Add Connect** icon in the top menu.

   The Options form changes.

4. Make sure the **Replace Etch** option is enabled.

5. Start adding a line from a point on an existing etch line, then define a path that would form a loop:
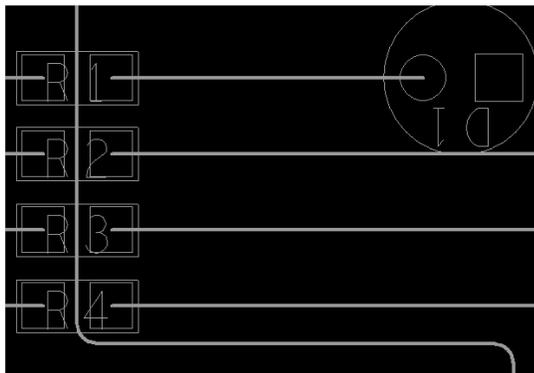
Before Replace Etch
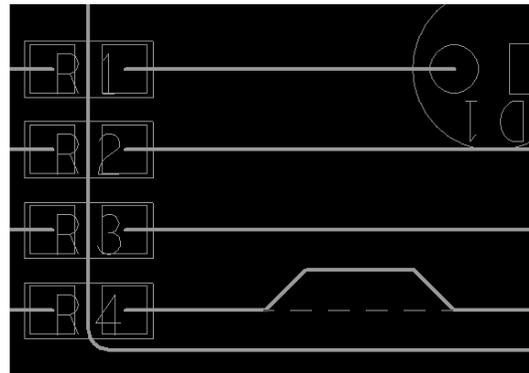
After Replace Etch

   When you click on part of the original line, the older part of the loop disappears.

6. Right click and choose **Done** from the pop-up menu.

Using Cut with Delete

1. Either use the "**Z**" stroke or press **F8** to zoom in to any area of the design so that only two or three components fill the Allegro display, and trace thickness is apparent.

2. Choose **Edit > Delete** from the top menu.

3. Set the Find Filter so that only **Cline Segs** is toggled ON.

4. Right click and choose **Cut** from the pop-up menu.

Note

On a two-button mouse, shift + right = middle mouse button.

5. Click two points, *within a single segment*, where you want the cut to occur.

    The selected section is highlighted.

6. Right click and choose **Done** from the pop-up menu.

    The highlighted portion is deleted, leaving a ratsnest in its place. Add the connection back using the skills you have learned for manual routing.

First pick

Second pick

Cut section of
routed segment
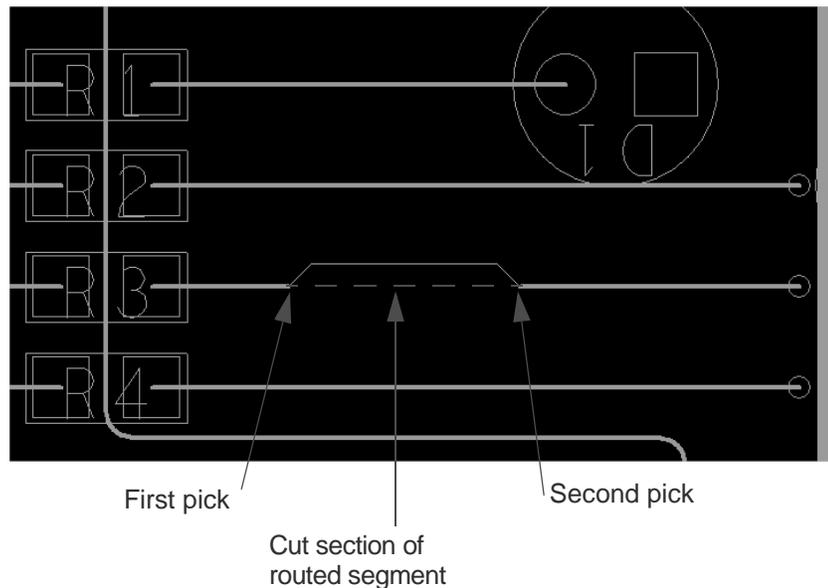
Using Cut with Slide

1. Click the **Slide** icon in the toolbar.

2. Set the Find Filter so that only **Cline Segs** is ON.

3. Right click to display a pop-up menu and choose **Cut** in this menu.

4. Click two points, *within a single segment*, where you want to define a section.

   As soon as you make the second click you will notice that the section is now moveable.

5. Click on the new location or position for the section of etch you are sliding.

6. Right click and choose **Done** from the pop-up menu.

Using Cut to Change Width

1. Choose **Edit > Change** from the top menu.

2. Set the Find Filter so that only **Cline Segs** is toggled ON.

3. In the Options form, set the options to match the figure. Change the value in the Line Width field if the current width is already 20.
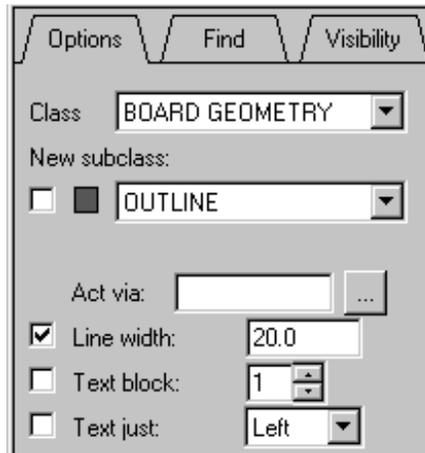
4. Right click to display a pop-up menu and choose **Cut**.

5. Click on two points, *within a single segment*, where you want to define a section to be changed.

   The new section is highlighted and changes width immediately.

6. Right click and choose **Done** from the pop-up menu.

STOP **End of Lab**

Glossing the Design
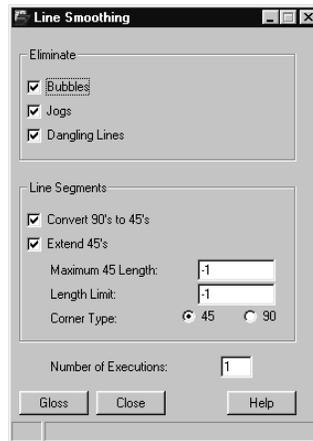
More Information

Line smoothing removes extra jogs and line segments in the design. It also converts orthogonal corners to diagonal corners. Line smoothing is a good tool to help open channels during routing.

Bubbles specifies whether Line Smoothing will attempt to eliminate connect lines that have a 45-degree line segment, followed by an orthogonal segment, followed by another 45-degree segment that slopes in the opposite direction to the first 45-degree segment, as shown in the following example:

This etch configuration can result from via elimination. Line Smoothing is a tool that smooths bubbles configured around pads that are no longer in the design.

Jogs specifies the elimination of repeated jogs or "stair steps."

Dangling Lines indicates whether Line Smoothing eliminates connect lines without two owners (pins or vias). The default is ON.

Convert 90's to 45's changes orthogonal 90-degree angles to 45-degree diagonals.

Extend 45's attempts to extend the 45-degree segment so that either the horizontal or the vertical segment can be eliminated.

Maximum 45 Length specifies the maximum orthogonal distance to which a 45-degree angle segment will be extended.

Length Limit limits the maximum length of line segments that are to be considered by Line Smoothing. Bubbles are processed if the orthogonal segment in the bubble is less than or equal to the value of this parameter. Diagonals whose orthogonal length of the diagonal is longer than this value are skipped. Jogs are only considered if the orthogonal segment in the jog is less than or equal to this limit. The default value is -1 and indicates no length limit.

Corner Type specifies whether corners are diagonal (45) or orthogonal (90). The default is 45.

Number of Executions specifies the number of times that Line Smoothing is executed. Cadence recommends that you run multiple executions. The default value is 1.

Lab

◆ Lab: Running Gloss
  ■ Cleaning routes and chamfering corners.

More Information

The following lab will allow you to familiarize yourself with the glossing process.

Lab 10-8: Running Gloss

Objective: Learn how to run gloss to make the design more manufactureable.

The Glossing program may significantly modify the route in your design. For this reason, if you have any route that you do not want to be modified, you should add properties to the nets so they will not be moved. You can attach either the NO_GLOSS property or the FIXED property to the nets so that gloss will not modify the routing of these nets. If you use the FIXED property, not only will the glossing routines not modify the route, but the user also cannot modify the route.

Using Gloss

1. Select **Route > Gloss** from the main menu.

2. Set the Number of Executions to **2**.

3. Select **Gloss**.

   The Glossing routine is run. You will see the traces being moved, and corners will change from orthogonal to diagonal.

4. After Gloss has finished, you may view the gloss log file by selecting **File > Viewlog** from the main menu.

   If you opened the *gloss.log* file, close the log file.

5. Select **File > Save As** from the top menu.

   A browser form appears.

6. In the File Name field, enter:

   gloss

7. Choose **Save**.

   The file *gloss.brd* is saved to disk.

   STOP **End of Lab**

Lesson 11: Copper Areas and Positive or Negative Planes

Learning Objectives

◆ Generate positive or negative planes.

Summary

In this section you will learn about shapes. Shapes are used to represent copper areas, among other things. Shapes can be added to a routing layer and to a plane layer. This lesson will focus on using shapes to represent a plane. However, all the procedures and ideas presented when discussing positive shapes can be applied to creating copper areas on a routing layer.

Design Layout Process
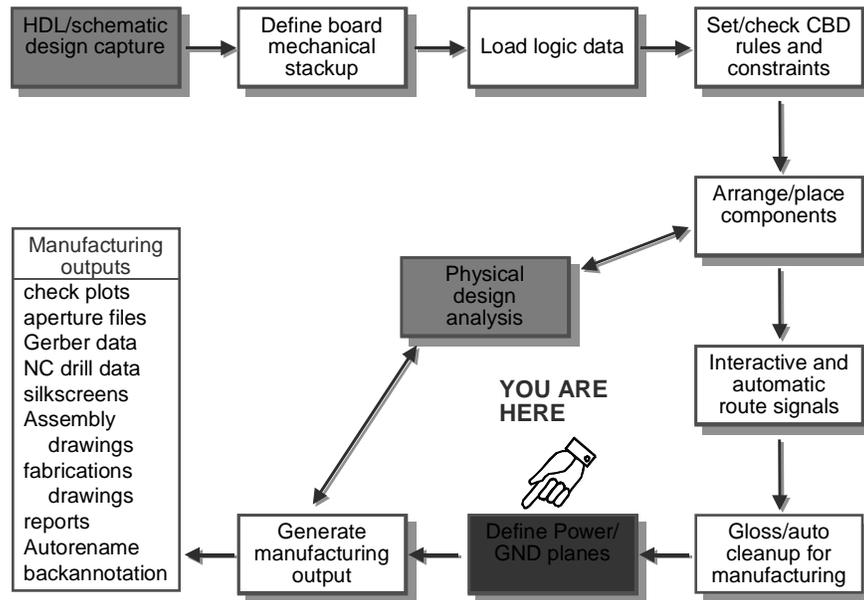
```
┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│ HDL/schematic│──▶│ Define board │──▶│ Load logic   │──▶│ Set/check CBD│
│design capture│   │  mechanical  │   │    data      │   │  rules and   │
│              │   │   stackup    │   │              │   │ constraints  │
└──────────────┘   └──────────────┘   └──────────────┘   └──────────────┘
```

```
┌────────────────────┐        ┌──────────┐        ┌──────────────┐
│   Manufacturing    │        │ Physical │        │ Arrange/place│
│      outputs       │        │  design  │        │  components  │
│ check plots        │        │ analysis │        └──────────────┘
│ aperture files     │        └──────────┘
│ Gerber data        │     YOU ARE
│ NC drill data      │     HERE              ┌──────────────┐
│ silkscreens        │                       │ Interactive  │
│ Assembly           │                       │     and      │
│    drawings        │                       │  automatic   │
│ fabrications       │                       │ route signals│
│    drawings        │                       └──────────────┘
│ reports            │ ┌────────────┐ ┌──────────────┐ ┌──────────────┐
│ Autorename         │ │  Generate  │ │ Define Power/│ │ Gloss/auto   │
│ backannotation     │ │manufacturing│ │  GND planes  │ │ cleanup for  │
└────────────────────┘ │   output   │ │              │ │ manufacturing│
                       └────────────┘ └──────────────┘ └──────────────┘
```

More Information

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the define power/gnd planes box will now be discussed.

Copper Area Images

Negative plane   **Positive plane**

Artwork

Allegro
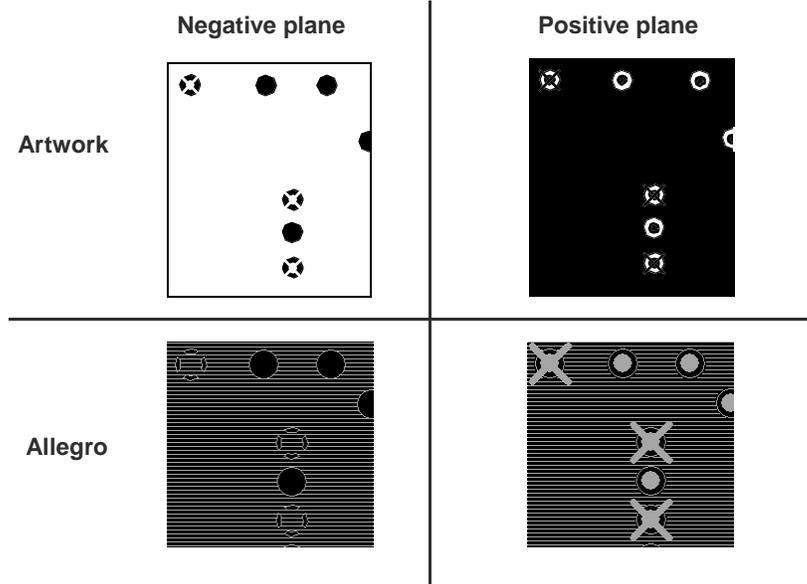
More Information

There are two methods of creating copper areas, each with advantages and disadvantages.

◆ Negative Image

One advantage is that when you use the vector Gerber format, the artwork file required to plot this copper area is much smaller because no data is required to fill the polygon.

Another advantage is that this type of copper area is more flexible; it can be created early in the design process, and will accommodate dynamic placement and routing changes.

A disadvantage is that you must build flash symbols for all thermal relief flash names.

◆ Positive Image

An advantage is that the Allegro display is WYSIWYG (you see the actual positive copper fill as well as the anti-pad and thermal relief features—no special flash symbols are required).

One disadvantage is that if you are not generating rasterized output, the artwork file required to plot this copper area is much larger because of the vector data required to fill the polygon. You also need to fix any shape fill problems before artwork can be created.

Another disadvantage is that you must regenerate the shape after making placement and routing changes.

Creating a Negative Copper Area

1. Use the **Add Shape** command to draw the polygon on the proper etch layer.
   - Check **Options** for active class and subclass.
   - Polygon must be within route keepin.
   - To close the polygon, right click and select **Done** from the popup.
   - As soon as the polygon is closed, the Allegro top menu changes.
   - You are now in the **Edit Shape** mode.
2. Use the **Edit > Change Net** command to assign a netname to the copper area.
   - Examples are: vcc, gnd, +5v, agnd, +12v
3. Use the **Shape > Fill** command to fill the polygon.
   - The Allegro top menu changes, and you are no longer in **Edit Shape** mode.

Summary

It is important to understand the process Allegro uses at artwork time for a negative plane. When the Gerber files are being generated, Allegro looks at each pin and via in the design. If the net name associated with the pin or via IS NOT the name associated with the copper area, Allegro will look at the padstack associated with the pin or via, and use the anti-pad definition for the subclass. If the net name associated with the pin or via is the same as the name associated with the copper area, Allegro will look at the padstack associated with that pin or via, and use the flash name defined for the thermal relief for the subclass.

More Information

Select the **Add > Shapes > Solid Fill** option from the top menu to execute the command to create a copper area. After executing the command, you should first ensure that the Options folder tab has been set correctly, verifying that the class is set to Etch, and the subclass is set to the layer on which the copper area should appear.

You then select each vertex for the polygon. The polygon MUST start and stop at the same point. You can also select **Done** from the right mouse button pop-up menu to close the polygon. When you use the Done option, Allegro takes your last entered vertex and completes the polygon from that point to the original starting point.

Once the polygon has been closed, the menu bar changes. You are now in Edit Shape mode. Select the **Edit > Change Net** option from the top menu to assign a net name to the polygon. Next, select the **Shape > Fill** option from the top menu to fill the polygon. The shape becomes filled, and you are no longer in the Edit Shape mode. Your negative plane is now complete.

Creating a Positive Copper Area

1. Use the **Add Shape** command to draw the polygon on the proper etch layer.
   - Check **Options** for active class and subclass.
   - Polygon must be within route keepin.
   - To close the polygon, right click and select **Done** from the popup.
   - As soon as the polygon is closed, the Allegro top menu changes.
   - You are now in the **Edit Shape** mode.
2. Use the **Edit > Change Net** command to assign a netname to the copper area.
   - Examples are: vcc, gnd, +5v, agnd, +12v
3. Use **Shape > Parameters** to specify void and fill options.
4. Use the **Void > Auto** command for manual and automatic voiding.
5. Use the **Shape > Fill** command to fill the polygon.
   - The Allegro top menu changes, and you are no longer in **Edit Shape**

More Information

Creating a positive copper area is a five-step process. The first, second and last steps are exactly the same as for building a negative copper area.

The **Add Shape** command offers three choices of shape types: Crosshatch, Solid, or Unfilled. Use Crosshatch or Solid (it is possible to switch between these fill styles).

Set the Options form to the correct etch layer. Draw the polygon and use the **Edit > Change Net** command to assign a net name to this copper area.

A positive copper area is different from a negative copper area. Positive copper will undergo parameter-driven "void-and-fill" processes. Because of this, the following extra steps are needed:

- **Shape > Parameters** controls the void-and-fill processes within the copper area.

- **Void > Auto** reads the parameters for the copper area. Clearances for all pins and vias are created. Voltage pins that need to connect to the surrounding copper area receive thermal relief tie bars. When **Void > Auto** is run, it checks for filling problems (small or narrow areas that will be difficult to fill based on the size of the art-check aperture).

■   Select the **Shape > Fill** button from the top menu to complete this
        process.

Void and Fill Parameters

Shape > Parameters

More Information

While you are in Edit Shape mode, select the Shape Parameters option
from the top menu to open the Shape Parameters form. The parameters in
this form are used to drive the autovoid routine.

There are four sections to the Shape Parameters form. The first section,
located at the top left of the form, is the Shape Fill section. You use this
section to set the fill style of the shape. The fill style can be either solid or
crosshatched. There are several different crosshatch styles that you can set,
such as Vertical, Horizontal, Diagonal Positive, Diagonal Negative, and so
forth. There is also a Custom style that you can choose to define your own
crosshatch style.

The second section, located at the top right of the form, is the Clearances
section. You use this section to set how far away the copper should be kept
from pins and vias, lines, clines, text, other shapes, and rectangles. For
each of these items, the options are: DRC Value, where Allegro looks at the
shape-to-item clearance as defined in the constraint set; Default, where you
specify an exact amount of clearance for this item, which is defined in the
Default field to the right of the item; and None, where no clearance will be
generated for this item. For Pins, which includes pins and vias, an
additional option of Thermal Anti-Pad can be set. With this option set,
Allegro looks at the padstack for the pin or via and uses the size and shape
of the anti-pad for the subclass.

The third section of the Shape Parameters form, located at the bottom left of the form, is the Void Controls section. The Create Pin Voids toggle specifies an algorithm for generating voids around a series of pads, mainly dip patterns. In this section, the option individually correlates to drawing a void around each pad separately. In Line correlates to drawing one void around the entire group of pads.

The fourth section of the Shape Parameters form, located at the bottom right of the form, is the Thermal Relief Connects section. This section specifies how pins and vias with the same net name as the shape should be connected to the shape. You can specify an orthogonal connection, a diagonal connection, a full contact connection where the copper actually floods over the pad, or an 8-way connection. You also specify the width and the number of connections from the pad to the copper area. After you set the parameters, select the **OK** button to close the form.

Crosshatch Copper

Shape > Parameters
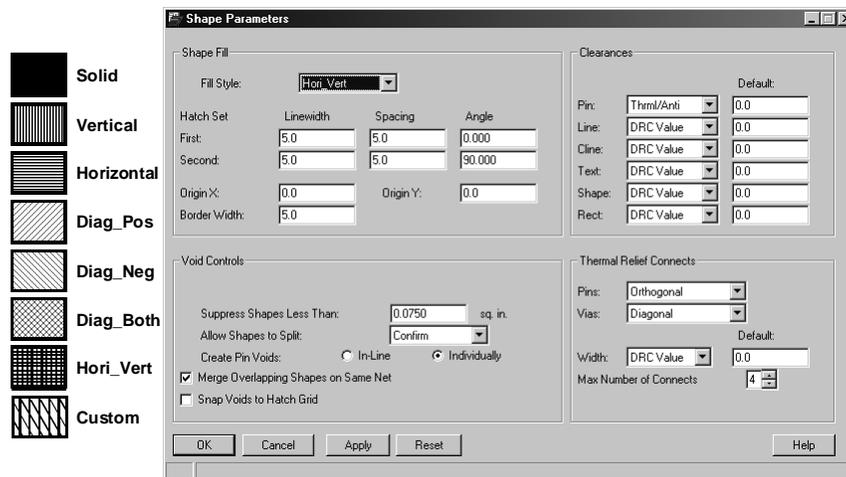
More Information

In the Shape Fill section you can select from a number of crosshatch styles by clicking left in the Style field. (The most common is Hori_Vert.)

Hatch Set defines up to two different directions in which lines will be drawn.

Linewidth, **Spacing** and **Angle** are defined for each hatch set (or direction).

Origin X and **Origin Y** let you define the starting point for a group of hatch lines.

Border Width is the line used to "profile" all the edges of the polygon.

Allow Shapes to Split: Depending upon how you set your void and fill parameters, so much copper may be removed around pads, vias, lines, and so forth, that the copper area can no longer remain contiguous. If this happens, the following options are invoked:

- **Yes** means to break up the copper into multiple pieces.

- **Confirm** lets you choose to proceed with the split, or abort the autovoid process.

- **No** means do not split up the copper area (the autovoid process is aborted).

Snap Voids To Hatch Grid controls how the clearance areas for pins, vias, and so forth are created. If this option is off, the void geometries are not forced onto the routing grid.

WYSIWYG crosshatch lines are displayed at true width.

Use the **Apply** and **Reset** buttons to experiment with parameter changes. These buttons let you toggle between previous and current settings to see the "before/after" effects of parameter changes (for example, changes to border width).

Editing Copper Areas

1. Choose **Edit > Shape** from the top menu.
2. Select the shape.
3. Choose **Done** from the pop-up menu.
4. Shape is now in an "unfilled" state. The top menu changes, and you are now in Edit Shape mode.
5. You can now edit the shape outline boundaries.
6. You can add, delete, and edit void areas with the shape outline.
7. You *must* use **Shape > Fill** to fill the shape and exit from Edit Shape mode.

More Information

The first step in editing any existing copper area is to unfill the shape. Shapes cannot be edited while they are filled. There is no "unfill" button, so to accomplish this, use the following process:

- Select **Edit > Shape** from the top menu.

- Click left to select the shape.

- Click right to display a pop-up menu, and select **Done**.

  - The copper area becomes unfilled.
  - The top menu changes, and you are now in Edit Shape mode.

You can only edit one shape at a time, so all **Chg Net, Void**, and **Edit** commands affect only the current (unfilled and active) area.

After all editing is complete, you must select **Shape > Fill** to exit from Edit Shape mode.

You can also add, delete, or change existing voids within the current shape while editing.

Editing Copper Areas—Options
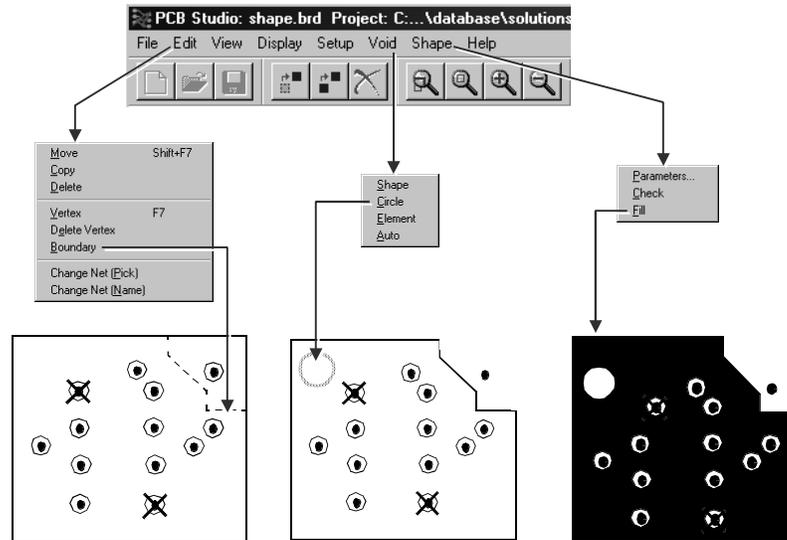
More Information

Void > Auto invokes a routine that checks for small or narrow areas that might cause problems during filling. If filling problems are found, these areas are flagged with circles (known as shape problems). Use the **Void** command options to fix these problems. Then select **Shape > Check** from the top menu to remove the error markers and recheck the copper area. When checking the copper area for fill problems, never specify an aperture less than 4 mils (unless you are generating raster data).

Void > Shape creates a non-copper polygon within the copper area.

Void > Circle creates a non-copper circle within the copper area.

Void > Element lets you select a pin or via and automatically adds a clearance hole.

Edit > Boundary lets you change the shape of the copper area.

Note that the shape must be in an "unfilled" state to access the commands shown.

Lab

◆ Lab: Copper Areas
  ■ Generate positive and negative planes.
    ● Set up for embedded planes
    ● Set up for thermal pad display.
    ● Edit the shape to assign a net name.
    ● Change DRC settings.
    ● Void the shape and other copper void options.

More Information

The following lab will allow you to familiarize yourself with the process required to create both negative and positive planes. You will learn how to set your display for negative planes, learn how to add shapes and how to void positive shapes.

Lab 11-1:   Copper Areas

Objective: Learn how to generate negative and positive planes.

At the end of this lab, you will be able to:

◆   Generate positive and negative planes.

◆   Learn how to set the parameters for a positive plane.

Set up for Embedded Planes

In the routing lesson, you created the VCC and GND planes so that the SPECCTRA autorouter knew where the planes where and also knew the net names associated with each shape. You will use these shapes as the basis for the final planes.

1.   If you don't already have the Allegro software running, start Allegro.

2.   Open the *gloss.brd* file if it is not the current design.

The *gloss.brd* file appears in the work area.

Setup for Thermal Pad Display

1.   Choose **Setup > Drawing Options** from the top menu.

The Drawing Options window appears.

2.   In the Display folder tab of the Drawing Options window, turn on **Thermal Pads** and **Filled Pads**.

This enables the display of thermal relief patterns for negative copper areas.

3.   Click **OK**.

4.   Use the Visibility tab to turn ON only the **VCC** layer.

5.   Choose **Display > Dehighlight** from the top menu.

6.   In the Find Filter tab, set the Find by Name section to **Net**.

7.   Enter "*****" in the Find by Name value field.

Any nets that have been highlighted will now be dehighlighted.

8.   Select **Done** from the right mouse button popup.

9.   Zoom in to see the clearances around the pins and vias that do not connect to the VCC plane.

The pins and vias connected to the plane will have the appropriate flash symbol displayed. Since the VCC plane is a negative plane, it is now created and ready for artwork.

10.   Choose **File > Save As** from the top menu.

A browser form appears.

11. In the File Name field enter:

shape

12. Choose the **Save** button in the file browser.

The file *shape.brd* is saved to disk.

Changing DRC Settings

You will now finish the positive GND plane. When artwork is created, this layer will be plotted as a positive image (copper = black). First you need to change the layer stackup so this plane layer will have DRC run as a positive plane.

1. Choose **Setup > Subclasses** from the top menu.

The Define Subclass form appears.

2. Select the **Etch** subclass from the form.

The Define Etch Subclass form appears.

3. In the Film Type column of this form, change the GND layer from Negative to **Positive**.

4. Click **OK** in the Define Etch Subclass form.

5. Click **OK** in the Define Subclass form.

Editing the GND Plane

You will now edit the positive GND plane. When artwork is created, this layer will be plotted as a positive image (copper = black).

1. Click the **Visibility** folder tab in the Control Panel to bring the Visibility menu forward.

2. Toggle all layers OFF, then toggle all GND layer items ON.

3. Select **Edit > Shape**.

4. Select the **GND** shape.

The GND shape highlights.

5. Select **Done** from the right mouse button popup.

As soon as you select Done, the top menu changes to the Shape Edit menu.

Voiding the Shape

1. Choose **Shape > Parameters** from the top menu.

The Shape Parameters form opens.

2. Review the parameter settings, but no changes are needed at this time.

3. Click **OK** in the Shape Parameters form to close the form and apply your changes.

4. Choose **Void > Auto** from the top menu.

Pin clearances and GND connections are added.

A Shape Log window displays. If any problem areas are detected while avoiding the plane, the shape log will document them, and "circles" will be drawn around the problem areas on the class/subclass MANUFACTURING/SHAPE PROBLEMS.

5. Click **Close** to close the Shape error log window.

6. Choose **Shape > Fill** from the top menu.

7. Choose **File > Save** from the top menu.

A window appears and warns you that the *shape.brd* file already exists. It asks if you want to overwrite the file.

8. Click **Yes** to confirm the overwrite.

The *shape.brd* file is saved to disk.

Other Copper Void Options

In this section of the lab, you experiment with other techniques for creating void areas.

1. From the top menu, choose **Edit > Shape**.

2. Click on the **GND** plane.

The shape is highlighted.

3. Right click and choose **Done**.

A message window appears and asks if you want to rip up the thermal relief clines.

4. Click **Yes**.

The shape becomes *unfilled* and the top menu changes.

5. Choose **Shape > Parameters** from the top menu.

The Shape Parameters form appears.

6. Set the Create Pin Voids option to **In-Line**.

7. Click **OK**.

8. From the top menu, choose **Void > Auto**.

Allegro Layout System   11-13

Notice the Allegro message line informs you of creating voids, performing autovoid, and connecting thermal relief pads. Also the Shape Log form appears.

9. Click **Close** to close the Shape error log window.

   Notice that the pins on the through-hole connector on the left side of the board have a single void, instead of individual voids.

10. Right click and choose **Done** from the pop-up menu.

11. Experiment with the **Void > Circle** and **Void > Shape** commands to create additional areas that are free of copper.

12. Experiment with the **Edit > Boundary** command to change the outline of the copper area. Make sure to turn OFF the Route Keepin Class so as not to edit the route keepin by mistake.

13. Choose the **Shape > Fill** button to fill the shape.

14. Examine the results.

15. Choose **File > Save** from the top menu.

   A window appears and warns you that the *shape.brd* file already exists. It asks if you want to overwrite the file.

16. Click **Yes** to confirm the overwrite.

   The *shape.brd* file is saved to disk.

STOP **End of Lab**

# Lesson 12: Preparing for Post Processing

Learning Objectives

- ◆ Learn how to reset reference designators.

- ◆ Learn how to backannotate changes made in Allegro to one of three different schematic design environments:

  - ■ Concept HDL

  - ■ Capture

  - ■ Third-party

Summary

In this section you will learn about preparing your design for post processing. This will include automatic and manual renaming of reference designators, and backannotating your design changes to your schematic.

Design Layout Process
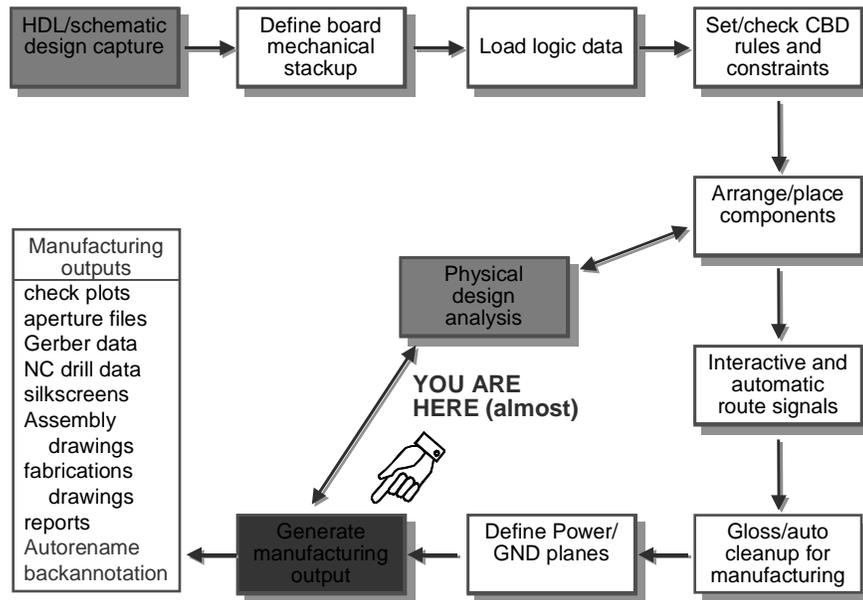
```
┌─────────────┐    ┌─────────────┐    ┌─────────────┐    ┌─────────────┐
│HDL/schematic│───▶│Define board │───▶│Load logic   │───▶│Set/check CBD│
│design capture│   │mechanical   │    │data         │    │rules and    │
│             │    │stackup      │    │             │    │constraints  │
└─────────────┘    └─────────────┘    └─────────────┘    └─────────────┘
```

Arrange/place components

Physical design analysis

YOU ARE HERE (almost)

Interactive and automatic route signals

Manufacturing outputs
check plots
aperture files
Gerber data
NC drill data
silkscreens
Assembly
    drawings
fabrications
    drawings
reports
Autorename
backannotation

Generate manufacturing output

Define Power/ GND planes

Gloss/auto cleanup for manufacturing

More Information

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. The items about to be discussed are sometimes included in the manufacturing output area.

Renaming Reference Designators

Choose a resequencing method
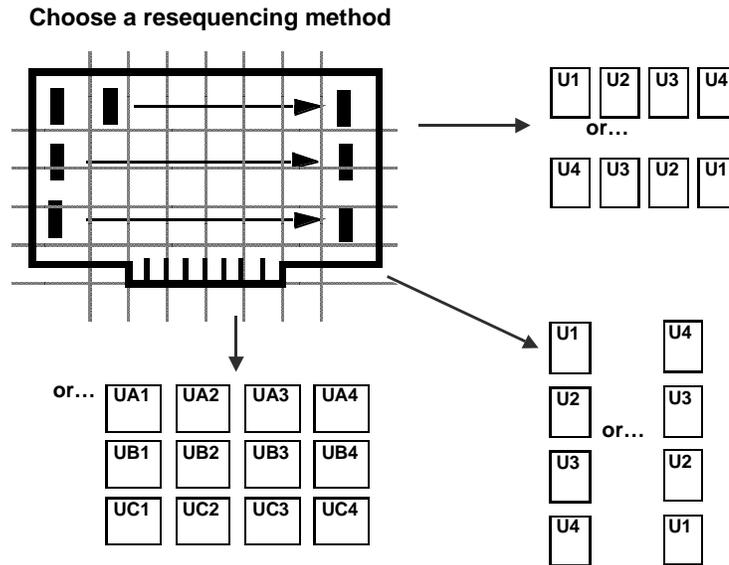
Summary

You can rename your reference designators and backannotate to your schematic at any time in the design process. For example, after placement, you may want to rename your components to reflect the changes. After renaming, you would want to backannotate your schematics. Renaming and backannotation are presented here mainly to present a consistent flow and also as another point during which you may want to perform these tasks.

More Information

It is not uncommon to rename (resequence) the reference designators on a board after part placement, or at the end of the layout phase. The process results in a physical layout that is easier to test, debug, rework, assemble, and maintain in the field. A particular component is easier to locate when reference designators on the board are ordered in a consistent and predictable fashion (such as left to right, top to bottom).

The automatic renaming process in Allegro lets you rename every component on a design in a single operation. You can also elect to rename individual components by attaching the AUTO_RENAME property to them, or rename components on one side of the board only.

Renaming is controlled by placement grid line locations only (user-defined or default selection) or by sequential renaming within grid blocks. With grid-based renaming, you can designate the direction (horizontal or vertical) and order (left-right, right-left, upwards-downwards) of the renaming process. Additionally, you can define grid descriptions by alpha characters and/or integers.

To access automatic renaming tools in Allegro, select **Tools > Auto Rename RefDes**.

Rename Reference Designators (Main Form)

Tools > Auto Rename RefDes

Click More to get to the setup form
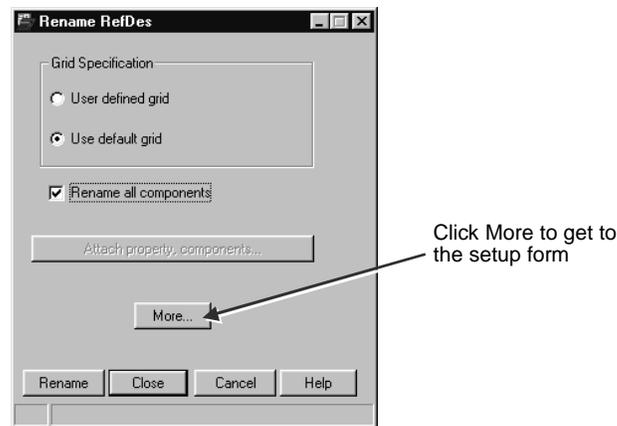
More Information

Use the following steps to automatically rename your components:

1. Choose **Tools > Auto Rename Refdes** from the top menu.

2. Choose the type of placement grid you want to use.

   ■ **User Defined Grid** - You define a grid on the class BOARD GEOMETRY and subclasses PLACE_GRID_TOP and PLACE_GRID_BOTTOM. The system will use these grids, looking at each grid square based upon the direction specified in the Rename RefDes Setup Form (see next page).

   ■ **Use Default Grid** - This option basically results in no two parts ever being considered in the same block for renaming purposes.

3. Select which components to rename.

   ■ **Rename All Components** - Renames all components on the side of the board specified in the Rename RefDes Setup Form (see next page).

■ **Attach Property, Components** - You must attach the property AUTO_RENAME to all components that are to be renamed in this pass.

4. Click **More**... to check or change sequencing parameters (see next page).

5. Click **OK** in the Rename RefDes menu to begin execution.

Rename Reference Designators (Setup Form)

More Information

Select the **More** button to bring up the Rename Ref Des Setup form. You use this second form to set the parameters used when running the rename reference designator command.

The **Layer Options** section of this form specifies whether to rename the top side, bottom side, or both sides of the design. You also specify the origin point of the part for renaming purposes.

Use the **Directions for Top Layer** and **Directions for Bottom Layer** sections of this form to specify the rename order for the appropriate layer.

Use the **Reference Designator Format** section to specify how the new reference designator names should be created. The Ref Des prefix field specifies what the starting character or characters of the new name should be. An asterisk in this field specifies that the reference designator format as defined in the library footprint symbol should be used as the starting character or characters of the new name. If you want to keep the current prefix as was defined from the schematic, use an asterisk in this field, and check the box titled Preserve Current Prefixes. Use the fields Top Layer Identifier and Bottom Layer Identifier to specify a character that will be appended to the new reference designator name on the appropriate layer. Use the field Skip Characters to identify the characters that should not be included when creating a new reference designator name.

The Renaming Method field can be set to either Sequential or Grid Based. If you choose the sequential method, the **Sequential Renaming** section becomes available. Use the field Ref Des Digits to specify the minimum number of digits that should be used when creating a new reference designator name. For example, if 2 is specified, the numbers following the reference designator prefix would be 01, 02, 03 and so forth.

If you choose the Grid Based method, the **Grid Based Renaming** section becomes available. You use the **First Direction Designation** and **Second Direction Designation** fields to assign the prefixes to be used when creating the new reference designator name. Use the **Suffix** field if there is more than one component in the same grid cell. If you are going to use the grid based renaming method, you should use the User Defined Grid method as discussed above.

Once you have specified all the parameters in the Rename Ref Des SetUp form, select Close in this form. To execute the renaming sequence, select **OK** in the Rename Ref Des form.

Rename Reference Designators—Key Points

Things to remember:

- A component can be individually renamed by editing its attached reference designator text.

- An **AUTO_RENAME** property can be attached to specific groups of components to sequence them separately.

- A **HARD_LOCATION** property can be used to prevent certain components from being renamed.

- User-defined grid cells can be used to determine specific row and column boundaries.

- There are many options available for determining number and letter sequencing. Refer to the online help files to find your best settings.

- When you rename components, you must backannotate to your schematic source.

More Information

When you rename reference designators, there are a few things to remember. You can manually rename a part by changing the reference designator text. To manually change the reference designator, select the **Edit > Text** option from the top menu, select the reference designator to be renamed, and enter in the new reference designator on the Allegro command line. You can change the text on the assembly top, assembly bottom, silkscreen top, or silkscreen bottom subclasses under the class Ref Des. If there are certain parts that you do not want to be renamed by the auto rename tool, attach the property **HARD_LOCATION** to them. When you rename your components, you must backannotate your schematics with the reference designator changes to keep the schematic and the design in sync.

Lab

- ◆ Lab: Renaming Components
  - Use the renaming capability in Allegro to set up resequencing and change Reference Designators.

More Information

The following labs will allow you to familiarize yourself with the process and steps required to automatically and manually rename your design.

Lab 12-1:   Renaming Components

Objective: Learn how to assign new reference designators automatically and interactively.

1. If you don't already have Allegro software running, start Allegro.

2. Open the file *shape.brd*.

Setting Colors and Visibility

1. Choose **View > Zoom Fit** from the top menu.

2. Choose **Display > Color/Visibility** from the top menu.

3. In the Global Visibility scroll bar window, select **All Invisible**.

4. Select **Yes** to confirm change of visibility of all classes.

5. Select the **Components** group.

6. Under the REF DES class, turn ON **ASSEMBLY_TOP** and **ASSEMBLY_BOTTOM**.

7. Select the **Geometry** group.

8. Under the BOARD GEOMETRY class, turn ON **OUTLINE**.

9. Under the PACKAGE GEOMETRY class, turn ON **ASSEMBLY_TOP** and **ASSEMBLY_BOTTOM**.

10. Select the **Stack-Up** group.

    It is easier to see the reference designators with the wiring turned off.

11. Turn ON the following:

    TOP-PINS, BOTTOM-PINS, TOP-VIAS

12. Click **OK** to close the Color and Visibility form.

Renaming Components

1. Choose **Tools > Auto Rename RefDes** from the top menu.

    The Rename RefDes menu appears.

2. Check to see that **Use Default Grid** is selected.

3. Check to see that **Rename ALL Components** is selected.

4. Click on the **More**... button.

    The Rename RefDes Setup form appears.

5. Make adjustments to this menu to match the following:

Notice that the Top Layer Identifier and the Bottom Layer Identifier fields have been blanked out and the Preserve current prefixes check box has been enabled.

6. Click **Close** to return to the Rename RefDes Setup menu.

7. Click **Rename** to begin executing the automatic rename process.

8. Click **Close** to close the Rename RefDes form.

9. Zoom in or pan your view to inspect your results.

10. Choose **File > Save As** from the top menu.

A browser form appears.

11. In the File Name field, enter:

final

12. Click **Save** in the file browser.

The file *final.brd* is saved to disk.

You will overwrite this version of your design while preparing it for final output phases.

Interactively Renaming Parts

1. Zoom in to view a component of your choice.

2. Choose **Edit > Text** from the top menu.

   The Allegro message area prompts,

   ```
   Pick text to edit.
   ```

3. Click on the reference designator of the part you want to rename.

   The selected refdes id is highlighted.

4. At the Allegro command line, enter:

   U99 (or any name you wish)

   ### Note

   If the name you choose already exists in your design, you are notified in the Allegro message area that the name is being swapped with another component. This feature prevents you from accidentally creating duplicate names.

5. To exit from the **Edit > Text** command, right click and choose **Done** from the pop-up menu.

6. Choose **File > Save** from the top menu.

   A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

7. Click **Yes** to confirm the overwrite.

   The file *final.brd* is written to disk.

STOP End of Lab

Backannotation

**Mapping changes from the physical layout
back to the logical schematic world**
- property changes
- ref-des changes
- pin and gate swaps
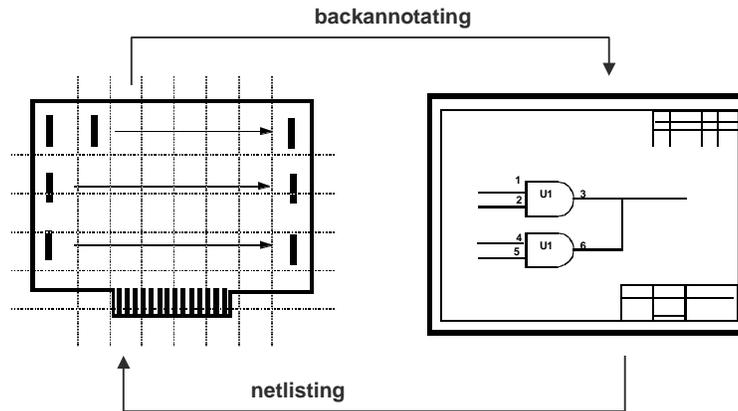
More Information

If you rename the reference designators in your design, you will need to
backannotate these changes to the schematic. In order for backannotation
to work correctly, the schematic must not have been changed since the last
logic import into the Allegro board or the last backannotation had been
performed.

Backannotation Examples

Gate Swapping

Pin Swapping

Reference Designator Rename

U1   U2   U3
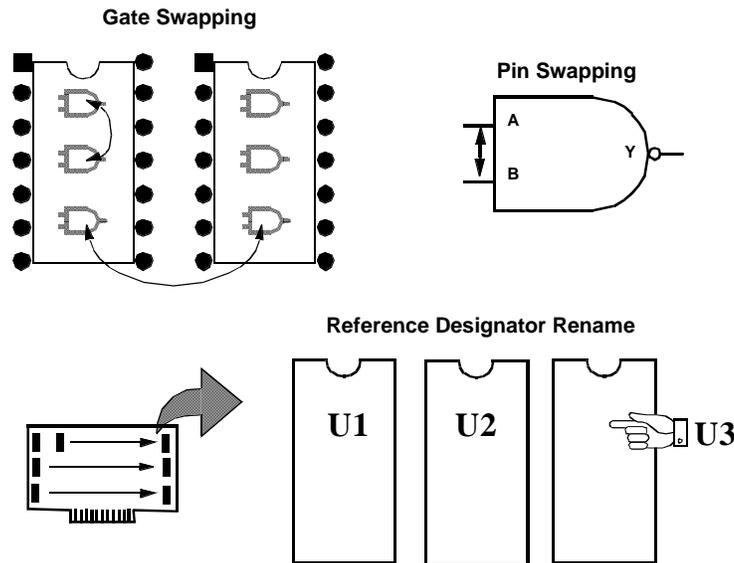
More Information

There are other changes that can be made that will require backannotation. The Allegro tool can perform gate and pin swapping, which can improve component placement and routing.

These processes—gate and pin swapping, and rename—represent changes to the Allegro database, and must be communicated back to the schematic.

Backannotation is capable of documenting reference designator and physical pin number changes only. To perform properly, the schematic and physical layout must match. If parts exist in the schematic that are not on the board (or vice versa), or schematic connectivity does not match the physical layout, these differences will be identified.

Backannotation—Concept Export Netlist

| …/worklib/esdesign/packaged | …/worklib/esdesign/physical |

pinView.dat
netView.dat
funcView.dat
compView.dat

Design Sync ▶

← **design.brd**

Packager-XL

feedback.log

pstback.dat
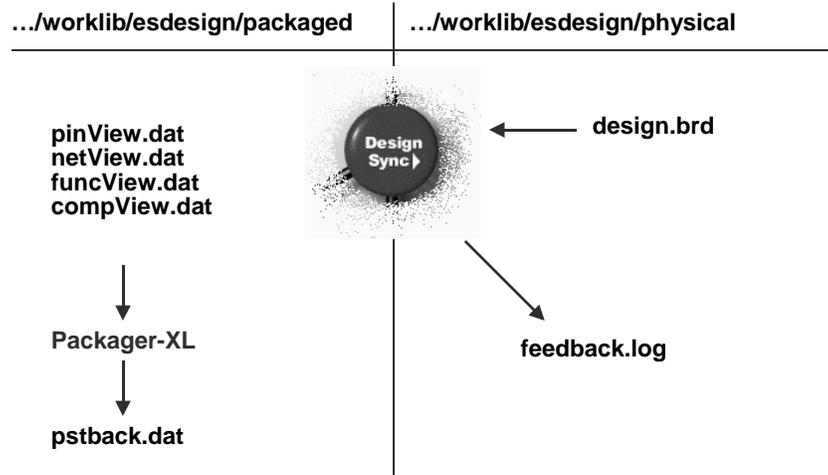
More Information

The **Export Netlist** command generates the backannotation files required to update the schematic. When communicating information back to the Concept tool, these files are:

- ■ *pinView.dat* contains reference designator, pin number, and netname for each device pin in the schematic.

- ■ *compView.dat* contains component instance properties.

- ■ *netView.dat* contains net properties.

- ■ *funcView.dat* contains function properties.

- ■ *cmdbview.dat* contains the electrical constraints.

- ■ *cmbcview.dat* contains the baseline electrical constraint sets.

Before you can update the Concept schematic you must repackage it. This file serves as input to the Packager (when run in "feedback" mode).

- ■ *pstback.dat* is the backannotation file that is produced whenever you run the packager. Use this file to update the schematic.

Backannotation to Concept

From Allegro:
File > Export > Logic

From Concept:
File > Import Physical
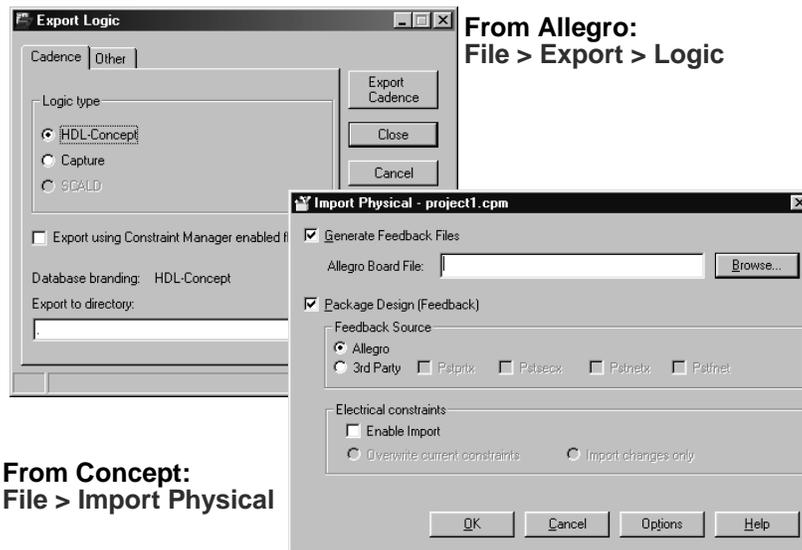
More Information

Export Logic creates a temporary file from the active board and creates the required *.dat* files. The Allegro tool knows which *.dat* files to create, based on a directive in each *pstxprt.dat* file.

- ◆ From Allegro, select **File > Export > Logic**.

- ◆ From Concept, select **File > Import Physical**.

- ◆ From the Project Manager, click **Design Sync**.

The Allegro tool creates the output files in the Allegro working directory. A log file, *feedback.log*, is also created, which you can view using the **File > Viewlog** command.

Property Backannotation

- ◆ Component Instance Properties (*compView.dat*)
- ◆ Schematic Instance Properties (*funcView.dat*)
- ◆ Pin Instance Properties (*pinView.dat*)
- ◆ Net Properties (*netView.dat*)
- ◆ Electrical Rules (*cmdbView.dat* and *cmbcView.dat*)

NOTES

- Properties added to Allegro will transfer back to the schematic.
- Component definition properties are **NOT** backannotated.

Logical World   **Physical World**
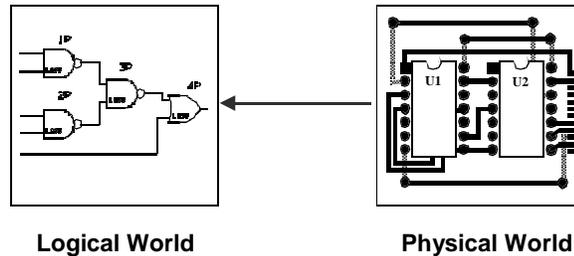
More Information

The Allegro tool does not backannotate Component Definition Properties (in general, because they cannot be changed in Allegro software). The exception is jedec_type (changed when using alt_symbols).

Property Changes During ECO

Property values in the new (edited) schematic override the existing values in the Allegro tool. Existing Allegro properties not defined in the schematic remain unchanged. For example:

■ A logic designer utilizes the ECL property to indicate that five nets are high-speed. Later, the logic designer discovers he has labeled the wrong net(s). The property is removed, and attached to the correct net(s). After the ECO is performed, the Allegro design will contain ten ECL nets. Removing the property from the five original nets will not affect their current assignments in the Allegro software, nor will backannotation remove properties from the schematic.

■ A schematic contains a trace length requirement (delay_rule property). During placement, the layout designer determines that this requirement is too restrictive, and changes it in Allegro. Later, an edited schematic containing the old value is used to perform engineering changes, and the Allegro edit is lost. Solution: run backannotation after editing the property value within Allegro.

The file that controls which properties will be backannotated when using the Packager-XL is titled *<cds inst dir>/tools/pcb/text/views/pxlBA.txt*.

Capture Integrated Logic Design/Physical Layout
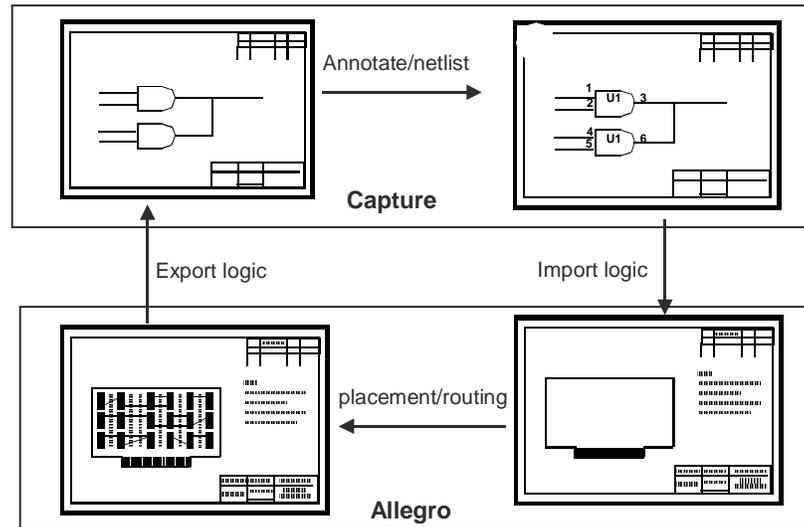
More Information

The diagram illustrates the front-to-back integration between Capture and Allegro tools.

Capture Front End

1. **Capture**: It is not required that the Capture schematic reside in the same directory as the Allegro design. However, it is recommended that the two be kept together.

2. **Annotate**: The Annotate program converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic.

3. **Allegro Netlister**: The Allegro Netlister creates the transfer files used by Allegro. By default, these files are created in a directory named *allegro*.

Allegro

1. **Import Logic**: After this step, the design now contains connection information.

2. **Allegro**: Places, routes, pin and gate swaps for optimum routing results; generates manufacturing output.

3. **Export Logic**: This program generates backannotation files the Capture tool uses to update the schematic.

Allegro-Capture Backannotation
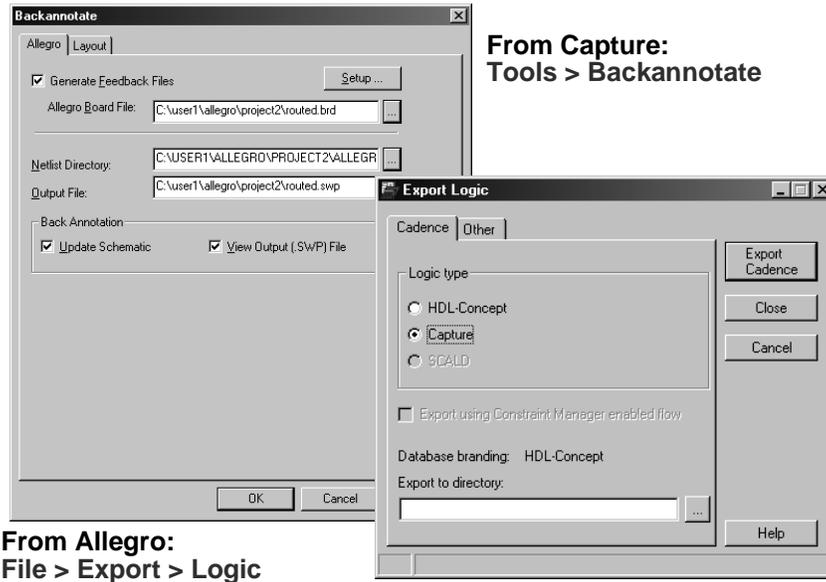
From Capture:
Tools > Backannotate

From Allegro:
File > Export > Logic

More Information

The first step in backannotating from Allegro to Capture is to generate the feedback files. These are the same four *compView.dat, funcView.dat, pinView.dat* and *netView.dat* files used in the Allegro to Concept backannotation process. This can be done from within Allegro by using the **File > Export > Logic** command or by using the **Generate Feedback Files** option from the Capture **Backannotate** command.

After the four feedback files have been generated from the Allegro design, you must run the backannotation process from within Capture. This process will read the Allegro-generated feedback files, create an output swap file that contains all the required backannotation information required by Capture, and update the schematic.

Third-party Backannotation Process

External Front End

From Allegro:
File > Export > Logic

netlist.txt

Allegro

device.txt

devpath

Netin

<design>.baf

netin.log

netin.brd
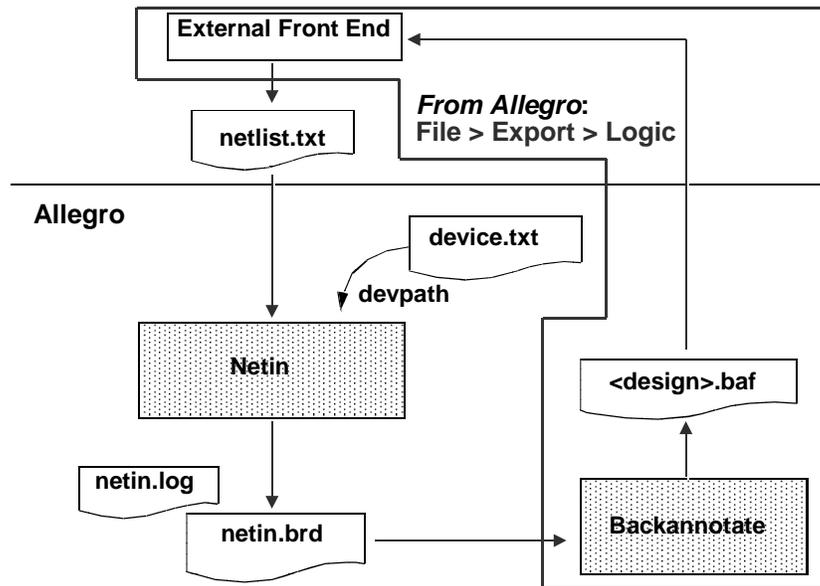
Backannotate

More Information

You need to perform backannotation for a third-party netlist board if you make any logical changes such as pin swapping, gate swapping, reference designator renaming, and so on. Remember that pin and gate swapping can only be accomplished if the device file is created to support swapping.

Third-Party Backannotation
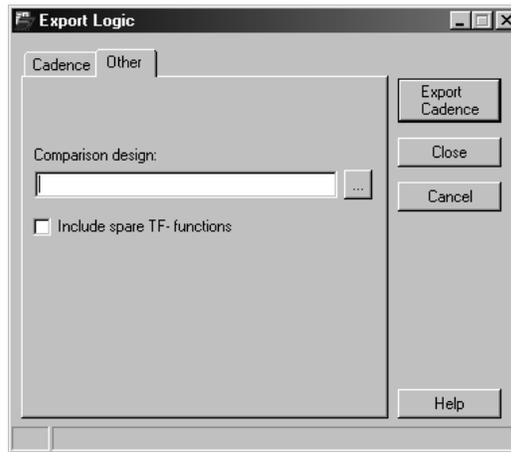
Summary

In order to successfully run backannotation for a third-party netlist, you must have a design saved on disk to compare against the current design. Enter this name in the Comparison Design field located in the Options folder tab. This means that you need to save a version of the design to disk before any backannotation type changes are made to your design. These types of changes consist of pin and gate swapping or reference designator renaming and so on.

More Information

File > Export > Logic creates a *<design>.baf* file from the active board. This file contains reference designator assignments (after gate/pin swap, or reference designator rename) indicating changes that may have occurred. Ensure that the Third Party toggle is set.

The optional Include Spare TF–Functions lets you include spare gates in the output file. Spare gates will appear at the end of the backannotation file.

Note

You must have saved a version of the design before ANY type of backannotation changes can be made.These types of changes are pin swapping, gate swapping, or reference designator renaming.

Labs

◆ Lab: Allegro to Concept Backannotation

- Backannotate changes made in the Allegro physical layout to the Concept logical schematic.

◆ Lab: Allegro to Capture Backannotation

- Backannotate changes made in the Allegro physical layout to the Capture logical schematic.

◆ Lab: Allegro Backannotation to a Third-Party Schematic Capture Tool

- Backannotate changes made in the Allegro physical layout to a third-party logical schematic.

More Information

The following labs will allow you to:

- Familiarize yourself with the process and steps required to backannotate your design to a Concept schematic. You should only perform this lab if you used Concept as your schematic input.

- Familiarize yourself with the process and steps required to backannotate your design to a Capture schematic. You should only perform this lab if you used Capture as your schematic input.

- Familiarize yourself with the process and steps required to backannotate your design to a third-party schematic system. You should only perform this lab if you used third party as your schematic input.

Lab 12-2:   Allegro to Concept Backannotation

Objective: Learn to create backannotation files and incorporate them into the Concept schematic.

You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.

Note

This lab is for designs that were created from Concept logic only! **Do not perform this lab** if your design was created from a Capture schematic or a third-party netlist.

1. Minimize the Allegro window.

2. Start the Project Manager and open *project1.com*.

3. From the Project Manager window, click **Design Sync > Import Physical**.

    The Import Physical form opens.

4. If necessary, change the settings to match the following:
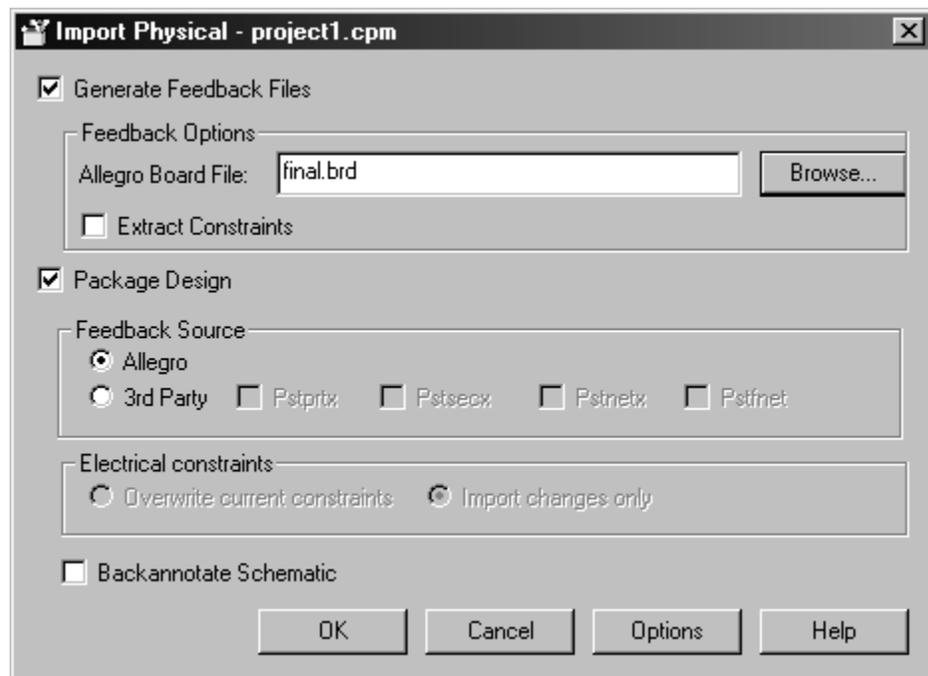
5. Click **OK** to begin generating feedback files.

6. A message appears, asking if you want to view the results. Unless you are extremely curious, click **No**.

    Feedback files are generated for Concept; however, one more procedure must be completed to actually make changes to the schematic.

7. In the Program Manager window, click **Design Entry**.

The Concept schematic window opens.

8. From the Concept top menu, choose **Tools > Back Annotate**.

A Backannotation form appears with the default file selected.

9. Click **OK**.

All pages of the schematic are updated. Lower levels of the schematic hierarchy are updated as well. After updating has occurred, your schematic may show a view at some low level in the hierarchy. If this is the case, you can use the large **Return** arrow icon to get back to the top level pages of the schematic.

10. Choose **File > Save All** in the Concept top menu.

11. Close the Concept window by selecting **File > Exit**.

12. Close the Project Manager window by selecting **File > Exit**.

13. Reopen the Allegro window.

🛑 **End of Lab**

Lab 12-3:   Allegro to Capture Backannotation

Objective: Learn to create backannotation files for the Capture schematic package.

You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.

Note

This lab is for designs that were created from a Capture schematic only! **Do not perform this lab** if your design was created from a Concept schematic or a third-party netlist.

1. Choose **File > Export > Logic**.

2. Select **Capture** in the Logic Type folder tab if it is not currently selected.

3. In the Export to directory field, browse to the *project2* directory.

4. Click **Export Cadence**.

   The feedback files *pinview.dat*, *compview.dat*, *netview.dat*, and *funcview.dat* are created. These files can be used in the Capture backannotation process.

5. Select **Close** to close the Export Logic form.

End of Lab

Lab 12-4:   Allegro Backannotation to a Third-Party Schematic Capture Tool

Objective: Learn to create backannotation files for a third-party schematic package.

You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.

1. Choose **File > Export > Logic**.

2. Select the **Other** Folder tab.

3. In the Comparison design field, either manually enter or use the browse button to select *placed.brd*.

4. Select the Include spare TF_functions option.

5. Select **Export Cadence**.

   The file *final.baf* is created. You can use the File Viewer to look at this file.

6. Select **Close** to close the Export Logic form.

STOP **End of Lab**

Lesson 13: Preparing the Board design for Manufacturing

Learning Objectives

◆ Generate and edit silkscreen layers.

◆ Use reports available in Allegro.

◆ Set up the design file for artwork.

◆ Preview Gerber files before plotting.

◆ Generate drill symbols and a drill legend for a fabrication drawing.

◆ Create penplot files for an HP plotter.

◆ Output a drill file used for drilling the board holes in manufacturing.

Summary

In this section you will learn more about preparing your design for post processing and will learn how to generate the required outputs. This will include creating silkscreens, generating reports, setting up for artwork, creating artwork files and creating NC files.

Design Layout Process
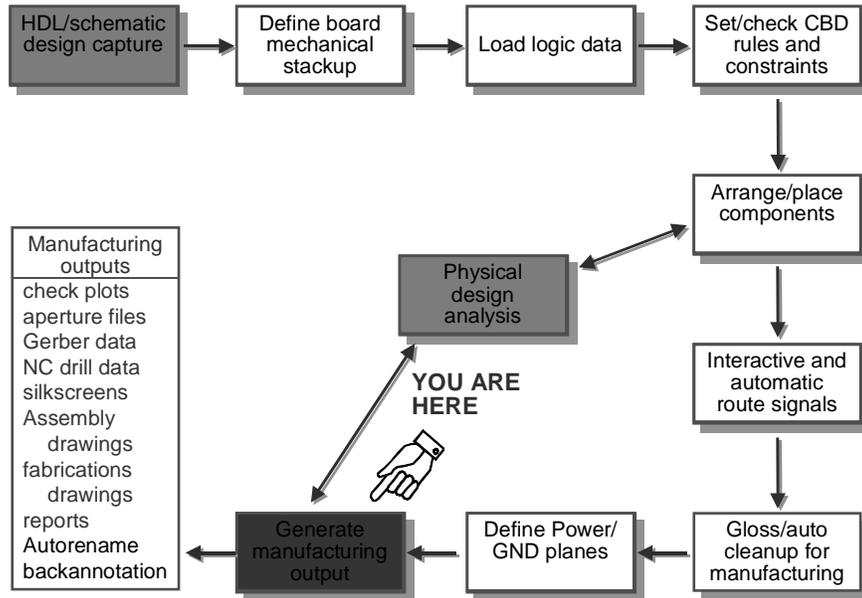
More Information

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. You will now learn the steps and processes required to generate the standard output files to be delivered to manufacturing.

Creating Silkscreens
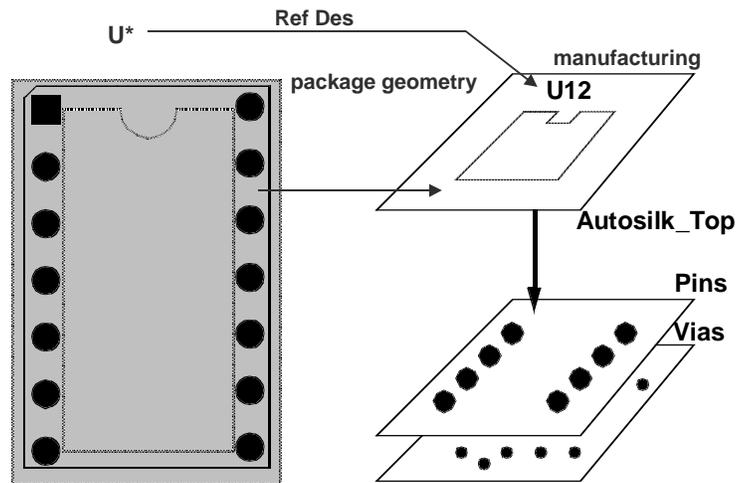
More Information

You access silkscreen mode by selecting **Manufacture > Silkscreen** from the text menu.

You can generate a silkscreen as a composite of the graphics from the following classes:

- BOARD GEOMETRY
- COMPONENT VALUE
- DEVICE TYPE
- PACKAGE GEOMETRY
- REF DES
- TOLERANCE
- USER PART NUMBER

Each of the classes has SILKSCREEN_TOP and SILKSCREEN_BOTTOM subclasses that you can use to generate silkscreens. This process first copies all of the selected silkscreen graphics to the MANUFACTURING class on either the AUTOSILK_TOP or AUTOSILK_BOTTOM subclasses. Many standards say to void soldermask of any silkscreen image. If a silkscreen line or arc crosses a pad or hole, the portion of the line or arc crossing the pad is automatically trimmed away. If a text string crosses a pad, the text is usually moved away from the pad.

If a text string cannot be moved to avoid a violation of a pad, a warning is recorded in the log file (*autosilk.log*). This warning identifies the coordinates and contents of the text string, as well as the side of the design where the violation occurs.

Creating Silkscreens—Menu

Manufacture > Silkscreen
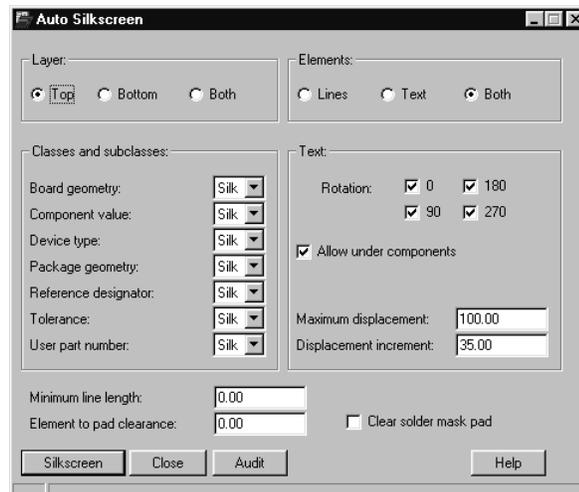
More Information

The options in the Auto Silkscreen form are:

Layer buttons specify the side of the design on which to generate the silkscreen.

Elements buttons specify whether lines, text, or both are processed. Only selected elements are erased from the specified AUTOSILK subclass and regenerated. Any elements that are not selected are untouched.

Classes and Subclasses fields define the Allegro classes where the Auto Silkscreen process looks for silkscreen graphics. For each of the classes listed on the parameter form, you can choose one of the following:

- **Silk**: only copies graphics from the SILKSCREEN subclass.
- **None**: specifies that nothing is taken from the class.
- **Any**: first uses the SILKSCREEN subclass. If nothing is found in the value you select, the ASSEMBLY subclass is used.

Text fields determine how text is (rotated) displayed on the silkscreen.

Maximum Displacement specifies in user units the maximum distance in any direction that silkscreen text strings can be moved from their original location.

Minimum Line Length specifies the minimum length of any line segment allowed on an AUTOSILK subclass. If trimming lines around pads produces segments shorter than the specified value, they will be removed. The default is 0 (no segments removed).

Element to Pad Clearance specifies in user units the amount of space to be left between silkscreen elements and the edges of pads. You can specify the clearance to the Regular pad or the Soldermask pad. Use the "Clear solder mask pad" option to specify the latter.

Clear solder mask pad specifies that when lines are being clipped or text is being moved, the soldermask pad will be used for determining the pad size rather than the regular top or bottom pad.

Incremental Update of Silkscreens

- There must be at least one run of the autosilk process for incremental silkscreen updates to occur.
- After incremental silkscreen mode is in effect, the following occurs:
  - If a component is moved, its old silkscreen will be removed and the new silkscreen will be generated to properly clear around pins and vias.
  - If a via is added, any silkscreen that is too close will be updated as required.
  - If a via is deleted, any silkscreen that was "clipped" because it was too close will be added back.
- When in incremental mode, any operation that results in a silkscreen error will only display a warning in the Allegro command area that a silkscreen failure occurred. To see the actual error, you must use the silkscreen Audit feature

NOTE: Running Refresh Symbol may cause both the original silkscreen layers AND the Autosilk layers to be re-generated.

More Information

The Silkscreen Incremental mode is only enabled after using the **Manufacture > Silkscreen** command.When moving or replacing parts in the incremental mode, the autosilk silkscreen is generated based upon the symbol's current silkscreen definition. Therefore, in general, the autosilk layer should not be manually edited. Instead, the original silkscreen subclass should be modified so that whenever any parts are moved, the correct autosilk information will be automatically generated. This includes both line and text information.

When you are either dumping the libraries or creating a clipboard, the autosilk information WILL NOT be created. Only the symbol's original silkscreen will be used.

Generating Reports
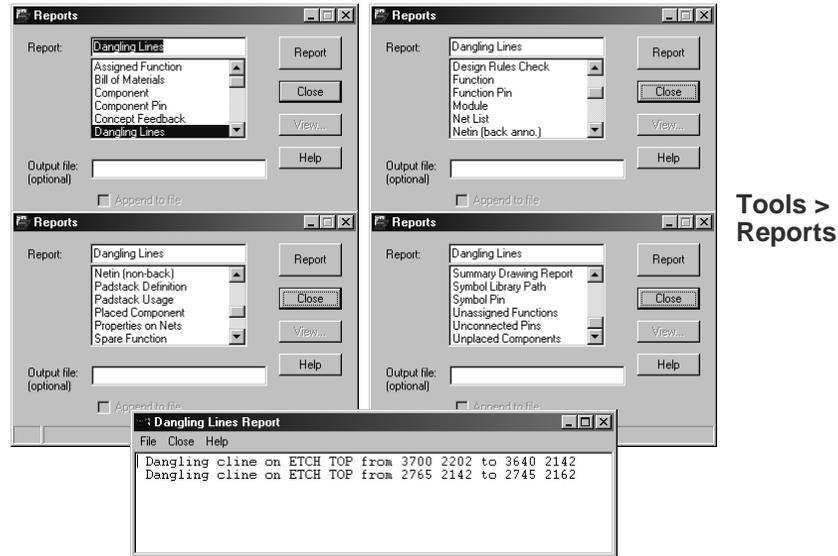
Tools > Reports

More Information

Allegro provides many predefined reports that can be run from within the current design. Select the **Tools > Reports** option from the top menu to display the Reports form. To choose a report to be generated, use the scroll bar on the right side of the Report field and then select the desired report. Select the **Report** button to run the specified report. After the report has been created, a window appears showing your report. You can save the report to a file from the displayed window by selecting **File > Save As** and specifying a file name in the Save window. If you wish to save the report to a file and NOT have the report shown in Allegro, specify a file name in the Output File Name field of the Reports form. Select **Close** to close the main Reports window.

When generating reports to a file, by default each time you run the report, it overwrites the previous version. The **Append to file** option will append the latest version of the report to the end of a pre-existing file.

Labs

◆ Lab: Creating Silkscreens

    ■ Generate and edit silkscreen layers.

        ● Set visibility.

        ● Execute the autosilk program.

        ● Edit the silkscreen.

◆ Lab: Creating Reports

    ■ Use reports available in Allegro.

More Information

The following labs will allow you to:

■ Familiarize yourself with the process and steps required to automatically and manually create and edit the silkscreen.

■ Familiarize yourself with the process and steps required to generate reports.

Lab 13-1:   Creating Silkscreens

Objective: Learn to generate and edit silkscreen layers.

Setting Visibility

Before you proceed, turn ON the drawing layers that display the silkscreen information.

1. Choose **Display > Color/Visibility** from the top menu.

2. Select the **Manufacturing** group.

3. Scroll through the list to find **AUTOSILK_TOP**.

4. Turn ON the visibility button for the AUTOSILK_TOP subclass.

5. In the Color Pad, select the color white, and assign it to the AUTOSILK_TOP layer.

6. Select the **Geometry** group.

7. Turn OFF the visibility button for the PACKAGE GEOMETRY class, ASSEMBLY_TOP and ASSEMBLY_BOTTOM layers.

8. Select the **Components** group.

9. In the REF DES subclass, toggle **ALL** subclasses OFF.

10. Click **OK** to close the Color and Visibility form.

The display is ready for silkscreen generation.

Executing the Autosilk Program

1. Choose **Manufacture > Silkscreen** from the top menu.

The Auto Silkscreen parameter form appears.

2. Set the following parameters:

Layer:	Top
Elements:	Both

CLASSES and SUBCLASSES

Board Geometry:	None
Component Value:	None
Device Type:	None
Package Geometry:	Silk
Reference Designator:	Any
Tolerance:	None
User Part Number:	None

TEXT

Rotation:	0,90
Allow Under Components:	Off
Maximum Displacement:	200
Displacement Increment:	25
Minimum Line Length:	10
Element to Pad Clearance:	10
Clear Solder mask pad:	Off

3. Click **Silkscreen**.

The automatic silkscreen program executes.

If the program failed to place any silkscreen reference designators legally (not under components, and away from pads and vias), the number of occurrences is also shown. Each reference designator that failed to meet these requirements is listed in the *autosilk.log* file.

4. Choose **File > Viewlog** from the top menu.

The *autosilk.log* file is displayed. Use the scroll bar to review this file.

5. Click **Close** to exit the log file.

6. Zoom in to review the resulting silkscreen.

Notice how the device outlines are broken where they intersect pads and vias. Also note the difference in refdes text sizes. This is controlled by the text block that was used when the refdes labels were added to the package symbols.

Editing the Silkscreen

1. Choose **Edit > Move** from the top menu.

2. Set the Find Filter so that only **Text** is ON.

3. Click on a reference designator.

It is attached to your cursor.

4. Click to place the refdes in a new location.

You are still in move mode.

5. Click on the refdes again.

6. Right click and choose **Rotate** from the pop-up menu.

7. Click left to select a new rotation for the text.

8. Click to place the refdes with its new rotation.

9. Find a refdes that is too small.

10. Choose **Edit > Change** from the top menu.

11. In the Options folder tab of the Control Panel, click the **Text Block** button. Make sure no other options are ON.

12. In the Options folder, select the Text Block data field and enter:

4

This will give you a text size of 63 mils.

13. Set the Find Filter so that only **Text** is ON.

14. Click on the refdes text to change its size.

15. Right click and choose **Done** from the pop-up menu.

16. Choose **File > Save** from the top menu.

A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

17. Click **Yes** to confirm the overwrite.

The file *final.brd* is written to disk.

STOP **End of Lab**

Lab 13-2: Creating Reports

Objective: Learn to use reports.

The Allegro design tool has several reports that provide information about your design. You can print reports at any time during the processing cycle. A report menu is included.

1. Choose **Tools > Reports**.

   The Reports menu appears.

2. Scroll through the list of reports and select **Summary Drawing Report** from the pull-down list.

3. Click **Report** to generate the report.

   A Summary Drawing Report appears in a new viewing window.

4. After viewing the report, click **Close** in the Reports window to close this window.

5. Repeat this process to create a Bill of Materials, a Design Rules Check, Unconnected Pins, Unplaced Components, or any other type of report you wish.

6. Click **Close** to close the Reports menu.

STOP **End of Lab**

Creating Checkplots

File > Plot   **This menu varies, depending on your system's printer/plotter.**

(NT)

(UNIX)
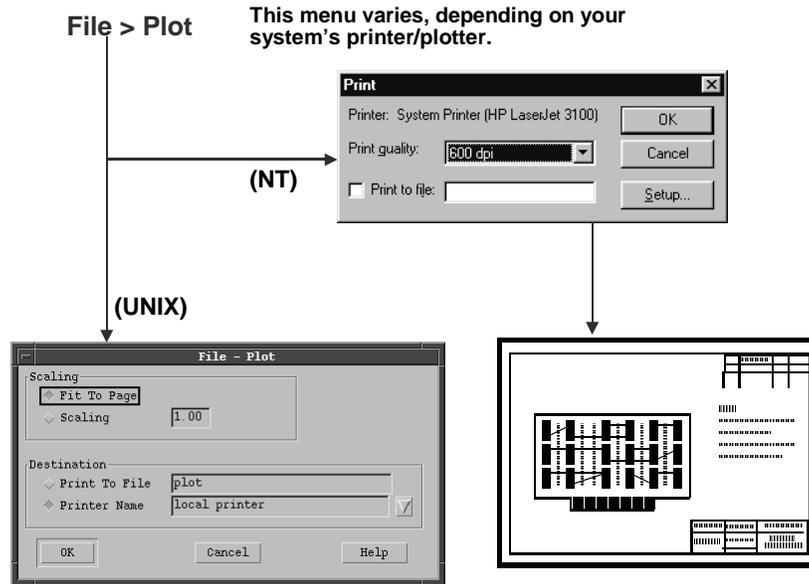
More Information

To create a hard copy from within Allegro, select the **File > Plot** option from the text window. The standard print form is displayed. Whatever is displayed in your current Allegro work area is what will be plotted.

Generating Artwork

Input files needed   **Output files created**

Allegro Design File (.brd)   **Top.art**
                                          VCC.art
                                          GND.art
                                          Bottom.art

SilkTop
Smask_top
Top
VCC   **Gerber files**
GND
Bottom
Smask_bot   **To photoplotter**
SilkBot

Film Control
records

                                          Mylar Film

Parameter file   **Aperture file**   **Log file**

art_param.txt   art_aper.txt   photoplot.log

                       (vector only)
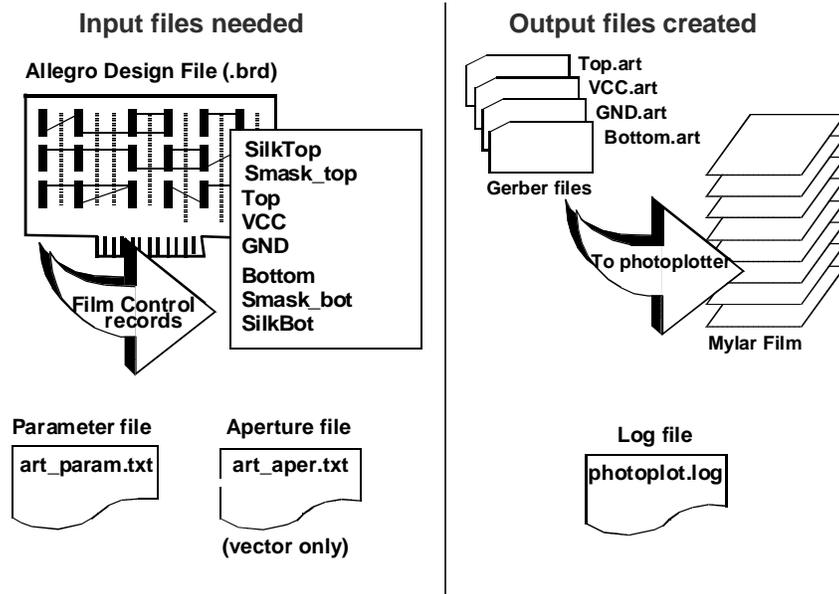
More Information

Artwork files, or Gerber files, are some of the most important items
required to manufacture a printed circuit board. The following items and
files must be created in order for Allegro to generate the artwork files.

First, **Film Control** records must exist within the Allegro design. Second,
the file *art_param.txt* should exist. If this file does not exist, then the
default parameters will be used. And third, the file *art_aper.txt* must exist if
you are NOT using the 274X, Barco DPF, or MDA Gerber file formats.
These items will be discussed later.

With the preceding items defined, Allegro can create the Gerber files for
the design. The Gerber file names created will be the film control record
name appended with the string *.art*. Along with the Gerber files, a log file
titled *photoplot.log* will be created. It is very important to check this log
file to ensure all Gerber files have been created successfully.

Artwork Parameters
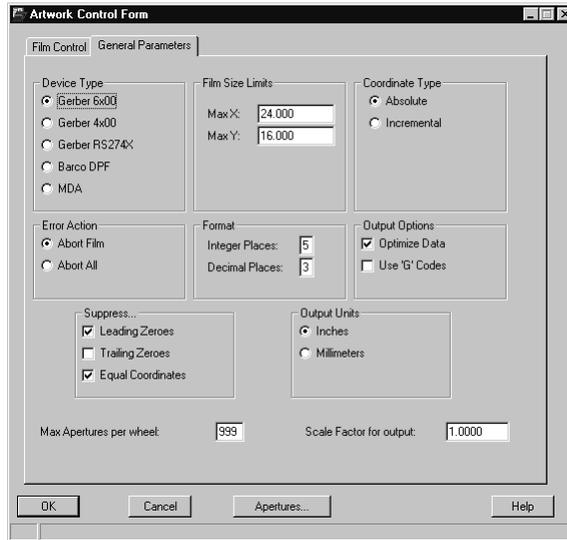
More Information

To display the Artwork Control form, select **Manufacture > Artwork** from the top menu. Select the **General Parameters** tab to bring to the front the Artwork Parameters section of the form.

The parameter form displays the default settings if no *art_param.txt* file exists in your ARTPATH (in the env file). To control artwork parameters for all users, set the ARTPATH variable to the location of an existing parameter file.

Standard Artwork Parameters

More Information

The portion of the form shown contains the standard parameters that you can set for all five photoplotter model types supported by Allegro software. The other portion (shown later) of the parameters form shows different parameters and default settings, depending on your Device Type (photoplotter model) selection.

◆ **Device Type** fields specify the photoplotter model.

◆ **Film Size Limits** fields specify the dimensions of the film used by the photoplotter. If there are elements that plot outside the boundaries, a warning is issued in the log file.

◆ **Error Action** specifies the action taken when an error is found during processing (such as an undefined aperture, and so forth). All errors are written to the log file.

◆ **Format** specifies the number of integer places and the number of decimal places in the output coordinates (range is from 0 to 5). Gerber format should reflect your design accuracy settings. For example, if design units are mils, and accuracy is set to 1 (sub-mil values), then make your Gerber format accurate to four decimal places (output in inches).

◆ **Scale Factor for Output** (not shown) scales all entries in the Gerber file.

Artwork Parameters—Device Dependent

**Gerber 6x00 and 4x00**

Gerber RS274X, Barco and MDA
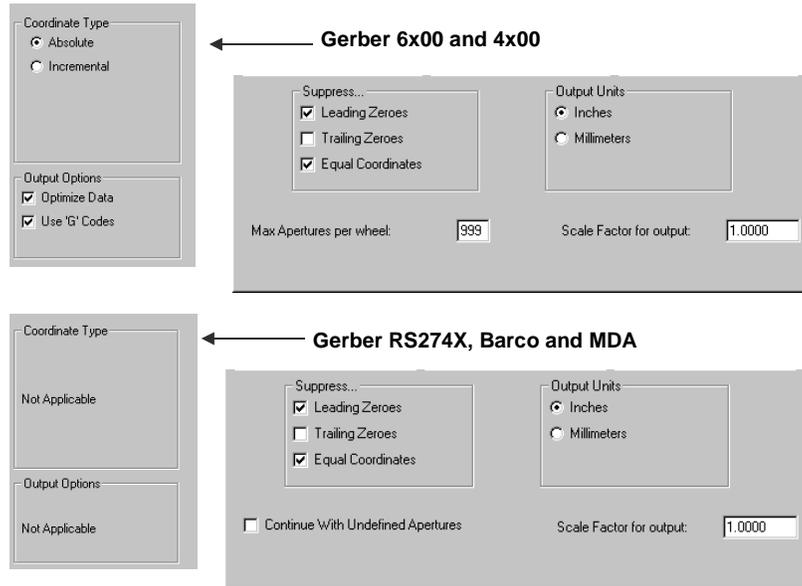
More Information

Device-Dependent Parameters

◆ **Coordinate Type** specifies whether the photoplot coordinates are always the absolute distance from the drawing origin (Absolute) or the relative distance from the last coordinate (Incremental). Not applicable to Barco DPF.

◆ **Suppress** controls whether the Allegro tool writes leading or trailing zeroes, or equal coordinates in the Gerber data file. You cannot suppress both leading and trailing zeroes. Selecting Equal Coordinates reduces the size of the Gerber data file. Not applicable to Barco DPF.

◆ **Output Units** specify the output units as either inches or millimeters (also mils for Barco DPF).

◆ **Output Options** are miscellaneous parameters (not applicable to Gerber RS274X, MDA or Barco DPF devices).

◆ **Optimize Data** sorts coordinates to minimize photo-head travel time. Laser plotters optimize the data at plot time, making this step unnecessary for artwork.

◆ **Use 'G' Codes** specifies G codes in the Gerber data. Gerber data uses G codes to describe an upcoming process (for example, prepare to receive x, y coordinates, prepare to select aperture, or prepare to flash aperture). Gerber 4x00 photoplotters require G codes (default for that device). Gerber 6x00 plotters do not need G codes.

◆ **Max Apertures per Wheel** specifies the maximum number of apertures the photoplotter wheel uses. You can enter a value between 1 and 999. If your layout uses more than the number specified, the Allegro software writes a warning to the log file. For Gerber 4x00, 6x00 only.

◆ **Continue With Undefined Apertures** tells the Allegro program what to do when it cannot find a definition for a flash aperture in the padstack. For use with Gerber RS274X, MDA, and Barco DPF raster formats only.

The Aperture File
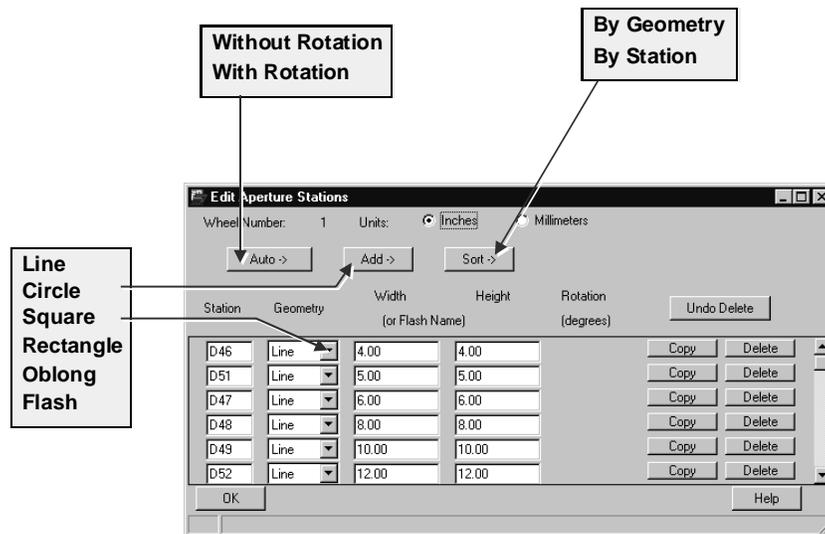
More Information

If you have chosen to use a vector format, which is either the Gerber 6x00 or Gerber 4x00, you must define an aperture wheel. To create an aperture wheel, select the **Apertures** button located at the bottom of the Artwork Control form. An Edit Aperture Wheels form will appear (not shown). Select the **Edit** button for wheel 1, and the Edit Aperture Stations form will appear.

To automatically generate all the apertures required for your current design, select the **Auto** button. You will have two options for automatic generation, one with rotation and one without rotation. The option for With Rotation specifies generation of a different aperture entry for all flashed pads at all rotations used in the design. The Without Rotation option specifies that only a 0-rotation aperture entry will be created in the aperture wheel.

You can also manually add individual aperture entries by selecting the **Add** button and then selecting the appropriate type of aperture to create. When you create apertures manually, you will also have to manually enter in the station number. You can also sort the aperture wheel based upon the station number or the type of aperture. When you select **OK** at the bottom of the form, the apertures are written to the file *art_aper.txt*.

Film Control
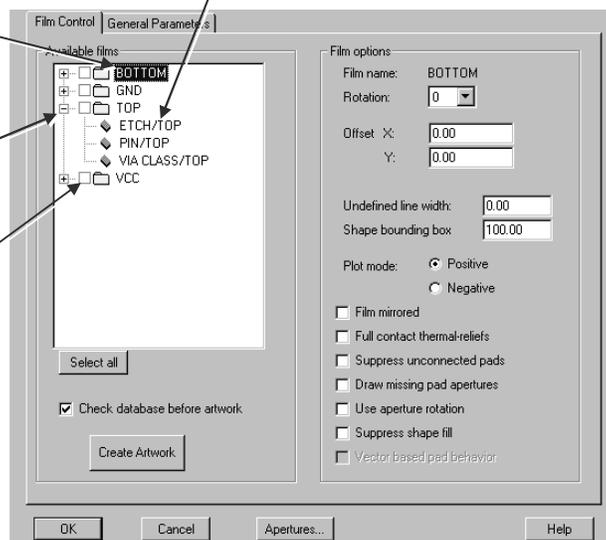
More Information

The film control records define the artwork files that will be created, as well as the contents of those artwork files. The film control records are stored internally in the Allegro design file. The **Film Control** folder tab is where you specify the film control records. The first time you access this form, you will have one film control record for each etch subclass of the design.

Each film control record will contain the classes Etch, Pin and Via for that subclass. To see the class and subclass pairs that are defined for a film control record, select the plus sign to the left of the film control record name.

To add or delete class and subclass pairs to or from the film control record, select one of the current class and subclass pairs with the right mouse button to display a context-sensitive menu.

To add a film control record, select any current film control record name with the right mouse button and select **Add** from the context-sensitive menu. You will be prompted to enter the name of the new film control record. After you enter the new film control record name and select **OK**, the new film control recorded is added. The class and subclass pairs that are currently visible at the time the new film control record is added will be the contents of the new film control record.

To delete a film control record, select the name of the film control record with the right mouse button and select **Cut** from the context-sensitive menu.

Film Options
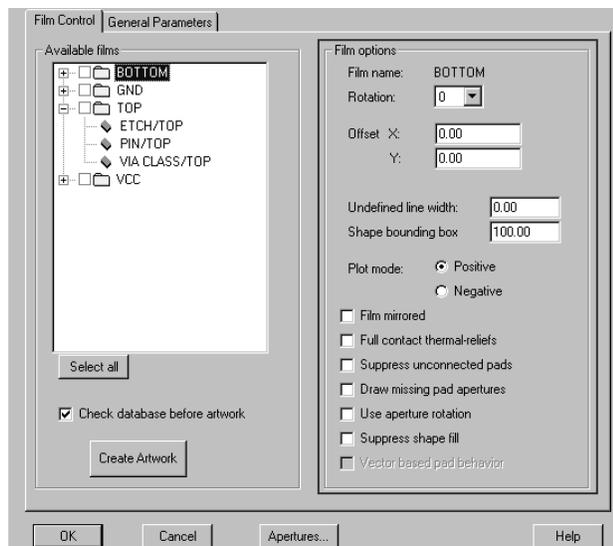
More Information

The Film Options form further describes each film control record. View film options for a film control record by selecting the film control record name with the left mouse button.

- **Film Name** displays the Gerber data file name.
- **Rotation** specifies in degrees the rotation of the plotted film image.
- **Offset X Y** shifts the positions of the photoplot coordinates. You can enter positive or negative values in these fields.
- **Plot mode** specifies positive or negative artwork. This should always be set to positive except for negative planes.
- **Undefined Line Width** specifies the photoplotted width of any line that has a zero width in the Allegro layout (for example, text, assembly and silkscreen lines).

◆ **Film Mirrored** mirrors the artwork about the Y axis.

◆ **Full Contact Thermal-Reliefs** specifies no thermal relief flash for pins and vias with negative planes.

◆ **Suppress Unconnected Pads** will not plot the pads of pins and vias that have no connections (for flashing "used pads only" on inner layers).

◆ **Draw Missing Pad Apertures** substitutes another aperture in the aperture list and uses it to draw the pad. This feature will not resolve missing flash names. This button does not appear in raster-based parameter forms.

◆ **Use Aperture Rotation** means that the Gerber data can use apertures in the aperture list that have rotation information defined for them (for example, flash names). This button does not appear in raster-based parameter forms.

Adding a Photoplot Outline

x, y origin of Gerber data (only needed for vector)

**MANUFACTURING/PHOTOPLOT_OUTLINE**
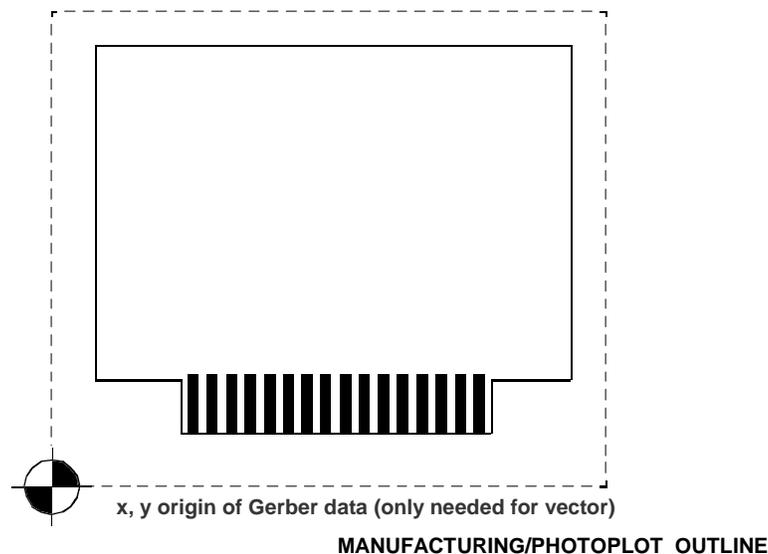
More Information

For vector-based artwork, Allegro uses the lower left corner of the drawing extents as the origin of the Gerber file. If you want a different origin for the Gerber file, you can draw a rectangle on the CLASS manufacturing, SUBCLASS photoplot_outline. The lower left corner of this rectangle will now be the origin of the Gerber file. Note that only elements contained entirely inside the rectangle will be included in the Gerber file. Any data that is not inside the rectangle will not be included.

For raster-based artwork, the board origin is the origin of the Gerber file.

Generating Gerber Files
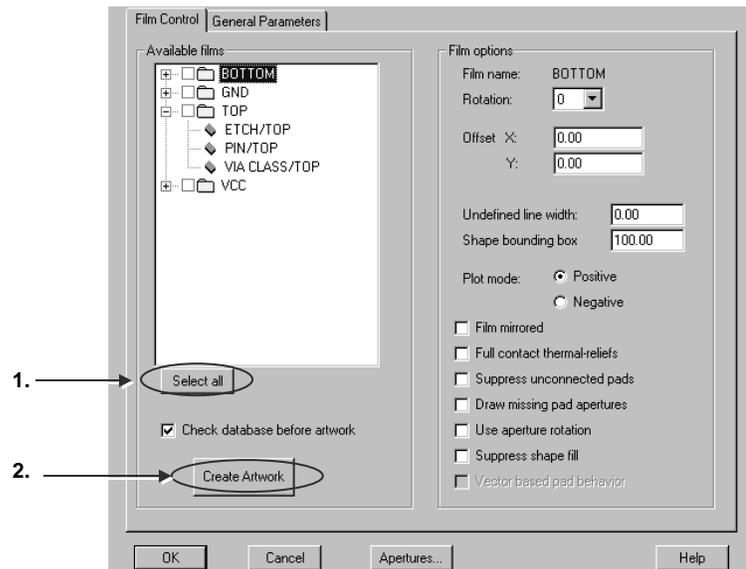

More Information

After you have specified the artwork parameters, generated an aperture list (if required), and created all artwork film control records, you are ready to create your artwork files. To identify which artwork files should be generated, either select the blank box immediately to the left of the film control record name for each artwork file to be created, or choose the **Select All** button to have all artwork files generated. Select the **Create Artwork** button to create the artwork files.

Note

Remember, all artwork files will be created on disk with a file name of the film control record name, appended with the string *.art*. Also, remember to check the log file *photoplot.log*.

Viewing Gerber Files
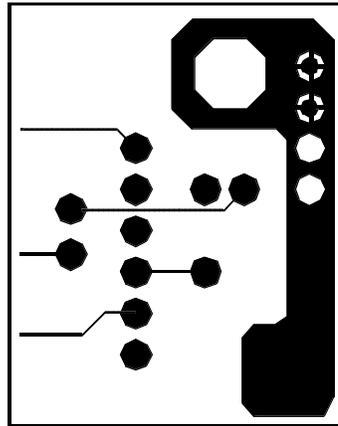
Positive (copper = black)   **Negative (copper = clear)**
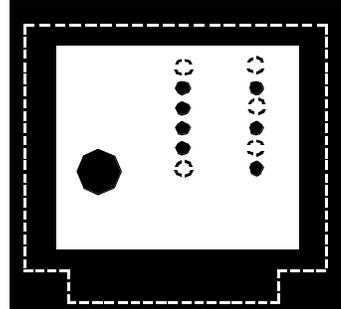
More Information

You can load Gerber files into Allegro by selecting the **File > Import > Artwork** option from the top menu. If you are using a vector format artwork file, you will need the Allegro aperture file and the Allegro parameters file. The data loaded will be of a graphical nature only. No signal intelligence will be associated with the graphics.

Labs

- ◆ Lab: Creating Artwork Files
  - ■ Set up the design file for artwork.
    - ● Set up film control records.
    - ● Create new film records.
    - ● Create the soldermask top film control record.
    - ● Create the soldermask bottom film control record.
    - ● Set manufacturing file parameters.
    - ● Create an aperture list.
    - ● Run DRC.
    - ● Save the design file.
    - ● Create the manufacturing files.
- ◆ Lab: Viewing Gerber Files
  - ■ Preview Gerber files before plotting.

More Information

The following lab will allow you to:

- ■ Familiarize yourself with the process and steps required to set up your design for artwork and to create the artwork files.

■ Familiarize yourself with the process and steps required to load gerber files into Allegro.

Lab 13-3:   Creating Artwork Files

Objective: Learn to set up the design file for artwork.

In this lab, you will learn how to define the artwork layers required for photoplotting a design. You will learn about parameter and aperture files that are used to create the photoplot files.

Setting Manufacturing File Parameters

1. Choose **Manufacture > Artwork** from the top menu.

   The Artwork Control form opens. Notice that there are four entries in the Available Films window of the Artwork Control form. There is one entry for each of the etch subclasses of your design.

2. Select the **General Parameters** folder tab in the Artwork Control Form.

   This form specifies the plotter type, film size, and format of the manufacturing data.

3. You will create Gerber files in the RS274X format. Update the format parameters as follows:

Device Type:	RS274X

   Format

Integer Places:	2
Decimal Places:	5

   When you close the Artwork Control form, the parameter settings will be written to a file called *art_param.txt* in the working directory.

Setting Up Film Control Records

Each layer for which you want to create artwork must be entered into an Artwork Film Control table. By default, the Allegro software will create a film control record for each of the etch subclasses in the design.

1. Select the **Film Control** folder tab in the Artwork Control Form.

   This form specifies which artwork files are to be created and which objects in the Allegro database constitute each artwork file.

2. Select the plus + sign to the left of the BOTTOM entry in the Available Films window of the Artwork Control form.

   The BOTTOM film control record expands to display the class/subclass entries that will be included in the manufacturing file for this artwork film. By default, the Allegro software includes the ETCH, PIN, and VIA class for each of the etch subclasses.

The Film Options section of the Artwork Control form displays the current options set for the selected film control record.

3. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

4. Select the **GND** film control record in the Available Films section of the Artwork Control form (select on the word GND).

The Film Options section of the Artwork Control form now shows the film options for the GND film record.

5. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

6. Select the **TOP** film control record in the Available Films section of the Artwork Control form (select on the word TOP).

The Film Options section of the Artwork Control form now shows the film options for the TOP film record.

7. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

8. Select the **VCC** film control record in the Available Films section of the Artwork Control form (select on the word VCC).

The Film Options section of the Artwork Control form now shows the film options for the VCC film record.

9. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

10. Verify the Plot Mode field is set to **Negative** in the Film Options section of the Artwork Control form.

Creating New Film Control Records

You will also need to create artwork files for your soldermask layers and your silkscreen layer. You need to create a film control record for each of these. By default, when you create a new film control record, all currently visible classes and subclasses are added to the film control record.

Note

Do not close the Artwork Control Form until told to do so.

1. Choose **Display > Color/Visibility** from the top menu.

2. Use the Global Visibility field to turn OFF all classes and subclasses.

3. Set the Group field to **Manufacturing**.

4. Turn on the **MANUFACTURING** class, **AUTOSILK_TOP** subclass and click **OK** to close the Color and Visibility form.

5. Use the right mouse button to select the last film control record name in the Available Films section of the Artwork Control form and access a context-sensitive menu.

6. Choose **Add** from the menu.

   A text form opens asking for the name of the new film.

7. Enter a name of **SILK_TOP** and select the **OK** button.

   A new film control record is added.

8. Select the **SILK_TOP** film control record in the Available Films section of the Artwork Control form (select on the word SILK_TOP).

   The Film Options section of the Artwork Control form now shows the film options for the SILK_TOP film record.

9. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

Creating the Soldermask Top Film Control Record

1. Choose **Display > Color/Visibility** from the top menu.

2. Use the Global Visibility field to turn OFF all classes and subclasses.

3. Set the Group field to **Stack-Up**.

4. Turn on **PIN/SOLDERMASK_TOP** and **VIA/SOLDERMASK_TOP**.

5. Click **OK** to close the Color and Visibility form.

6. Use the right mouse button to select the **SILK_TOP** film control record in the Available Films section of the Artwork Control form to access a context-sensitive menu.

7. Select **Add** from the menu.

   A text form opens, asking for the name of the new film.

8. Enter a name of **SOLDER_TOP** and click **OK**.

   A new film control record is added.

9. Select the **SOLDER_TOP** film control record in the Available Films section of the Artwork Control form (select on the word SOLDER_TOP).

   The Film Options section of the Artwork Control form now shows the film options for the SOLDER_TOP film record.

10. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

Creating the Soldermask Bottom Film Control Record

1. Choose **Display > Color/Visibility** from the top menu.

2. Use the Global Visibility field to turn OFF all classes and subclasses.

3. Set the Group field to **Stack-Up**.

4. Turn on **PIN/SOLDERMASK_BOTTOM** and **VIA/ SOLDERMASK_BOTTOM**.

5. Click **OK** to close the Color and Visibility form.

6. Use the right mouse button to select the **SOLDER_TOP** film control record in the Available Films section of the Artwork Control form to access a context-sensitive menu.

7. Select **Add** from the menu.

   A text form opens, asking for the name of the new film.

8. Enter a name of **SOLDER_BOT** and select the **OK** button.

   A new film control record is added.

9. Select the **SOLDER_BOT** film control record in the Available Films section of the Artwork Control form (select on the work SOLDER_BOT).

   The Film Options section of the Artwork Control form now shows the film options for the SOLDER_TOP film record.

10. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

11. Select **OK** to close the Artwork Control Form.

Running DRC

Before you create artwork files, make sure your design has no DRC errors.

1. Choose **Setup > Drawing Options** in the top menu.

   The Drawing Options form appears. In the DRC folder tab, the Status section might display an "Out Of Date" message

2. Click **Update DRC**.

   The Allegro message area reports:

   Performing DRC. Please wait...

3. When the DRC check is completed, click **OK** to close the Drawing Options form.

4. If any DRCs are created, they should be corrected before creating artwork. Turn the DRC class ON (under the Stack-Up group) to locate the DRCs.

Saving the Design File

1. Choose **File > Save** from the top menu.

   A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

2. Click **Yes** to confirm the overwrite.

   The file *final.brd* is written to disk.

Creating the Manufacturing Files

1. Choose **Manufacture > Artwork** from the top menu.

   The Artwork Control form opens.

2. Select the **Film Control** folder tab in the Artwork Control form.

3. The check box to the left of each film control record controls whether a manufacturing file will be created for that record. Since you want to generate all artwork files, select the **Select All** button below the Available Films window.

4. Select the **Create Artwork** button in the Artwork Control form.

   Gerber format artwork files are written to your current working directory.

   If you wish, you can use the Windows file manager or the UNIX *ls* command to check for these files. Each artwork file has the same extension (*top.art, gnd.art, vcc.art*). These are the plot files that are used to create the film required for manufacturing the board.

5. Choose **File > Viewlog** to see the log file.

   Check to make sure all artwork files have been created successfully.

6. Click **Close** to exit the log file.

7. Click **OK** in the Artwork Control form to close the form.

STOP **End of Lab**

Lab 13-4:   Viewing Gerber Files

Objective: Learn how to preview Gerber files before plotting.

1. Choose **File > New**.

    A window appears and asks you if you want to save the *final.brd* file before creating a new design.

2. Click **Yes** to save the changes.

    The file *final.brd* is written to disk.

    The New Drawing window appears.

3. Enter the following name in the Drawing Name field:

    viewgerber

    This will create a new layout drawing called *viewgerber.brd*.

4. Click **OK** in the New Drawing window to open the new design *viewgerber.brd*.

5. Choose **Setup > Drawing Size**.

    The Drawing Parameters form opens.

6. In the Drawing Parameters form, use the scroll button in the Size field, and select **D**.

7. In the Drawing Parameters form, use the scroll button in the Accuracy field, and select **2**.

8. Click **OK** to close the form.

Creating a New Subclass for the Artwork

If you load the artwork on the Class/Subclass pair Etch/Top, all of the line draws will be seen as etch and will therefore be subject to the standard DRC settings such as line-to-line, and so forth. You will create a new subclass under the Manufacturing class to load all of the artwork into.

1. Choose **Setup > Subclasses** from the top menu.

2. Select the box next to Manufacturing.

3. In the New Subclass field, enter **ARTWORK**.

    Press the **Enter** or **Return** key after entering the new subclass name.

4. Select **OK** in the Define Subclasses form.

    You are now ready to load in your artwork.

Loading the Artwork Files into Allegro

1. Choose **File > Import > Artwork** from the top menu.

The Load Gerber form appears.

2. Set the Class field to **MANUFACTURING** using the pull-down menu.

3. Set the Subclass field to **ARTWORK** using the pull-down menu if it is not currently selected.

4. Click the **Browse** button. In the file browser window select *TOP.art*, and click **Open**.

   The entire path appears in the File Name field.

5. Click the **Load File** button.

   A rectangle now attaches to your cursor. This represents the outline of the plot you are about to place.

6. Move the cursor near the upper left area of the blank screen, then click left.

   The artwork image appears.

7. Repeat this process for the other etch layer artwork files you have created (*vcc.art, gnd.art, and bottom.art*).

8. Click **OK** to close the Load Photoplot window.

9. Zoom in to view the artwork layers.

   Notice the difference between the positive and negative image planes.

   The database for this course includes the flash symbols (*.fsm* files) that let you see flash features while viewing Gerber files in Allegro software.

   When you load an artwork layer that contains flash names (defined in your padstack data), Allegro tools use the PSMPATH to locate corresponding flash symbols. (*.fsm* files must have the same name as the flash.)

STOP **End of Lab**

Creating Fabrication Drawings

Fab Drawing

FAB NOTES:
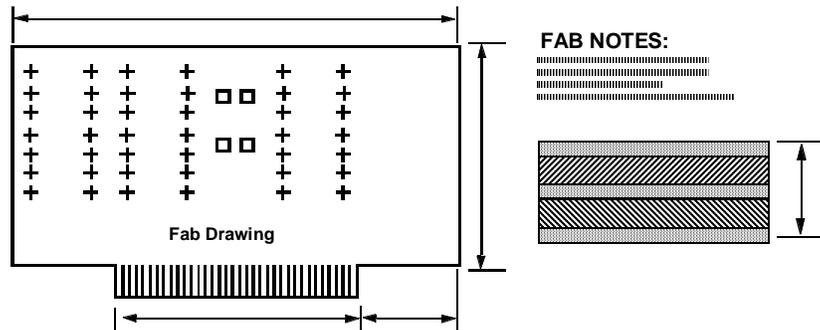
DRILL CHART			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
+	39.0	PLATED	42
▢	43.0	PLATED	4

More Information

In order to create a fabrication drawing, you will have to create your own company format and cross section format symbol, if one is required. You will also need to dimension your drawing if you have not done so in the board mechanical drawing. Select the **Manufacture > Dimension/Draft** option from the top menu to access all the available drafting and dimensioning commands. For more information on dimensioning, see the online Help files.

Drill Symbols and Legend Table

Title of drill legend
(user-specified)

The legend header and
content can be modified
by creating a custom drill
template (.dlt)

DRILL CHART			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
○	39.0	NON-PLATED	82
□	49.0	NON-PLATED	8
△	39.0	NON-PLATED	5
◇	28.0	NON-PLATED	3
○	72.0	OPTIONAL	2

FIGURE column
displays a drill
figure for each size.

SIZE column
displays the size
for each hole.

PLATED column
displays the plating
for each hole.

QTY column
displays the
quantity (total
count) of each
hole size.

More Information

Allegro's Drill Legend command automatically creates a drill legend and the drill drawing information. To execute the Drill Legend command, first make visible all pins and all vias in the design. Next, select the **Manufacture > NC > Drill Legend** option from the top menu. Fill out the Drill Legend form and select the **OK** button. The Drill Legend program runs. The program will first draw, over each hole in the design, the drill character as defined in the padstack for that hole. This drill character will be drawn on the class Manufacturing, subclass NCDRILL_FIGURE.

After a drill character has been drawn for every hole in the design, a rectangle will be attached to your cursor. This is the outside extents of the drill legend. You select with your mouse where to place the drill legend inside of your database. The legend will be drawn on the class Manufacturing, subclass NCDRILL_LEGEND. Every time the Drill Legend program is run, it deletes any previous drill legends and drill figures.

⚠ Caution

If you add, delete, or move holes, or change drill information in padstacks, you must regenerate the legend (it does not update automatically).

Generating an NC Drill File

Manufacture > NC > Drill Tape
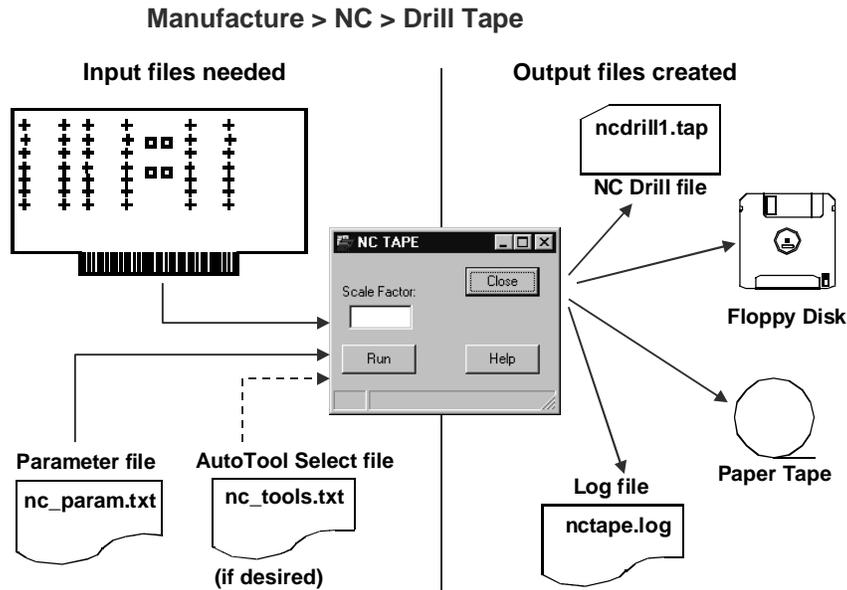
More Information

In order to generate a drill file for manufacturing, you must have a parameter file (*nc_param.txt*) that specifies the format of the drill coordinate data. If you are generating drill data for a machine that is able to perform its own drill bit selections automatically, then you will also need an *nc_tools.txt* file. The Allegro program searches the NCDPATH you specify in the environment file (env) to locate these files.

To create a parameter file, select **Manufacture > NC > Drill Parameters** from the top menu.

To create a drill file, select **Manufacture > NC > Drill Tape** from the top menu.

The nctape program reads the parameter file(s) and examines the Allegro layout drawing. It outputs a minimum of one NC drill file (*ncdrill1.tap*) and a log file (*nctape.log*).

The NC drill file contains all the coordinates for each of the hole sizes in the layout. You can copy this file to a floppy disk, or you can punch onto a paper tape.

The log file shows the parameters that were used to create the drill data, a summary of hole sizes and quantities, and any warnings or errors.

Creating the Parameters File—Paper Tape
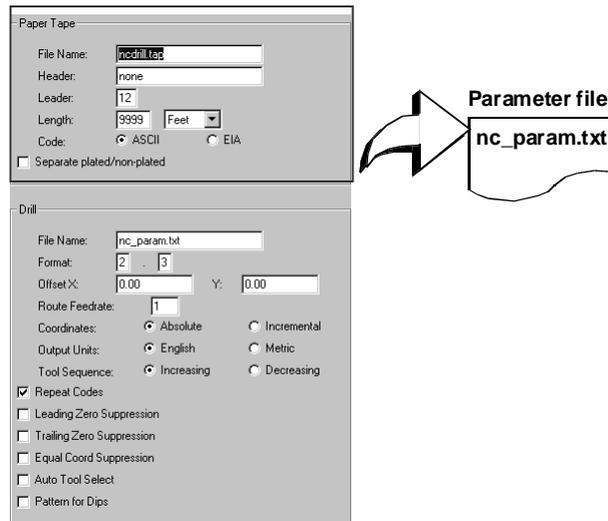
More Information

To set the parameters for the drill coordinate data, select **Manufacture > NC > Drill Parameters**.

The fields in the NC Drill/Tape parameters form are divided into two categories: Paper Tape and Drill.

The Paper Tape section of the NCDrill/Tape form contains:

◆ **File Name** specifies a name you use to construct the output text file names. These files are numbered sequentially, starting with one. The numbers are appended to the given name before any extension. If a file name extension is not specified, then *.tap* is assumed. The default value of this parameter is ncdrill. This means that the NCDRILL files created are named *ncdrill1.tap*, *ncdrill2.tap*, and so forth.

◆ **Header** specifies an ASCII header for the paper tape. The default is none.

◆ **Leader** specifies the leader length on the paper tape. The units of this value are the same as the units of the Length parameter. The default is 12 feet.

◆ **Length** specifies the paper tape length. Files that are too long to fit on the tape are broken into multiple files. The units field that follows this number toggles between Feet and Meters. This value defines the units for both Length and Leader. The default is 9999 Feet.

◆ **Code** specifies the paper tape output format. The two formats allowed are ASCII or EIA. The default is ASCII.

◆ **Separate plated/non-plated** specifies whether separate tapes are to be created for drilling plated and non-plated holes. The default puts plated and non-plated holes on the same tape.

Creating the Parameters File—Drill
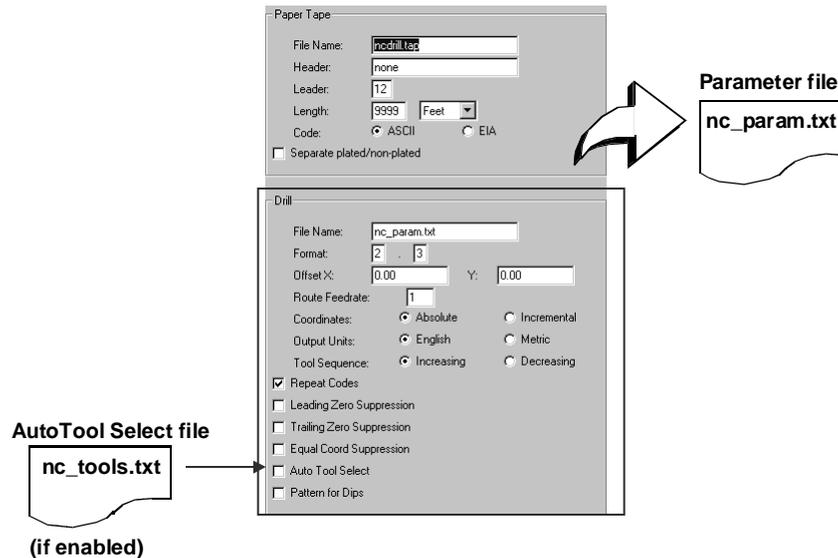
More Information

The Drill section of the NC Drill/Tape parameters form contains:

◆ **File Name** is the path name of the text file into which the values of the NCDRILL parameters are saved when you exit from the form. The name of the file must be *nc_param.txt*, but you can specify any directory path for the file (for example, */usr/library/nc_param.txt*).

◆ **Format** is the format for coordinate data in the output NCDRILL file. The default is 2.3.

◆ **Offset X: Y:** specifies an offset from the drawing origin for the coordinate data.

◆ **Coordinates** specifies whether the output coordinates are incremental or absolute.

◆ **Output Units** specifies whether the output units are English or Metric. The default is English.

◆ **Tool Sequence** specifies the tool sequence as smallest to largest drill size by default.

◆ **Repeat Codes** specifies whether repeat codes are supported by your drill machine.

◆ **Leading Zero Suppression** specifies whether the output coordinates are padded with leading zeros.

◆ **Trailing Zero Suppression** specifies whether the output coordinates are padded with trailing zeros.

◆ **Equal Coord Suppression** specifies whether equal coordinates are suppressed. The default does not suppress equal coordinates.

◆ **Auto Tool Select** specifies whether the drilling machine has an automatic tool changer. If this field is not checked, the drill pauses for manual tool changes (default). If the field is checked, you will need to create an *nc_tools.txt* file.

◆ **Pattern for Dips** specifies whether the drill supports drill patterns for standard dual in-line packages. The default does not support drill patterns for standard dual in-line packages.

Creating Assembly Drawings
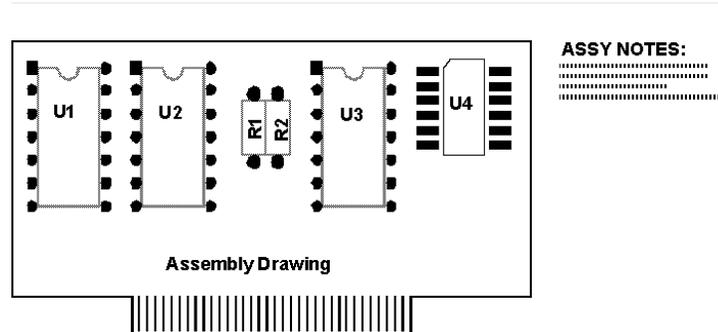
Assembly Drawing

More Information

If you started your layout from a template or master design file, you already have a drawing border (A-D size format symbol), as well as format symbols for assembly notes.

You are now ready to create a plot file for the assembly drawing. Like the photoplot process, what you see in the work area is what is included in any plot file. The various format symbols (like assy notes) need to be created with this in mind. For example, when you create an ASSY_NOTES format symbol (with the Symbol Editor), create a special layer for it (such as Manufacturing/Assynotes). When you need to create a plot file for the assembly drawing, toggle the appropriate special layers in the layout drawing to make only the assembly-related data visible.

To set visibility, select **Display > Color/Visibility** from the top menu.

For assembly drawings, you will need to toggle the appropriate layers to display package outlines, reference designators, pins, and so forth. You can also include mechanical symbols for extractors and other mounting hardware.

To create a plot for a pen or electrostatic plotter, select **File > Plot**.

Labs

◆ Lab: Creating a Drill Legend
- Generate drill symbols and a drill legend for a fabrication drawing.
  - Open the final design file.
  - Set visibility.
  - Create drill symbols and legend.

◆ Lab: Creating Fab and Assembly Drawings
- Create penplot files.
  - Create a fab drawing.
  - Create an assembly drawing.

◆ Lab: Creating an NC Drill F   ile
- Output a drill file used to drill the board holes in manufacturing.

More Information

The following labs will allow you to:

- Familiarize yourself with the process and steps required to create the drill figures and create a drill legend.

- Familiarize yourself with the process and steps required to create a fabrication and an assembly drawing.

- Familiarize yourself with the process and steps required to create the NC drill files.

Lab 13-5:   Creating a Drill Legend

Objective: Learn how to generate drill symbols and a drill legend for a fabrication drawing.

Opening the Final Design File

1. Choose **File > Open**.

   A warning is issued and you are asked whether you want to save the existing *viewgerber.brd* file.

2. Click **No** to the warning.

   A file browser window opens.

3. Select the *final.brd* file and click Open to close the browser.

   The *final.brd* file appears in the work area.

Setting Visibility

In order to generate drill symbol and legend information, you must make all pins visible. Drill symbols and legend information for routing vias are also generated, but they do not need to be visible. In this section, you will turn on the visibility for all pins and vias as well as the drawing layers that display the drill symbols and legend information.

1. Choose **Display > Color/Visibility** from the top menu.

2. Use the **Global Visibility** field to turn OFF all classes and subclasses.

3. Set the group to **Geometry**.

4. Under the BOARD GEOMETRY subclass, turn ON **OUTLINE**.

5. Under the BOARD GEOMETRY class, turn ON the **DIMENSION** layer.

6. Set the group to **Stack-Up**.

7. Under the PIN class, turn ON both **TOP** and **BOTTOM** subclasses.

8. Under the VIA class, turn ON both **TOP** and **BOTTOM** subclasses.

9. Set the group to **Manufacturing**, and turn ON the **NCDRILL_FIGURE** and **NCDRILL_LEGEND** layers.

10. Click the button under the class name **DRAWING FORMAT** to turn ON all items in that class.

11. Click **OK** to close the Color and Visibility form.

12. Choose **View > Zoom World** from the top menu.

Creating Drill Symbols and Legend

1. Choose **Manufacture > NC > Drill Legend** from the top menu.

   The Drill Legend menu appears.

2. If you want to change the Legend Title you can. Accept all remaining defaults and click **OK**.

   When processing is complete, a rectangle appears attached to your cursor, and the Allegro message area prompts you to pick a location for the legend information.

3. Place the legend data someplace on the drawing so as to not interfere with any other drawing/board data.

   The legend appears.

   The default drill legend is relatively large for this board, but you can control this by creating a custom or standard template to your liking.

   If you have filled pads turned on, you will probably not be able to see the drill figures. You will need to turn this option off in order to see the actual drill figures in your design.

4. Choose **File > Viewlog** to see the log file.

5. Click **Close** to exit the log file.

STOP **End of Lab**

Lab 13-6:   Creating Fab and Assembly Drawings

Objective: Learn to create penplot files for the an HP penplotter.

Creating a Fab Drawing

1. At the Allegro command line, enter:

   add text

2. In the Options folder tab of the Control Panel, set the Active Class and Subclass fields to **DRAWING FORMAT / TITLE_DATA**.

3. In the Options folder tab of the Control Panel, double click in the **Text Block** area, and enter:

   14

   Make sure the Rotate field is set to **0**.

4. In the Allegro work area, click in the title block (lower right corner of the drawing format), and enter your name. Right click and choose **Done**.

   If you zoom in to do this, be sure you zoom back out before going to the next step, because whatever is in the work area gets passed to the plot file.

5. At this point you can print what you have currently displayed in the Allegro screen to create a print of the fabrication drawing.

Creating an Assembly Drawing

1. Choose **Display > Color/Visibility** from the top menu.

   First you will turn OFF some of the items from the previous lab.

2. In the Geometry group, under the BOARD GEOMETRY class, turn the **DIMENSION** subclass OFF. Under the PACKAGE GEOMETRY class, turn the **ASSEMBLY_TOP** subclass ON.

3. In the Manufacturing group, turn OFF the **NCDRILL_LEGEND** and **NCDRILL_FIGURE** subclasses.

4. In the Stack-Up group, turn ON **TOP PIN** and turn **OFF BOTTOM** PIN. Turn OFF all **VIA** subclasses.

5. In the Components group, under the REF DES class, turn ON the **ASSEMBLY_TOP**.

6. Click **OK** to close the Color and Visibility form.

   The assembly drawing information is now visible.

7. If your classroom is networked to a printer, you can at this point print what you have currently displayed in the Allegro screen; otherwise, begin the next lab.

STOP **End of Lab**

Lab 13-7: Creating an NCDRILL File

Objective: Learn to create a drill file used to drill the holes during manufacturing.

1. Choose **Manufacture > NC > Drill Parameters** from the top menu.

   An NC/Drill Tape parameter form appears.

2. In the Drill section, set the Format to **2.5**

3. Click **OK**.

   The parameters are written to a file called *nc_param.txt*.

4. Choose **Manufacture > NC > Drill Tape** from the top menu.

   An NC Tape window appears.

5. Click **Run** to start the tape creation process.

6. Click **Close**.

   The drill data is extracted from the design file (*final.brd*), and the drill file (*ncdrill1.tap*) is written to disk.

7. Use the File Manager or a viewer of your choice to view the *ncdrill1.tap* file.

8. Choose **File > Viewlog** to view the *nctape.log* file that was created.

   The log file displays format information, as well as hole size and quantity data.

9. Click the **Close** button in the log file window to close the window.

10. Choose **File > Save** from the top menu.

    A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

11. Click **Yes** to confirm the overwrite.

    The file *final.brd* is written to disk.

STOP End of Lab