

A 1.8 μW 60 nV/ $\sqrt{\text{Hz}}$ Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes

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Abstract—This paper presents a low-power precision instrumentation amplifier intended for use in wireless sensor nodes. It employs a capacitively-coupled chopper topology to achieve a rail-to-rail input common-mode range as well as high power efficiency. A positive feedback loop is employed to boost its input impedance, while a ripple reduction loop suppresses the chopping ripple. To facilitate bio-potential sensing, an optional DC servo loop may be employed to suppress electrode offset. The IA achieves 1 μV offset, 0.16% gain inaccuracy, 134 dB CMRR, 120 dB PSRR and a noise efficiency factor of 3.3. The instrumentation amplifier was implemented in a 65 nm CMOS technology. It occupies only 0.1 mm² chip area (0.2 mm² with the DC servo loop) and consumes 1.8 μA current (2.1 μA with the DC servo loop) from a 1 V supply.

Index Terms—Bio-signal sensing, chopping, high power efficiency, low offset, low power, precision amplifier, wireless sensor nodes.

I. INTRODUCTION

NOWADAYS, the use of wireless sensors is opening up new applications in medical diagnostics, infrastructure monitoring, and environmental sensing [1]–[3]. In medical diagnostics, wireless sensors can be implanted to monitor bio-potentials, body temperature and other clinically relevant data; while in heating, ventilation and air conditioning (HVAC) systems, wireless sensors can be used to optimize energy distribution by, for instance, establishing patterns of building occupancy [2]. Individual wireless sensor nodes should be designed for low power consumption, small size and low cost [1], [2]. Low power consumption (in the order of tens to hundreds of microwatt) is required, since wireless sensors are typically powered by energy harvesters or by batteries, which cannot be easily replaced or recharged. Small size and low cost facilitate the use of tens or even hundreds of nodes in a wireless sensor network. Both of these requirements can be achieved by integrating the entire node on a single chip.

A wireless sensor node consists of a number of sensors, their readout electronics, and an RF front-end. Since sensor signals

are often quite small (millivolt level), the readout electronics often consists of an instrumentation amplifier (IA) that precedes an ADC [1]. Since the RF front-end is usually the most power-hungry block in a node, its efficient implementation drives the choice of the technology in which the entire node is realized. In practice, this means the use of deep submicron CMOS processes, as this results in RF front-ends with smaller area and greater power efficiency [4]–[6], while also being favorable for the implementation of ADCs and digital circuitry [7]–[9]. For full integration, the IA must then be realized in the same technology.

However, most recent IAs have been implemented in relatively mature technologies [10]–[18]. Moreover, the power consumption of the IAs in [10]–[13] is in excess of 100 μW , which is too high for use in wireless sensor nodes. Although the IAs in [14]–[18] have sufficiently low power consumption, they are optimized for bio-potential (electrocardiology (ECG) and electroencephalography (EEG)) sensing and have band-pass characteristics to reject the relatively large electrode offsets that may arise in such applications. As a result, these IAs cannot sense the DC outputs of sensors such as resistive bridges, strain gauges and thermocouples. To satisfy a variety of wireless sensors applications with minimum hardware and cost, a low power multi-purpose precision IA is needed. A promising IA topology has been reported in [14], [18], which consists of a chopped inverting opamp whose gain is set by a capacitive feedback network. This capacitively-coupled chopper topology offers rail-to-rail sensing capability, high power efficiency and high gain accuracy. However, its input impedance is defined by a switched-capacitor (SC) resistance and is limited to a few Mega ohms at typical chopping frequencies. Furthermore, the chopping ripple at its output must be filtered out by an additional low-pass filter, thus increasing the required chip area significantly. The amplifier can also be used for bio-potential sensing by employing a DC-servo loop; however, the implementation described in [14] requires large capacitors, which significantly increase its chip area. Disabling chopping also enables the use of the IA for bio-potential sensing [18]; however, this is at the expense of reduced CMRR due to capacitor mismatch.

This paper describes a precision IA with high power efficiency which can be used for accurate DC readout as well as for bio-potential sensing. Implemented in a 65 nm CMOS technology, it can be easily integrated in a wireless sensor node [19], [20]. Instead of employing traditional IA topologies such as the

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three-opamp, current feedback or resistive feedback topologies, it employs the capacitively-coupled chopper topology recently introduced in [14], [18]. In this work, a positive feedback loop (PFL) is employed to boost the amplifier's input impedance, while the chopping ripple is suppressed by a ripple reduction loop (RRL). For bio-potential sensing, a DC servo loop (DSL) establishes a high-pass characteristic [20]. In contrast with [14], the DSL employs an area-efficient very-large time constant (VLT) SC integrator [21] to define the amplifier's high-pass corner.

The paper is organized as follows. In Section II, the advantages and disadvantages of the traditional IA topologies are discussed. The capacitively-coupled chopper topology is then presented in Section III. The working principle and the implementations of the PFL, the RRL and the DSL will be described in Section IV. In Section V, experimental results will be shown and the paper ends with conclusions.

II. TRADITIONAL TOPOLOGIES

Three topologies have been traditionally used to realize IAs: the three-opamp, current feedback and resistive feedback topologies. The classic three-opamp topology [22]–[26] has high input impedance and excellent linearity. However, its power efficiency is reduced by the need for the two low-noise input amplifiers. Furthermore, the three-opamp IAs can not sense the rail since their input CM voltage must also fall within the input amplifiers' output voltage range. Current feedback IAs (CFIAs) [10]–[13] also have high input impedance. However, their gain accuracy is limited by the mismatch between their input and feedback transconductances. CFIAs can have rail-sensing capability by employing either an NMOS or PMOS-based input differential pairs. However, achieving rail-to-rail input capability as well as high gain accuracy is quite challenging, as the mismatch between their input and feedback transconductors is usually also a function of the input CM voltage [13]. The power efficiency of CFIAs is also limited by the need for the two input and feedback transconductances. The resistive feedback topology [27] is a third option. However, the value of its input resistors is a compromise between noise and input impedance. Last but not least, the closed-loop gain of the all three topologies is defined by a resistive network that loads the IA's output stage. For a 1 V output voltage and a 100 k Ω feedback network, the current required to drive the network is 10 μ A, which is already larger than the total supply current of the IAs in [14]–[20]. Increasing the resistance of the network is not a very attractive option as it leads to larger chip area and more noise.

III. CAPACITIVELY-COUPLED CHOPPER INSTRUMENTATION AMPLIFIER (CCIA)

A) Basic Topology: The capacitively-coupled chopper topology has recently been employed in bio-potential sensing IAs [14], [18]. As shown in Fig. 1, it comprises an opamp (A) and a capacitive feedback network (C_{in} and C_{fb}), an input chopper CH_{in} , a feed back chopper CH_{fb} , and a third chopper CH_{out} . To first-order, the gain of the IA is defined by C_{in}/C_{fb} and the offset and $1/f$ noise of the opamp are removed from

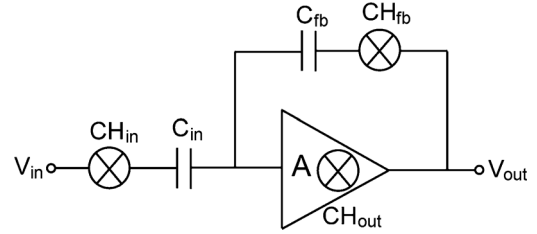


Fig. 1. A simplified block diagram of a capacitively-coupled chopper instrumentation amplifier.

the baseband. Compared to IAs based on the three traditional topologies, a CCIA has four main advantages.

- 1) Rail-to-rail sensing capability: with CH_{in} employing complementary switches, a CCIA has a rail-to-rail DC CM input range without requiring a rail-to-rail input stage for the opamp.
- 2) High power efficiency: the noise of a CCIA is dominated by that of the opamp [14], [18], thus it is more power efficient than the three-opamp and current-feedback IAs.
- 3) High gain accuracy: The accurate lithography of deep sub-micron technology results in good matching between C_{in} and C_{fb} , which in turn ensures high gain accuracy without the need for trimming.
- 4) Suitability for low power design. The capacitive feedback network can be designed to have relatively large impedances, which minimizes the current consumption of the feedback network, especially for large output signals.

B) Design Considerations: A block diagram of the proposed CCIA is shown in Fig. 2. It is based on a two-stage Miller-compensated opamp, which consists of an input transconductance G_{m1} and an integrator built around G_{m2} . A capacitive bridge comprising of input capacitors $C_{in1,2}$ and feedback capacitors $C_{fb1,2}$ is built around the opamp. Taking into account the finite open-loop gain of the opamp, the gain G of the CCIA is given by

$$G = \frac{A_0}{1 + A_0 C_{fb1,2} / C_{in1,2}} \quad (1)$$

where A_0 is the open-loop gain of the opamp. To ensure a gain inaccuracy better than 0.1%, for example, A_0 should be larger than 100 dB. This is not easily achieved by a single stage opamp, which is why a two-stage Miller-compensated opamp was chosen. The combination of $CH_{in1,2}$ and $C_{in1,2}$ can be seen as an equivalent input resistor with a resistance of $1/2f_{chop}C_{in}$, where f_{chop} is the chopping frequency. This resistor then defines the input impedance of the CCIA. The combination of CH_{fb} and C_{fb} can be seen as an equivalent feedback resistor with a resistance of $1/2f_{chop}C_{fb}$ that loads the CCIA's output stage. The offset and $1/f$ noise of G_{m1} are up-modulated by CH_{out} and then filtered by the integrator built around G_{m2} . The up-modulated offset and $1/f$ noise generate a ripple, which will be suppressed by the ripple-reduction loop (RRL) introduced in Section IV. The offset and $1/f$ noise of G_{m2} is suppressed by the gain of G_{m1} . The DC level at the opamp's input is properly biased to a reference voltage V_{ref}

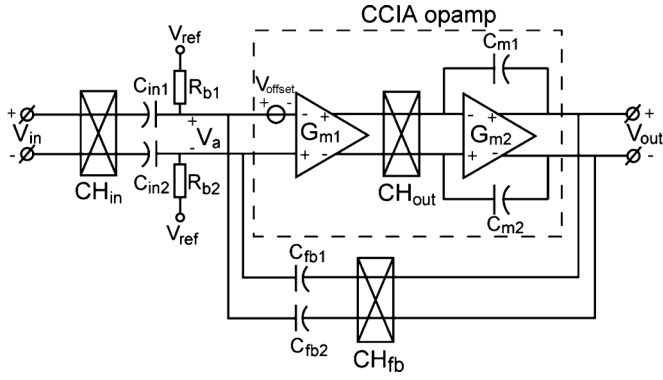


Fig. 2. A schematic of the proposed capacitively-coupled chopper instrumentation amplifier.

by high-resistance resistors implemented as MOS transistors operated in their sub-threshold region [14].

The action of the choppers will produce spikes since the bridge capacitors $C_{in1,2}$ and $C_{fb1,2}$ are constantly being charged and discharged by the input and output signal voltages. Due to the opamp's finite output impedance, the output spikes associated with $C_{fb1,2}$ will be fed to a succeeding ADC and could cause error. To reduce the duration of these spikes, the CCIA opamp's output stage must be able to provide currents much larger than the average DC current required to drive the capacitive bridge. To reduce the amplitude of the spikes, smaller feedback capacitors can be chosen at the expense of lower capacitance matching. A low-pass filter can be used after the CCIA to suppress the spikes; however, this is at the expense of extra power consumption and chip area. A better solution is to ensure that the succeeding ADC only samples the CCIA's output after it has fully settled. This can be readily implemented in fully integrated systems.

C) Implementation: In this implementation, the gain of the CCIA is fixed to 100. f_{chop} is chosen to be 5 kHz, which is higher than the $1/f$ noise corner of G_{m1} . Increasing f_{chop} will result in more charge injection and clock feed-through, leading to higher residual offset [28]. With $C_{in1,2} = 12$ pF and $C_{fb1,2} = 120$ fF, the equivalent input and feedback resistances are around 8 M Ω and 800 M Ω respectively without considering parasitic effects. Fringe capacitors (metal-oxide-metal) were employed to implement the capacitive bridge.

The schematic of the opamp is shown in Fig. 3. For high DC gain, G_{m1} is implemented as a folded-cascode OTA, while for large output swing, G_{m2} is implemented as a class-A output stage. All transistors used in the CCIA are thick-oxide transistors despite their relatively high threshold voltages (0.6 V). This is because such transistors have low gate leakage currents and also offer higher intrinsic gain. In a low power design, leakage currents can cause significant errors, especially at the opamp's virtual ground node (V_a). Due to noise considerations, the resistance of the bias resistors is about 10 G Ω , and so 50 pA of gate leakage from the two PMOS input transistors is more than enough to cause the input voltage to clip. The simulated DC gain of the two-stage Miller-compensated CCIA opamp is 130 dB, which according to (1) corresponds to a gain errors $<0.01\%$ for $G = 100$. Since the gain is mainly determined by $C_{in1,2}/C_{fb1,2}$,

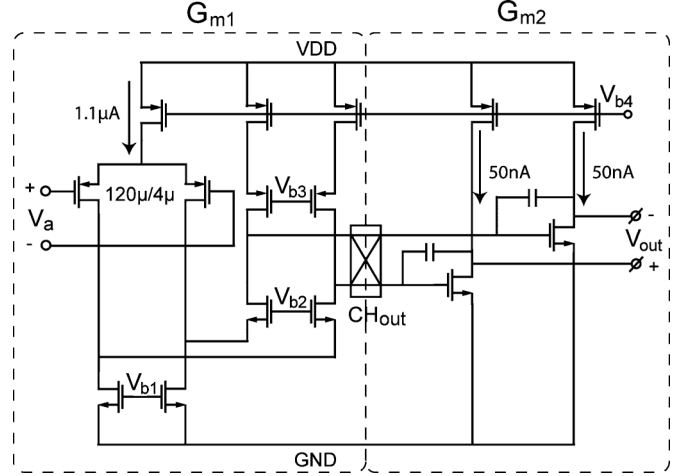


Fig. 3. A schematic of the capacitively-coupled instrumentation amplifier opamp.

the final gain inaccuracy will be determined by the process spread and variation of $C_{in1,2}/C_{fb1,2}$, which is expected to be around 0.1%. The CCIA's noise is dominated by the noise of the input stage of G_{m1} . To achieve high power efficiency, the input PMOS differential pair is biased in weak inversion. It consumes 61% of the total supply current and consequently, a 55 nV/ $\sqrt{\text{Hz}}$ simulated noise voltage density V_{nopamp} of the input stage is obtained. With $C_{in1,2}/C_{fb1,2} = 100$, the CCIA's input-referred noise is essentially equal to V_{nopamp} [14]. The Miller capacitor $C_{m1,2}$ (fringe capacitor) are chosen to be 30 pF, and so the unity-gain frequency of the CCIA is 70 kHz. The bias current of the class-A output stage is chosen to be 2×50 nA which is sufficient to drive the capacitive bridge with a 1 V_{pp} output signal.

The bias resistors $R_{b1,2}$ are implemented as NMOS transistors biased in the sub-threshold region. Their resistance is set to approximately 10 G Ω to obtain an input noise density of about 10 nV/ $\sqrt{\text{Hz}}$ [14], which is negligible compared to that of the whole CCIA.

IV. POSITIVE FEEDBACK LOOP (PFL), RIPPLE REDUCTION LOOP (RRL), AND THE DC SERVO LOOP (DSL)

The CCIA has two main drawbacks: 1) limited input impedance mainly determined by the equivalent resistance determined by $C_{in1,2}$ and f_{chop} , and 2) chopping ripple due to the up-modulated offset and $1/f$ noise of G_{m1} .

To boost the input impedance of the CCIA, a positive feedback loop (PFL) is employed. It consists of a positive feedback path connected between the input and the output of the CCIA. It converts the output voltage into a current which is injected back into the signal source. This current partially compensates for the current drawn from the signal source by the switched capacitor resistor formed by CH_{in} and $C_{in1,2}$, thus increasing the CCIA's input impedance.

The chopping ripple is mainly due to the up-modulated offset and $1/f$ noise of G_{m1} . To suppress it, a ripple-reduction loop (RRL) is employed [10], [13]. This senses the ripple at the CCIA's output and generates a current which compensates for

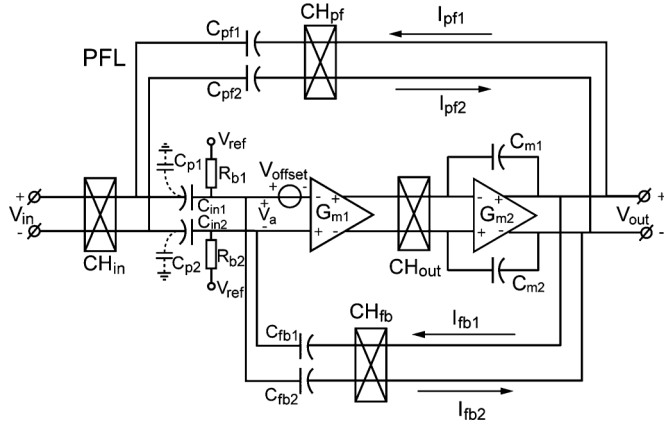


Fig. 4. A schematic of the capacitively-coupled instrumentation amplifier with the positive feedback loop.

G_{m1} 's offset current. When this current is fully compensated, no output ripple will be present.

For bio-sensing applications, where large DC electrode offsets are expected, a DC servo loop (DSL) can be optionally employed. The DSL is essentially an integrating negative feedback path. The CCIA's output is integrated and the resulting signal is fed back to its virtual ground in such a way as to cancel any DC component at the CCIA's output. The DSL acts as a high-pass filter that effectively rejects electrode offset, which could otherwise saturate the CCIA. The working principles and design considerations of the PFL, RRL and the DSL will be explained in more detail in the following sections.

A. Positive Feedback Loop (PFL)

1) *Working Principle:* A block diagram of the CCIA with a PFL is shown in Fig. 4. The loop comprises a chopper CH_{pf} and two feedback capacitors $C_{pf1,2}$ which provide positive feedback to the CCIA's input. In the ideal situation, the PFL generates currents $I_{pf1,2}$ equal to $I_{fb1,2}$, so that no input current is drawn from the signal source and the input impedance of the CCIA is infinite. The value of $C_{pf1,2}$ for infinite input impedance can be calculated by making $I_{pf1,2}$ and $I_{fb1,2}$ equal:

$$\begin{aligned} I_{pf1,2} &= 2(V_{out} - V_{in}) \cdot f_{chop} \cdot C_{pf1,2} \\ &= 2V_{out} \cdot f_{chop} \cdot C_{fb1,2} = I_{fb1,2} \\ \Rightarrow C_{pf1,2} &= \frac{C_{in1,2}}{G - 1} \end{aligned} \quad (2)$$

The PFL loads the CCIA since the current flowing through it has to be supplied by the CCIA. The equivalent loading resistance is around $1/2f_{chop} \cdot C_{pf1,2} = 800 \text{ M}\Omega$. This loading is equal to that of the negative feedback path ($C_{fb1,2}$).

2) *Implementation:* With $G = 100$, $C_{in1,2} = 12 \text{ pF}$ and $C_{fb1,2} = 120 \text{ fF}$, $C_{pf1,2}$ has to be 121.21 fF to reach an infinite input impedance according to (2). This can be challenging in layout and thus in this work, $C_{pf1,2}$ are chosen to be equal to $C_{fb1,2}$. The compromised boosted input impedance of the CCIA is then given by

$$Z_{in-pf} = \frac{V_{in}}{I_{in-pf}} = \frac{G}{2f_{chop} \cdot C_{in1,2}} = 100Z_{in} \quad (3)$$

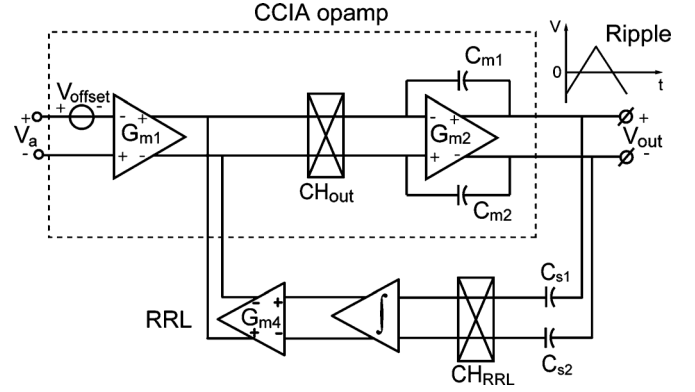


Fig. 5. A simplified block diagram of the ripple reduction loop.

where Z_{in} is the original input impedance and Z_{in-pf} is the boosted input impedance, I_{in-pf} is the net current drawn from the signal source.

3) *Parasitic Effects:* In practice, the parasitic capacitance $C_{p1,2}$ located between $C_{in1,2}$'s bottom-plate and ground shown in Fig. 4 will further limit the input impedance. CH_{in} and $C_{p1,2}$ act as an equivalent parasitic resistor with a resistance of $1/2f_{chop} \cdot C_{p1,2}$. The current drawn by this resistor will not be compensated by a PFL dimensioned according to (2). As a result, this parasitic resistor limits the maximum input impedance. In a standard CMOS process, $C_{p1,2}$ ranges between 10% to 40% of $C_{in1,2}$. This means that a PFL dimensioned according to (2) will only boost the input impedance by a factor of $2.5\times$ to $10\times$. To overcome this, the PFL can be designed to also compensate for the extra current flowing through the parasitic resistor $I_{p1,2}$. Equation (2) can then be modified as follows:

$$\begin{aligned} I_{pf-modi1,2} &= 2(V_{out} - V_{in}) \cdot f_{chop} \cdot C_{pf1,2-modi} \\ &= I_{fb1,2} + 2V_{in} \cdot f_{chop} \cdot C_{p1,2} = I_{fb1,2} + I_{p1,2} \\ \Rightarrow C_{pf1,2-modi} &= \frac{C_{in1,2} + C_{p1,2}}{G - 1} \end{aligned} \quad (4)$$

where $I_{pf-modi1,2}$ is the modified compensating current provided by the PFL, and $C_{pf1,2-modi}$ is the optimal value for $C_{pf1,2}$. In practice, however, the exact value of $C_{p1,2}$ will be uncertain, and so $C_{pf1,2}$ can be made adjustable in order to obtain maximum input impedance.

B. Ripple Reduction Loop

1) *Working Principle:* The up-modulated G_{m1} 's offset and $1/f$ noise create a ripple at the output of the CCIA. With 10 mV G_{m1} offset, $G_{m1} = 13 \mu\text{S}$, $f_{chop} = 5 \text{ kHz}$ and $C_{m1,2} = 30 \text{ pF}$, the ripple at the output is approximately

$$V_{ripple} = \frac{V_{offset} \cdot G_{m1}}{2f_{chop} \cdot C_{m1,2}} = \frac{10 \text{ mV} \cdot 13 \mu\text{S}}{2 \cdot 5 \text{ kHz} \cdot 30 \text{ pF}} = 433 \text{ mV}. \quad (5)$$

This would take excessive headroom for a 1 V supply and must be suppressed. Decreasing G_{m1} leads to more noise, while increasing f_{chop} and $C_{m1,2}$ results in larger residual offset and more chip area respectively. There are several effective techniques to reduce the ripple. In [29], a switched-capacitor notch filter is employed to notch out the chopping ripple. This method

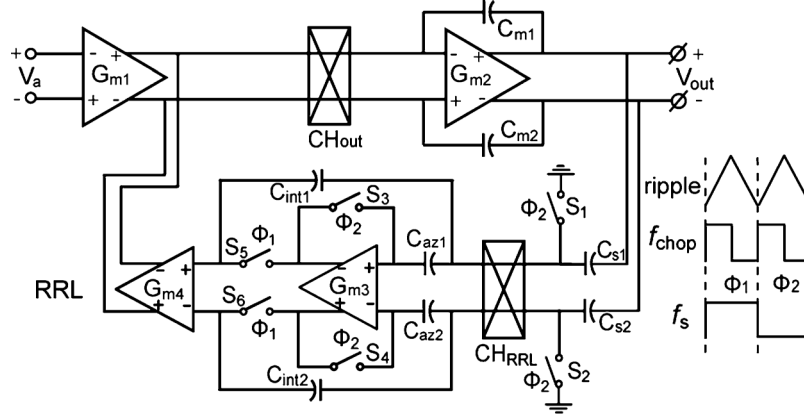


Fig. 6. A schematic of the ripple reduction loop with the proposed switched-capacitor integrator.

is very power efficient. However, including a notch filter in the signal path complicates the frequency compensation. In [30], an auto-correction loop is used to reduce the ripple. This method simplifies the required frequency compensation. However, the loop senses the ripple at a virtual ground node, where it is quite small, and so requires a relatively high gain. In this work, an AC coupled continuous-time ripple reduction loop (RRL) is employed [10], [13]. A block diagram of the RRL is shown in Fig. 5. It consists of sensing capacitors $C_{s1,2}$, a demodulating chopper CH_{RRL} , an integrator and a compensation transconductor G_{m4} . Instead of sensing at the virtual ground node of G_{m2} [30], $C_{s1,2}$ sense and convert the large ripple voltage at the amplifier's output into an AC current; the AC current is then integrated by the integrator into a voltage; this voltage is then converted by G_{m4} into a current, which compensates for G_{m1} 's offset current. The RRL creates a notch at f_{chop} with a width determined by flexible design parameters such as $C_{s1,2}$, and G_{m4} [13]. Compared to [30], the main drawback of this method is that $C_{s1,2}$ loads the amplifier's output, and thus should be kept small.

In [10] and [13], a passive integrator comprising a current buffer and an integration capacitor is used in the RRL. The offset of the current buffer, however, generates second harmonic ripple which could require large integration capacitor to filter [10], [13]. This is more problematic for low f_{chop} . To overcome this problem, an auto-zeroed SC integrator can be employed. However, a standard auto-zeroed SC integrator is reset during one phase so that its offset can be stored on an auto-zero capacitor. During that phase, the output of the integrator can not be connected to G_{m4} , otherwise, an error compensating current will be injected into the CCIA. To solve this problem, an auto-zeroed SC integrator with valid output voltage during all phases is proposed. A block diagram of the RRL with such an integrator is shown in Fig. 6. The SC integrator comprises sensing capacitors $C_{s1,2}$; a demodulation chopper CH_{RRL} ; integration capacitors $C_{int1,2}$; auto-zero capacitors $C_{az1,2}$ and a single stage opamp G_{m3} . CH_{RRL} is synchronized to f_{chop} . The rest of the switches ($S_1 - S_6$) are driven at switching frequency f_s which is chosen to be half of f_{chop} . f_s contains an integration phase Φ_1 and an auto-zero phase Φ_2 and each phase incorporates a complete cycle of f_{chop} , thus during Φ_1 , a full cycle ripple can be detected by the RRL. A timing diagram is shown in Fig. 6. During

Φ_1 , $C_{s1,2}$ convert the ripple voltage into an AC current, which is then demodulated by CH_{RRL} and integrated on $C_{int1,2}$. The voltages on $C_{int1,2}$ are then converted into a current by G_{m4} to compensate for G_{m1} 's offset current. During Φ_2 , $C_{s1,2}$ are shorted to ground so that no ripple current is integrated. G_{m3} is configured in unity-gain configuration so that its offset is sampled and stored on $C_{az1,2}$. During this time, $C_{int1,2}$ are disconnected from the output of G_{m3} , holding the voltage set at the end of last Φ_1 ; and connected to the input of G_{m4} . In this way, the correct compensating current is injected into G_{m1} during both phases. In the ideal case, the compensating current fully compensates for G_{m1} 's offset current, leaving no output ripple at the steady state.

2) *Implementation:* The values of $C_{s1,2}$, $C_{int1,2}$ and the transconductance of G_{m4} determine the RRL's unity-gain frequency f_{0RRL} which is given by [13]

$$f_{0RRL} = \frac{G_{m4} C_{s1,2}}{2\pi C_m C_{int1,2}}. \quad (6)$$

The notch width of the RRL equals to $2f_{0RRL}$. With the CCIA's bandwidth equal to 700 Hz and f_{chop} equal to 5 kHz, f_{0RRL} should be smaller than 4.3 kHz to maintain CCIA's signal bandwidth. Moreover, the value of G_{m4} usually has to be smaller than G_{m1} to suppress the noise of the RRL V_{nRRL} , which is calculated by the following equation when referred to the input of the CCIA

$$V_{nRRL} = \left(\frac{C_{in1,2} + C_{fb1,2} + C_g}{C_{in1,2}} \right) \frac{\sqrt{(V_{ninte}^2 + V_{nGm4}^2)} G_{m4}}{G_{m1}} \quad (7)$$

where V_{ninte} is the output voltage noise of the RRL integrator; V_{nGm4} is the input voltage noise of G_{m4} . To make V_{nRRL} negligible compared to G_{m1} 's noise, G_{m4} is designed to be $0.65 \mu S$ which is $20\times$ smaller than G_{m1} . Together with $C_{s1,2} = 240$ fF, $C_{int1,2} = 2.5$ pF and $C_{m1,2} = 30$ pF, f_{0RRL} is calculate by (6) to be around 330 Hz which is much smaller than 4.3 kHz. With $C_{s1,2} = 240$ fF, this RRL hardly loads the output of the CCIA. $C_{az1,2}$ are chosen to be 1.4 pF with the considerations of suppressing charge injection errors from switch $S_{3,4}$ and saving chip area.

G_{m3} employs a telescopic topology to obtain large DC open loop gain and its schematic is shown in Fig. 7. G_{m3} 's open loop

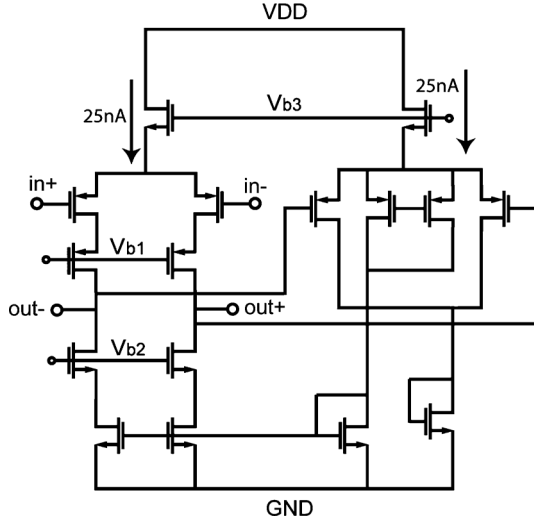


Fig. 7. A schematic of the ripple reduction loop switched-capacitor integrator opamp.

gain A_{Gm3} determines the RRL's loop gain $L(0)$ which is given by [13]

$$L(0) = \frac{A_{Gm3} G_{m4}}{C_{m1,2} f_{chop}}. \quad (8)$$

Ideally, the ripple should be suppressed by a factor equal to $L(0)$. To suppress the output ripple by 1000 times so that the input-referred ripple is in the order of a few microvolts, A_{Gm3} should be at least 48 dB. The open loop gain of the telescopic G_{m3} is simulated to be 76. G_{m3} consumes 50 nA supply current, which is negligible compared to the total current consumption of the CCIA.

C. DC Servo Loop (DSL)

1) *Working Principle and Implementation:* The DSL can be optionally employed for bio-sensing when large electrode offset is present. Although a high-pass transfer function can be easily obtained by disabling the choppers around the CCIA [16]–[18], the degraded CMRR due to feedback capacitors mismatch however, is undesirable. To obtain a high CMRR, chopping is maintained, and a high-pass transfer function is realized by implementing a DSL as also in [14]. The low-pass characteristic is automatically granted by the limited bandwidth of the CCIA, which is larger than the maximum ECG/EEG signal bandwidth (around 100 Hz). A block diagram of the CCIA with such a DSL is shown in Fig. 8. The DSL comprises an integrator which amplifies the DC signal at the output of the CCIA; a chopper CH_{hp} which up-modulates the amplified DC signal; and capacitors $C_{hp1,2}$ which feed the up-modulated signal to the CCIA virtual ground (V_a). The integrator will keep integrating until the signal at the output of the CCIA is DC free. The DSL creates a high-pass corner f_{hp} which is given by [14]

$$f_{hp} = \frac{C_{hp1,2}}{C_{fb1,2}} f_{0DSL} \quad (9)$$

where f_{0DSL} is the unity-gain frequency of the integrator in the DSL. f_{hp} is set to 0.5 Hz for bio-signals such as ECG/EEG

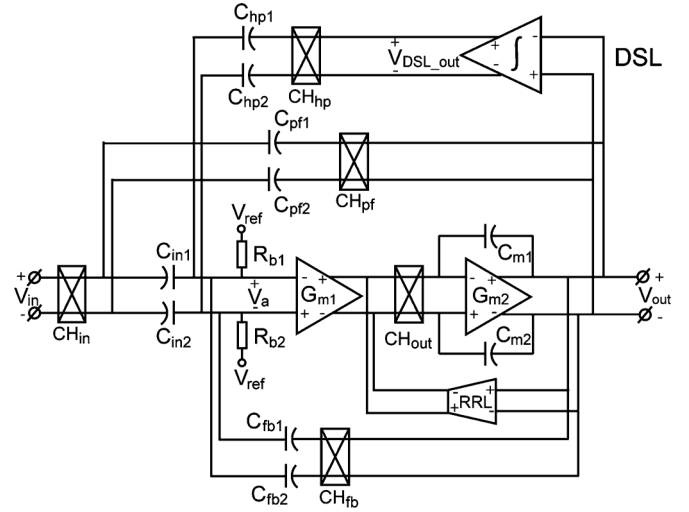


Fig. 8. A block diagram of the capacitively-coupled instrumentation amplifier with the optional DC servo loop.

signals [15], [16]. The values of $C_{hp1,2}$ is determined by the following equation

$$V_{outmax} = \frac{C_{in1,2}}{C_{hp1,2}} V_{eo} \quad (10)$$

where V_{eo} is the maximum expected electrode offset and V_{outmax} is the maximum output voltage of the DSL integrator (V_{DSL_out}) and in this case equals to the supply voltage 1 V. For wet electrodes, a maximum V_{eo} of 50 mV can be expected [14], [15]. Thus, $C_{hp1,2}$ are chosen to be 600 fF. And f_{0DSL} is calculated to be 0.1 Hz by (9). An SC integrator with such a low unity-gain frequency can occupy large chip area [14] which is not suitable for wireless sensor nodes. In this work, a very-large time constant (VLT) SC integrator [21] is employed to save the chip area significantly.

2) *Very-Large Time Constant SC Integrator (VLT SC Integrator):* A block diagram of the VLT SC integrator is shown in Fig. 9. The integrator comprises an opamp and a capacitor network around it ($C_{a1,2}$, $C_{A1,2}$, $C_{a'1,2}$ and S_1 – S_7). All switches in the capacitor network are driven at a switching frequency f_{sVLT} equal to $2f_{chop}$ in order to sample at the zero-crossing point of the CCIA's output ripple. A timing diagram is shown in Fig. 9. The transfer function of a VLT SC integrator is given by the following equation [21] when $C_{a1,2} = C_{a'1,2}$:

$$H(Z) = - \left(\frac{C_{a1,2}}{C_{A1,2}} \right)^2 \frac{Z^{-1/2}}{1 - Z^{-1}}. \quad (11)$$

By making $H(Z)$ equal to unity, the unity-gain frequency f_{0VLT} of the VLT-SC integrator can be computed as

$$f_{0VLT} = \frac{f_{sVLT} C_{a1,2}^2}{2\pi C_{A1,2}^2}. \quad (12)$$

The unity-gain frequency f_{0stan} of a standard fully differential SC integrator (shown in Fig. 10) is given by

$$f_{0stand} = \frac{f_{swi} C_{sam}}{2\pi C_{inte1,2}} \quad (13)$$

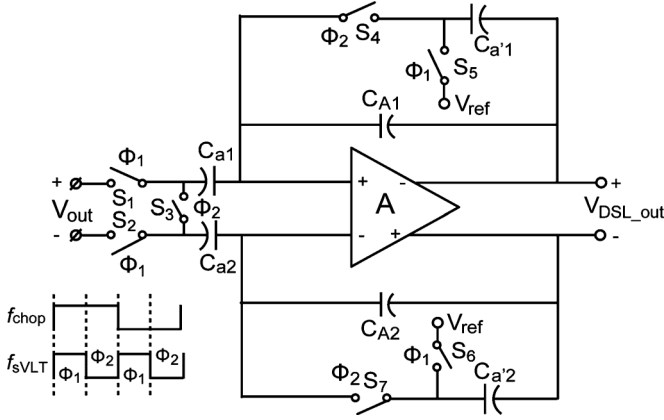


Fig. 9. A block diagram of the very-large time constant switched-capacitor integrator.

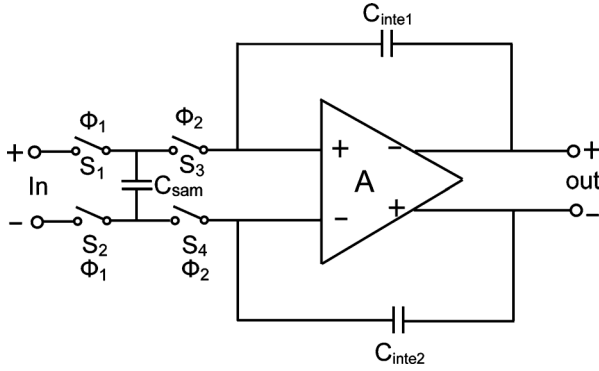


Fig. 10. A block diagram of a standard switched-capacitor integrator.

where f_{swi} is the switching frequency for switches S_1 – S_4 . In this work, to achieve the 0.1 Hz unity-gain frequency calculated by (9), when switching at 2.5 kHz, the VLT SC integrator uses $C_{a1,2} = C_{a'1,2} = 240$ fF and $C_{A1,2} = 15$ pF, while to achieve the same unity-gain frequency with the same sampling capacitor, a standard integrator has to use $C_{inte1,2} = 937.5$ pF according to (13)! This proves that the VLT SC integrator is much more area efficient.

V. EXPERIMENTAL RESULTS

The circuit was implemented in a 65 nm CMOS technology. The CCIA operates from a 1 V supply, from which it draws $1.8 \mu\text{A}$ without the DSL and $2.1 \mu\text{A}$ with the DSL. The active chip area is 0.1 mm^2 without the DSL and 0.2 mm^2 with the DSL. A chip photo is shown in Fig. 11, which includes the DSL.

With the DSL off, the measured DC CMRR is greater than 134 dB, while the DC PSRR is greater than 120 dB for 20 samples. The worst-case measured offset is $1 \mu\text{V}$. A histogram of the offset is shown in Fig. 12. Apart from layout issues which are very critical, this residual offset is also due to the mismatched charge injection and clock feed-through associated with the choppers [28]. The relative DC gain accuracy of the CCIA is better than 0.16%. A histogram of the gain variation is shown in Fig. 13. As shown in Fig. 14, the measured output noise spectrum density is $6 \mu\text{V}/\sqrt{\text{Hz}}$, which is equivalent to an input-referred noise of $60 \text{ nV}/\sqrt{\text{Hz}}$. This confirms that the noise is mostly dominated by the input stage. Furthermore, the

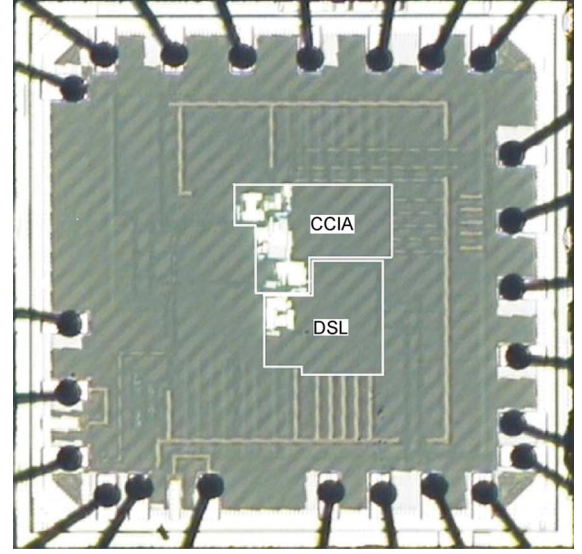


Fig. 11. Chip microphoto.

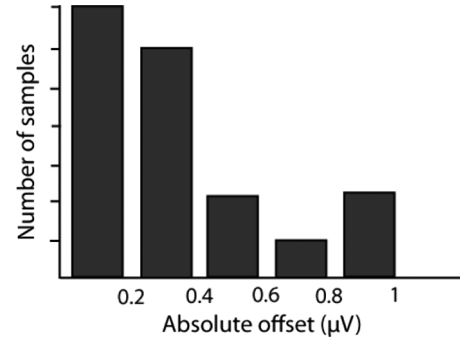


Fig. 12. Histogram of the residual offset.

noise floor is flat until 100 mHz which proves that the $1/f$ noise is effectively removed by chopping. After activating the PFL, the measured input-impedance increases from $6 \text{ M}\Omega$ to $30 \text{ M}\Omega$. The original input-impedance and the boost factor is lower than expected ($8 \text{ M}\Omega$ and 100) due to the presence of parasitic input capacitors, as has been explained in Section IV. The RRL reduces the amplitude of the output ripple to less than $300 \mu\text{V}$ at all the harmonics. This output ripple is relatively large compared to those reported in [10], [13], [29], [30]. The limited power consumption (50 nW) restricted the DC gain of G_{m3} , which in turn leads to a RRL with relatively low loop gain. However, at a gain of 100, the input-referred ripple ($3 \mu\text{V}$) is of the same order as the residual offset, and is thus low enough for most applications. The transient response of the CCIA to a 500 mV output step is shown in Fig. 15. The spikes due to the various switching events are also shown. It can be seen that the output settles well before the end of the clock phase so that an ADC can avoid the spikes by sampling just before the next clock transition. Table I summarizes the CCIA's performance without the DSL and compares it with other state-of-the-art IAs featuring high DC accuracy. This work achieves the highest power efficiency, which is indicated by a low Noise Efficiency Factor ($\text{NEF} = V_{n\text{rms}} \sqrt{2I_{\text{tot}} / (\pi \times V_t \times 4kT \times \text{BW})}$), where $V_{n\text{rms}}$ is the input-referred rms noise voltage, I_{tot} is the total

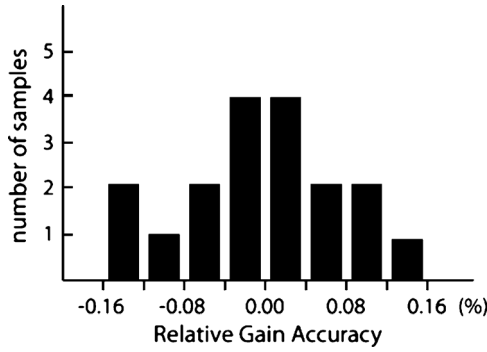
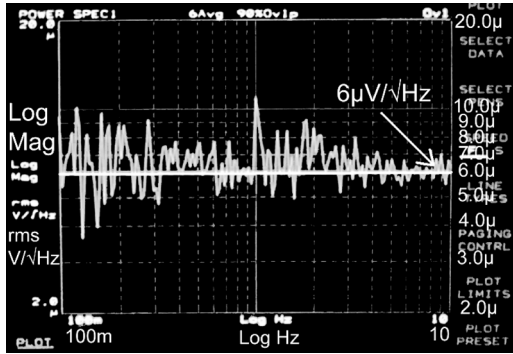


Fig. 13. Histogram of the relative gain accuracy.

Fig. 14. Output noise spectrum of the capacitively-coupled instrumentation amplifier with a gain of 100 (Y axis: log format; 2 $\mu\text{V}/\sqrt{\text{Hz}}$ –20 $\mu\text{V}/\sqrt{\text{Hz}}$; X axis: log format; 100 mHz–10 Hz).

current consumption and BW is the amplifier's bandwidth in Hertz [17]). Although such a low NEF is partly due to the smaller bandwidth compared to [10]–[13] and the fact that the CCIA is not designed to be unity-gain stable; the benefit of the CCIA topology is still evident as its noise is dominated by a single amplifier: G_{m1} . The CCIA also achieves the lowest residual offset, as well as the lowest supply voltage and power consumption, attributes that are critical for wireless sensor nodes. For bio-potential measurements, the DSL is added, resulting in the high-pass frequency response shown in Fig. 16. The high-pass corner frequency is located at 0.5 Hz. At frequencies below 100 Hz, the measured AC CMRR is larger than 110 dB which is at least 30 dB higher than [16], [17]. The chip area with the DSL is 7 \times smaller than that of the fully differential version of [14] where a similar DSL is employed but with a less area-efficient SC integrator. The noise of the CCIA with the DSL increases to 6.7 μV_{rms} in a bandwidth of 0.5–100 Hz for bio-signals.

VI. CONCLUSION

A precision CCIA has been implemented in a 65 nm CMOS technology. For DC measurements, it achieves state-of-the-art performances in terms of NEF, offset, CMRR, PSRR and gain accuracy. The power efficiency is due to the use of a capacitively-coupled chopper topology. It has a rail-to-rail DC CM input range without using a rail-to-rail input stage. Operating from a 1 V supply, the amplifier's power consumption is 1.8 μW with a chip area of 0.1 mm^2 . With an additional DSL, the CCIA can be used for bio-potential sensing where it consumes 2.1 μW

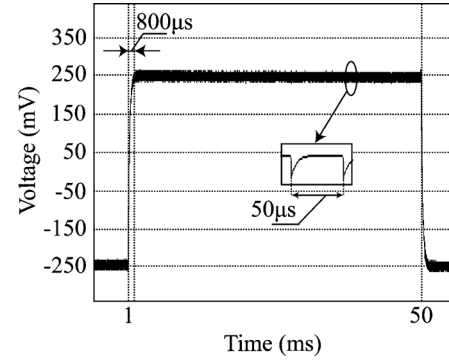


Fig. 15. Transient step response of the capacitively-coupled instrumentation amplifier.

TABLE I
PERFORMANCE SUMMARY

	[10]	[11]	[12]	[13]	This work
Input-referred offset	2 μV	3 μV	2.5 μV	5 μV	1 μV
CMRR(dB)	136	140	134	120	134
PSRR(dB)	120	120	120	120	120
Input-noise(nV/ $\sqrt{\text{Hz}}$)	21	27	42	15	60
NEF	9.6	43.5	29.2	8.8	3.3
Gain Accuracy (DC)	0.53%	0.1%	0.1%	0.5%	0.16%
Chip Area (mm^2)	1.8	2.5	1.8	4.8 (active)	0.1
Supply current (μA)	143	1700	340	230	1.8
Supply voltage (V)	5	3	5	5	1
Technology	0.7 μm	0.5 μm	0.7 μm	0.7 μm	65nm
Gain	Unity-gain stable	Unity-gain stable	Unity-gain stable	Gain >20	100 fixed gain

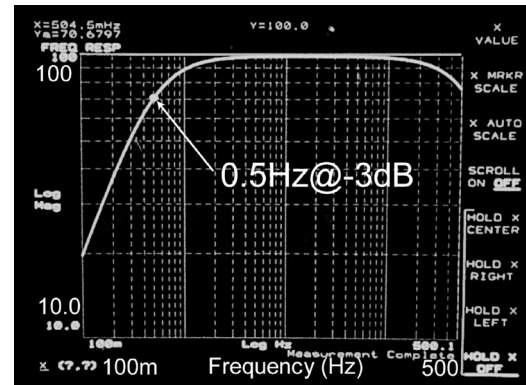


Fig. 16. The high-pass response of the capacitively-coupled instrumentation amplifier with the DC servo loop. (Y axis: log format; 10–100; X axis: log format; 100 mHz–500 Hz).

power consumption and occupies a chip area of 0.2 mm^2 . The deep submicron technology, the low supply voltage, low power consumption and low area makes the CCIA suitable for a variety of wireless sensor applications.

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