A 42 mW 2 GS/s 4-bit flash ADC in 0.18-μm CMOS

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***Abstract*—A low power 4-bit 2 GS/s flash ADC is presented. To enhance the speed, the analog part of the ADC is fully pipelined; reset switches are inserted into preamplifiers and comparators for fast overdrive recovery. Post-simulation results show that the peak DNL and INL are 0.04 LSB and 0.06 LSB, respectively. With 970.2 MHz input, the SFDR and ENOB achieve 33.2 dB and 3.61 bits at 2 GS/s. the ADC occupies 0.32 mm^2 active area in 0.18-μm CMOS process and consumes 42 mW with a 1.8 V power supply.**

Keywords-flash ADC; A/D converter; overdrive recovery; comparator; gray codes; encoder

I. INTRODUCTION

High-speed low-resolution analog-to-digital converters (ADCs) are the key building blocks in various fields, including the disk systems, wireless communication systems, high-speed instrumentations and regulators [1]-[3]. Many of these applications require 3 bits to 6 bits resolution at conversion rates of GHz or beyond. Although multi-channel ADC architectures such as time-interleaved ADCs can achieve high speeds, they often require extensive and costly post-fabrication calibration, and also need very precise multi-phase clocks [4]. Flash ADC architectures are typically the simplest and fastest structures that can be used to implement ultra-high-speed converters.

In this paper, a 4-bit 2 GS/s 42 mW flash ADC designed in 0.18-μm CMOS technology is presented. Reset switches are inserted into preamplifiers and comparators for fast overdrive recovery. To improve the sampling rate, the analog part of the ADC is fully pipelined. The encoder is implemented only by XOR gates for improving performance.

This paper is organized as follows: In Section II, the architecture of this ADC is presented, and its major building blocks are discussed in Section III. The post-simulation results and layout are shown in Section IV. A Conclusion is given in Section V.

II. ARCHITECTURE

The architecture of the ADC is shown in Fig. 1. It has a track-and-hold (T/H) circuit, a folded reference ladder, four-input preamplifiers, first-stage comparators, second-stage comparators, SR latches, and a digital encoder. The T/H circuit improves dynamic performance: by holding the input analog signal during quantization, it mitigates clock and signal skews [5]. As shown in Fig. 1, the folded reference ladder provides differential reference voltages to the preamplifier array, and the two preamplifiers at the edges are positioned next to each other [1]. The preamplifier stage amplifies the difference between the differential input signal and the reference voltage. The next stage is the array of the first-stage comparator. The maximum sampling rate of flash ADCs is limited by its preamplifiers and comparators overdrive recovery time, so reset switches are inserted into the preamplifiers and first-stage comparators for fast overdrive recovery [1]. To decrease the bit error rate, two more regeneration stages are added, the second-stage comparator and the SR latch shown in Fig. 1. The second-stage comparator provides rail-to-rail output to SR latch. The analog part of the ADC is fully pipelined to improve the sampling rate. The digital encoder converts the thermometer code to binary code with an intermediate Gray code. By taking advantage of the special format of thermometer codes, it consists of XOR gates only, which improves the reliability.

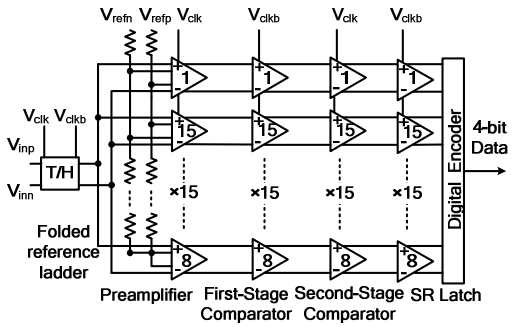

Figure 1. Block diagram of the ADC

III. CIRCUIT DESCRIPTIONS

A. Track-and-hold circuit

The T/H is critical for achieving good dynamic performance over broadband input signals [6]. By holding the input analog signal during quantization, the T/H circuit reduces errors due to skews in the clock and the input signal distributed to the multiple preamplifiers [1]. In this paper, the T/H circuit with a pseudo-differential configuration is employed. As shown in Fig. 2, it consists of an NMOS sampling switch, a dummy switch, a 1-pF MIM capacitor and a source follower. The dummy switch reduces the charge injection and the

This work is supported by the Major National S&T Project (No. 2009ZX03007-001), the National 863 Project (No. 2007AA01Z2b1 and No. 2009AA01Z261), the NSF fund (No. 60771022), Ph.D. fund (No. 20070286002) and the Research Fund of National Mobile Communications Research Laboratory of Southeast University (No. 2008B02).

978-1-4244-5668-0/09/$25.00

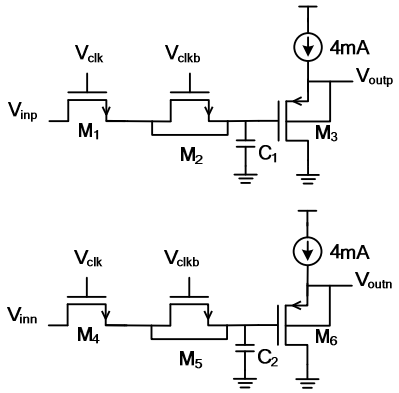

Figure 2. Track-and-hold circuit

voltage glitch, thus reducing the dynamic offset [1]. Because both the source and drain of the dummy switch are connected to the hold node, its W/L ratio is half the size of the switch.

The common mode voltage of the input signal is set to 0.3 V. The low input common mode voltage reduces the on-resistance of the NMOS-switches and increases the input tracking bandwidth. A source follower M_3 is used to shift the input common mode voltage to 1.15 V, and the source of M_3 and M_6 is tied to the well to eliminate nonlinear body effect [7].

B. Reference ladder

One source of flash ADC errors is feedthrough of input signal to reference ladder. As shown in Fig.3 (a), one input of the preamplifier is connected to the reference ladder while the other input is connected to the input voltage. The gate-source capacitances C_{gs1} and C_{gs2} couple the input signal to the reference ladder, which results in deterioration of the reference voltages. Since the reference voltage determines the location of the zero crossing generated by the preamplifier stage, this will result in distortion in the ADC [8].

As shown in Fig. 3 (b), a model is used to calculate the maximum allowed reference ladder resistance for a given shift in the reference voltages [8]. R represents the total ladder resistance and C represents the total coupling capacitance of the preamplifier stage. It is assumed that the feedthrough at nodes *refp* and *refn* is negligible due to proper decoupling. Maximum feedthrough occurs at the *mid* node, shown as follow [8]:

$$V_{mid} = \frac{\pi}{4} V_{in} f_{in} RC \tag{1}$$

In equation (1), V_{in} is the input voltage; f_{in} is the frequency of the input signal. So the required reference ladder resistance for given feedthrough is now defined by:

$$R = \frac{4V_{mid}}{\pi V_{in} f_{in} C} \tag{2}$$

C. Preamplifier

The preamplifier stage should be wideband and provide sufficient gain to overcome comparator offsets. It should also recover from large overdrive within one clock cycle [1].

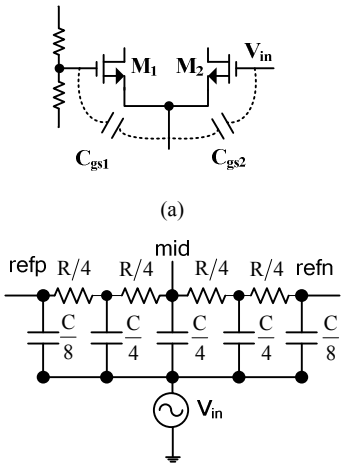

Figure 3. (a) Reference ladder feedthrough of the input signal; (b) Model for calculating the maximum reference ladder resistance

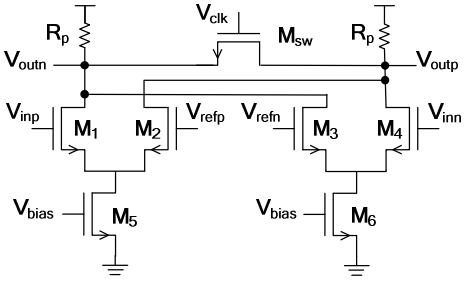

Figure 4. Preamplifier

The preamplifier circuit is shown in Fig. 4. It amplifies the difference between differential input (V_{inp}-V_{inn}) and differential reference (V_{refp}-V_{refn}). A reset switch M_{sw} is inserted between the two output nodes for fast overdrive recovery. When the V_{clk} is low, the reset switch is turned off; when the V_{clk} is high, the reset switch is turned on to erase the residual voltage from the previous sample. This method improves the bandwidth [1].

The size of the preamplifier is a trade-off between gain and bandwidth (BW). A higher transistor width will result in a higher gain. In addition, the gain is also affected by the load resistors. An increase in load resistor for higher gain lowers the output common-mode voltage, which will force the input transistors to enter the triode region [1]. The gain-BW trade-off limits the preamplifier's benefit: the higher the gain, the lower its BW, and thus the ADC's conversion rate.

Because the preamplifier is in reset mode for half the clock period T, the desired voltage gain should be available at t=T/2. The f_{-3dB} is given by [1]:

$$f_{-3dB} = -\frac{1}{\pi T} \cdot \ln[1 - \frac{G}{A}] \tag{3}$$

The gain-bandwidth product (GBW) is shown as:

$$GBW = A \cdot f_{-3dB} = -\frac{A}{\pi T} \cdot \ln[1 - \frac{G}{A}] \tag{4}$$

In equation (3), G is the desired voltage gain at t=T/2, A is the voltage gain. In this paper, a voltage gain of 3.4 is selected; f_{-3dB} can reach 2.85 GHz. Within 1 GHz, which is the Nyquist input frequency of this ADC, there is almost no drop in the gain.

D. First-stage comparator

The first-stage comparator is shown in Fig. 5. It is based on track and latch architecture. M_1 and M_2 consist of the track part, M_3 and M_4 is the latch part.

The major speed limitation of this stage is overdrive recovery. This problem is generated when the polarity of input signals is changed in two successive clock periods. For example, as shown in Fig. 5, in one clock period, V_{inp} is much larger than V_{inn}. And then in the next period, V_{inp} is smaller than V_{inn}. Reset switch M_{sw} is used to solve this problem. When V_{clk} is low, the tail current is diverted to the input differential pair, and the circuit operates in the track mode, in which M_{sw} is shorted to lower the voltage gain to less than one and the memory of the previous decision is erased [1]. When V_{clk} goes high, M_{sw} is off and the tail current is switched to the cross-coupled transistors M_3 and M_4 which form a positive feedback. The positive feedback regenerates the analog signal into a large scale output signal.

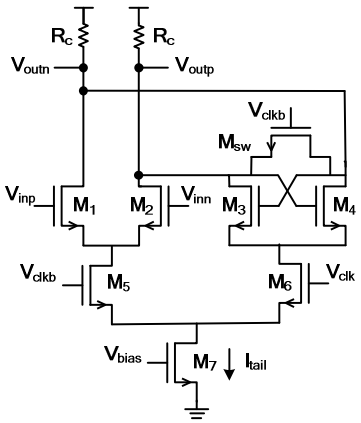

Figure 5. First-stage comparator

E. Second-stage comparator and SR latch

The second-stage comparator is shown as Fig. 6 [1]. It provides rail-to-rail output to the SR latch. The main speed limitation is the overdrive recovery time. A reset switch is introduced for fast overdrive recovery. As shown in Fig.6, when the clock is high, the comparator is in reset mode and the output is reset through two parallel discharge paths: one path is the M_5-M_1, and the other is the M_{sw}. When the clock is low, the circuit is in the regeneration mode and cross-coupled inverters M_2-M_7 and M_3-M_8 constitute a positive feedback. The tail current is steered from one side to the other, which speeds up regeneration [1].

To decrease the bit error rate, one more regeneration stage, SR latch stage is added. As shown in Fig. 7, its structure is similar to the second-stage comparator with no tail current source [1].

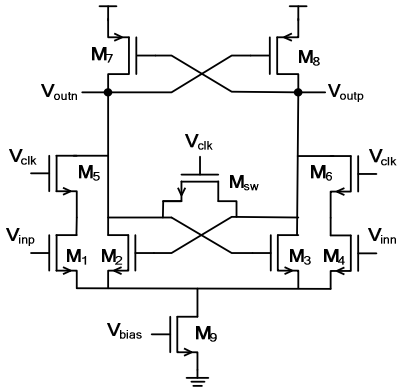

Figure 6. Second-stage comparator

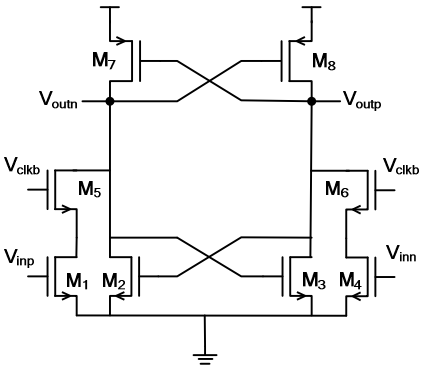

Figure 7. SR latch

F. Pipelining in the analog part

To improve the sampling rate, the analog part of the ADC is fully pipelined. As shown in Fig.8, when V_{clk} is low, the T/H is in the hold mode. At the same time the preamplifier is in the amplify mode; the first-stage comparator is in the track mode; the second-stage comparator is in the regeneration mode and the SR latch is in reset mode.

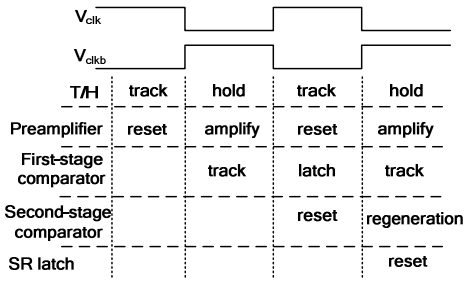

Figure 8. Timing diagram of the ADC

G. Digital encoder

The function of the digital encoder is to convert the thermometer code into binary code. The encoder typically suffers from two problems: metastability of the comparators and bubble errors in the thermometer code. Metastability errors occur when nonbinary comparator levels drive the digital encoder and produce senseless outputs [1]. For input signals with very high frequency, comparators may sample signals at

different points, which causes bubble errors in output code.

In this paper, the cascaded regeneration times of the two stages of comparators and SR latches largely reduce the metastability errors. The T/H circuit eliminates bubble errors caused by clock skews; the reset switches in the preamplifiers and first-stage comparators suppress the bubble errors caused by inadequate overdrive recovery [1]. Another effective method used to minimize the effect of metastability and bubble errors is to convert the thermometer code to Gray code as an intermediate step before binary encoding [9].

The encoder circuit is shown in Fig. 9. Logic functions are reformulated to reduce wire crossings and delays in the layout [10]. Gray code is chosen as an intermediate code to minimize the effect of metastability and bubble errors.

Because of the special format of the thermometer codes, XOR gates can be used instead of AND/NAND gates. Take T_4 and $\overline{T_{12}}$ for example, the proofs are shown as follows:

$$T_4 \bullet \overline{T_{12}} = T_4 \overline{T_{12}} \tag{5}$$

$$T_4 \oplus \overline{T_{12}} = T_4 \overline{T_{12}} + \overline{T_4} T_{12} \tag{6}$$

When $\overline{T_4}$ is 1, due to the special format of the thermometer code, T_{12} is 0, which means $\overline{T_4} T_{12}$ is always 0. The proof for other gates is similar. Therefore, the encoder can be implemented only with XOR gates, which improves the reliability of the encoder. As shown in Fig. 10, extra delay cells are added to match the delay difference among the signal paths.

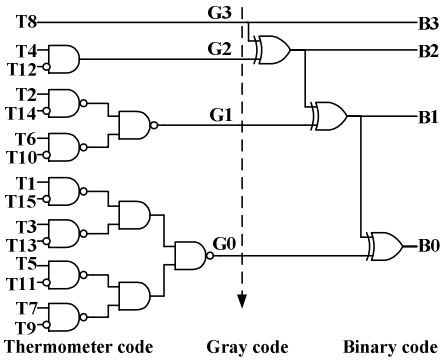

Figure 9. Digital encoder

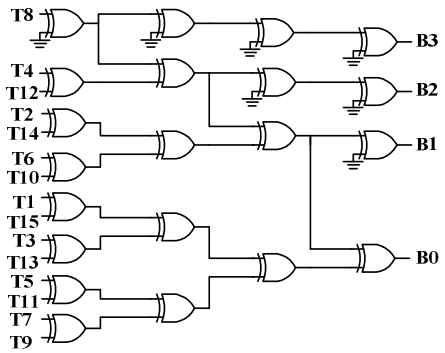

Figure 10. The encoder implemented in XOR gates

IV. POST-SIMULATION RESULTS

The post-simulation performance of this ADC is shown as follows. As shown in Fig. 11, at 2 GS/s sampling rate and about 9.8 MHz input frequency, the peak DNL and peak INL are 0.04 LSB and 0.06 LSB, respectively. The frequency spectrum of the reconstructed signal is shown in Fig. 12, where the input signal frequency is about 970 MHz and the clock frequency is 2 GHz. Fig. 13 depicts the spurious free dynamic range (SFDR) versus the input frequency at 2 GS/s sampling rate: when the input signal frequency is 91.8 MHz, the SFDR is 37.3 dB; the SFDR remains above 33 dB almost at the Nyquist input frequencies (up to 970.2 MHz). Fig. 14 shows the signal-to-noise-and-distortion (SNDR) and Effective Number of Bits (ENOB) versus input frequency at 2 GS/s. The SNDR is between 23.5 dB and 25.3 dB, and the ENOB is between 3.61 and 3.91 bits. The post-simulation results are summarized in Table I. The input voltage range of this ADC is 0.6 Vp-p.

The ADC is designed in SMIC 0.18-μm CMOS technology; it occupies 0.875 mm × 0.675 mm with 0.32 mm^2 active area. The layout is shown in Fig.15. Analog and digital supplies are separated to avoid noise injection to the analog circuits, and both supplies are respectively connected to on-chip decoupling capacitors (10 pF). Decoupling capacitors are also added at both ends (3 pF) and in the middle of the reference ladder (6 pF), which largely lowers the reference voltage bounce caused by capacitive coupling to the analog input [8]. The ADC consumes 42 mW with a 1.8 V supply which includes 37.5 mW in the analog part, 2 mW in the encoder, and 2.5 mW in the output buffer.

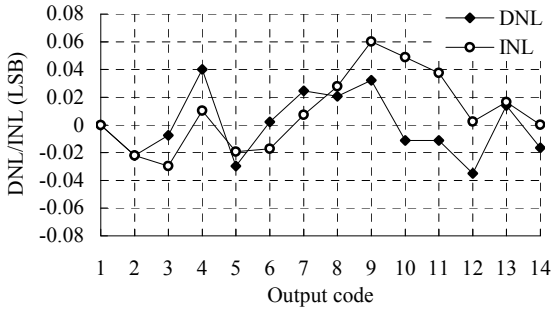

Figure 11. DNL and INL at 2 GS/s

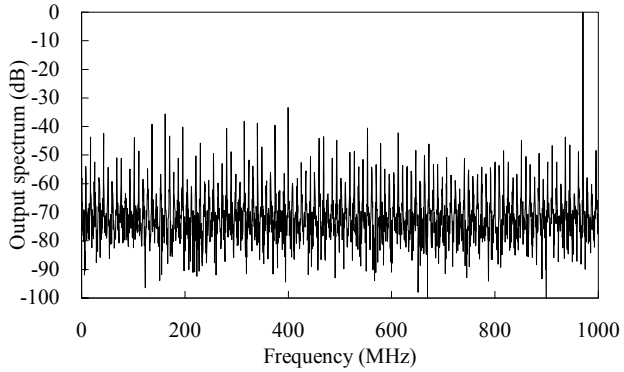

Figure 12. ADC spectrum at 2 GS/s and 970.2 MHz input frequency

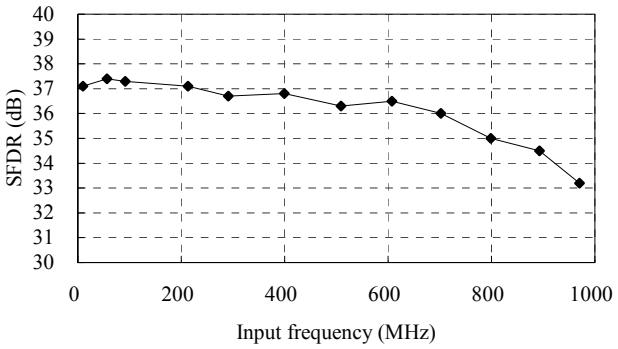

Figure 13. SFDR versus input frequency at 2 GS/s

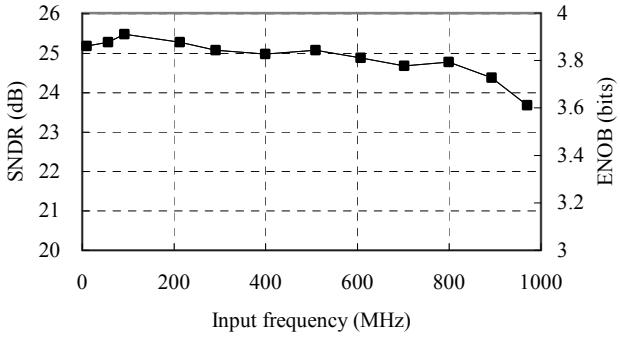

Figure 14. SNDR and ENOB versus input frequency at 2 GS/s

TABLE I. ADC PERFORMANCE SUMMARY

Technology	0.18-μm CMOS
Supply	1.8 V
Power	42 mW
Resolution	4 bits
Input range	0.6 Vp-p (differential)
Sampling Rate	Up to 2 GS/s
DNL/INL at 2 GS/s	DNL:-0.04～0.04 LSB INL: -0.03～0.06 LSB
SFDR at 2 GS/s	37.3 dB (91.8 MHz input) 33.2 dB (970.2 MHz input)
SNDR at 2 GS/s	25.3 dB (91.8 MHz input) 23.5 dB (970.2 MHz input)
ENOB at 2 GS/s	3.91 bits (91.8 MHz input) 3.61 bits (970.2 MHz input)
ADC active area	0.32 mm^2

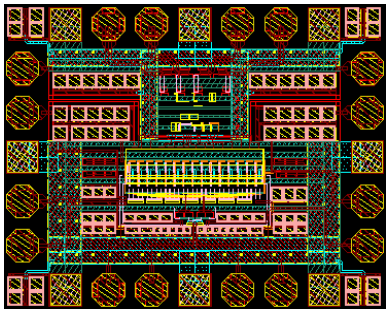

Figure 15. ADC layout (active area:0.32 mm^2)

V. CONCLUSION

In this paper, a 4-bit 2 GS/s flash ADC is presented. Reset switches in the preamplifiers and comparators give fast overdrive recovery. In order to enhance the speed, the analog part of the ADC is fully pipelined. The digital encoder is implemented only by XOR gates for improving reliability. Post-Simulation results show the peak DNL and peak INL are 0.04 LSB and 0.06 LSB, respectively; With 970.2 MHz input frequency, the SFDR is above 33 dB, ENOB is over 3.6 bits. The ADC is designed in SMIC 0.18-μm CMOS technology. It occupies 0.32 mm^2 active area and dissipates 42 mW under a 1.8 V power supply.

ACKNOWLEDGMENT

The author would like to thank Xusheng Tang, Yong Wang, and Xiaojun Wang for their successful collaboration and valuable advice.

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