Chapter 9 Sample-and-Hold Circuits

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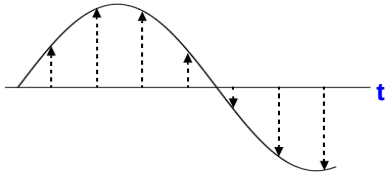
3. Sample-and-Hold Circuits

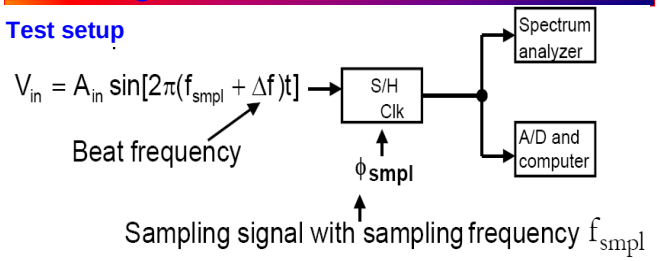
Sampling

Ideal uniform *sampling* of a continuous-time, band-limited signal, x(t), corresponds to a multiplication of that signal by an ideal impulse train.



Testing S/Hs

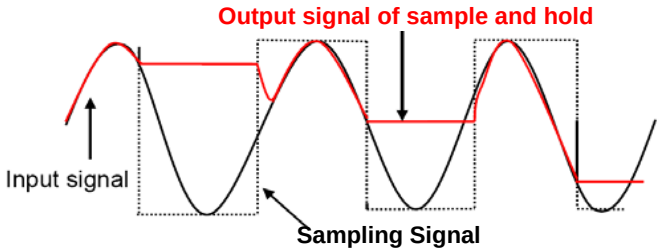
Test setup



where the S/H is operating at it's maximum sampling frequency f_{smpl}.

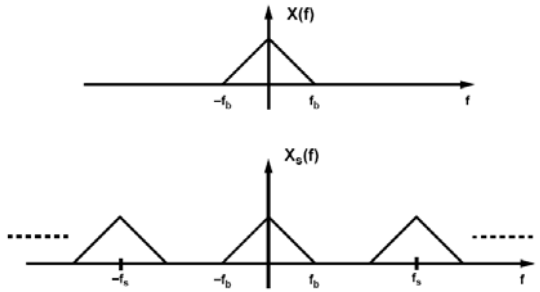
Testing S/Hs(Cont.)

•Example waveforms for the above test setup•



• The ideal sinusoidal wave at the beat frequency is subtracted from the measured signal. The error signal is then analyzed for RMS content and spectral components using FFT(fast Fourier Transform).

•In the frequency domain this is equivalent to convolving the input spectrum with a train of impulses and results in images of the input spectrum centered at integer multiples of the sampling frequency.



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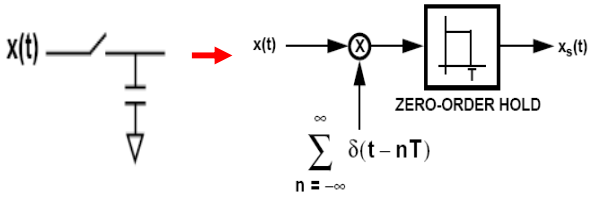
• Generally, it is necessary to "hold" the sampled signal for some period of time. A simple SAMPLE & HOLD circuit is formed by sampling switch followed by a hold capacitor. Ideally, this is equivalent to impulse sampling followed by a zero-order hold.



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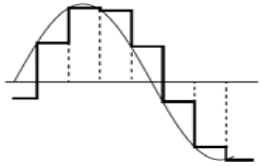
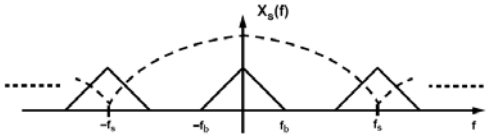
which results in a continuous time output waveform that steps between the sampled signal values



In the frequency domain, the continuous-time output of this sample & hold circuit consists of repeated images of band-limited input spectrum shaped by a sinc envelope.



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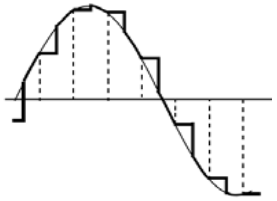
•In practice, it is not feasible to implement an impulse sampler in which the sampling switch is close and then opened in virtually "zero" time relative to the rate of change of the signal. Instead, the sampling switch and hold capacitor are operated as a TRACK & HOLD circuit. The switch is closed for some fraction of the sampling period, during which time the output "tracks" the input, and then is quickly opened at the sampling instant.



•In the frequency domain, the zeros of the sinc envelope are altered corresponding to the length fo the hold time. For example, it the hold time is $T_s/2 = 1/2f_s$, then the zeros of the sinc occur at integer multiples of $2f_s$.

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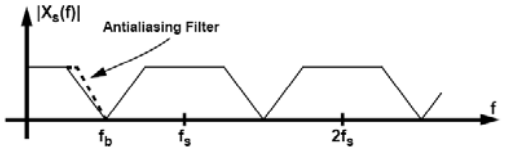
Classes of Sampling

NYQUIST-RATE SAMPLING

If signal has a bandwidth of f_b, then $f_s = 2f_b$.



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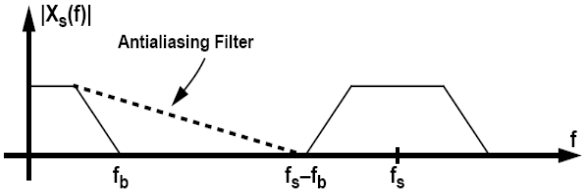
OVERSAMPLING

- **If signal has a bandwidth of fb, then $f_s >> 2f_b$**
- **Relaxes requirements on the preceding antialias filter.**
- **Reduces inband quantization noise when the sampler is followed by a quantizer.**



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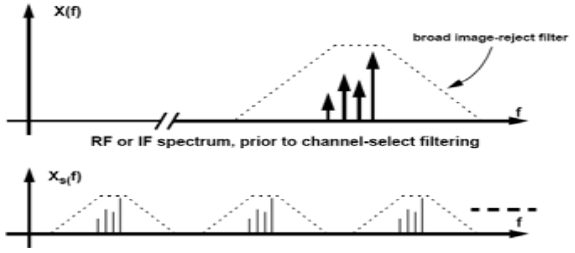
UNDERSAMPLING (also called SUBSAMPLING)

- **Sampling at a rate less than the Nyquist rate results in aliasing.**
- **But, if the signal is centered at an intermediate frequency and band-limited, it is not necessarily destructive.**
- **Undersampling can be exploited to mix a narrowband RF or IF signal down to a lower frequency. (P. Chan, et al., ESSCIRC, Sept. 1993)**



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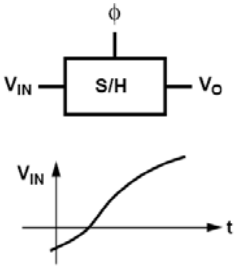
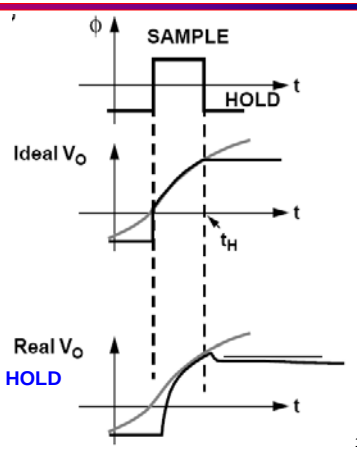
Sample & Hold Circuits

Ideal Track & Hold





REAL TRACK & HOLD

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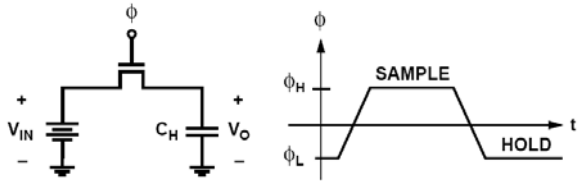
MOS Sample & Hold



Imperfections

- Non-zero acquisition time / Finite bandwidth in sample (track) mode
  - Acquisition time = τ

$\tau = R_{on}C_H$ $\qquad R_{on} = \dfrac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_T)}$

  - Bandwidth in sample mode =1/ τ

• EXAMPLE

W/L = 10 μm / 1 μm $\qquad$ V_T = 0.7 V

CH = 1 pF $\qquad$ μC_{ox} = 155.2 μA/V²

V_{IN}= 0 V $\qquad$ μ = 450 cm²/V-sec

φ_H = 3.3 V

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(\phi_H - V_{IN} - V_T)} = \frac{1}{(155.2)(10/0.8)(2.6)} = 198\Omega$$

$$BW \equiv \frac{1}{\tau} = \frac{1}{R_{on}C_H} = 5.05 \times 10^9 \text{rad/s} = 804\text{MHz}$$

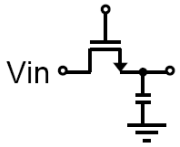
MOS S/H Basics

- Two error sources due to switch

a. channel charge injection

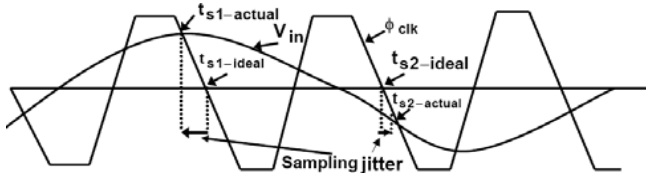
b. Clock feedthrough

where b is usually smaller than a



- Time jitter

–caused by clock waveforms having finite slopes



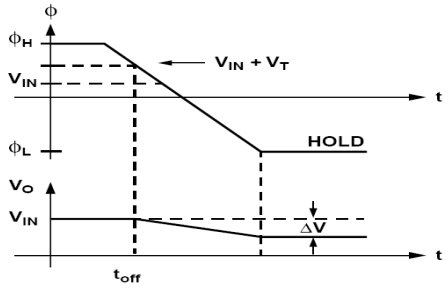
– When V_{in} is above 0V, the true sampling time is earlier than the ideal sampling time.

– When V_{in} is less than 0V, the true sampling time is late.

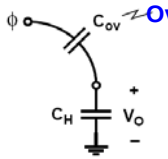
• S&H Pedestal Error

- error introduced at the S&H output during transition from sample to hold
- caused by charge injection
- depends on clock transition time (waveform of φ)

Quasi-Static (slow) Gating



• Channel charge has disappeared by t_{off} w/o introducing offset (all channel chg → V_{IN})
• For t > t_{off} ($\varphi < V_{IN} + V_T$)



At $\varphi = \varphi_L$ $\quad \Delta V = \left(\frac{C_{ov}}{C_{ov}+C_H}\right)(V_{IN}+V_T-\phi_L)$

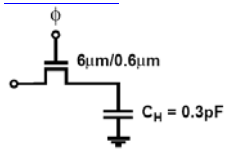
Thus, in the hold mode

$$V_O = V_{IN} - \Delta V = V_{IN} - \left(\frac{C_{ov}}{C_{ov}+C_H}\right)(V_{IN}+V_T-\phi_L)$$

$$\therefore\ V_O = (1+\varepsilon)V_{IN} + V_{os}$$

where $\varepsilon = -\frac{C_{ov}}{C_{ov}+C_H}$ $\qquad V_{os} = -(V_T-\phi_L)\left(\frac{C_{ov}}{C_{ov}+C_H}\right)$

EXAMPLE



$V_T = 0.7V$

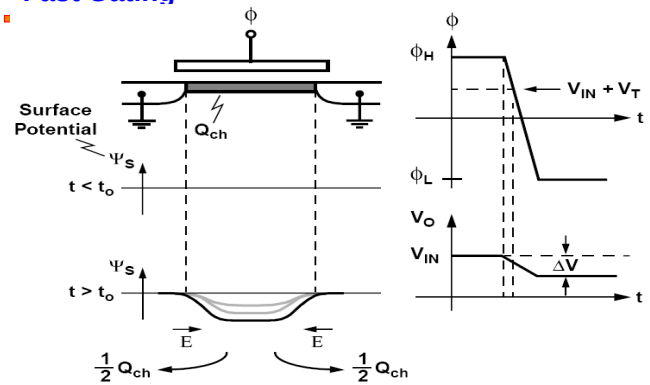
$\phi_L = 0V$

$C_{gdo} = 0.2fF/\mu m$

$$\varepsilon = -\frac{(6\mu m)(0.2fF/\mu m)}{(6\mu m)(0.2fF/\mu m)+0.3pF} = -\left(\frac{1.2fF}{0.3pF}\right) = -0.4\%$$

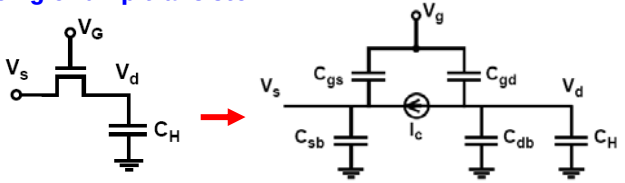
$$V_{os} = -(0.7V-0V)\left(\frac{1.2fF}{0.3pF}\right) = -2.8mV$$

Fast Gating

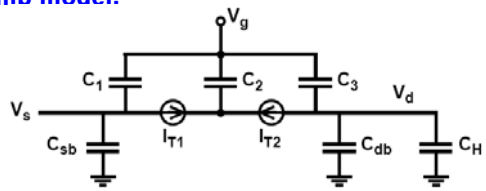


• Channel pinches off at source and drain
• Qch divides between source and drain depending on impedances loading these nodes

In the "fast gating"case, charge trapped in the channel is removed by diffusion to the source and drain The isolation of charge in the channel and its subsequent diffusion cannot be modeled with a single-lump transistor model.



- To model the isolation of channel charge in the fast-gating case, a distributed model (i.e. multiple lumps) must be used. The simplest of these is a two-lump model.



TWO-LUMP MODEL

Limiting Fast Case

- Assume that Qch divides equally between the input and output, which is true if CH is large and RS (source resistance) is small.

$$\Delta V = \left(\frac{C_{ov}}{C_{ov}+C_H}\right)(\phi_H-\phi_L)+\frac{1}{2}Q_{ch}\left(\frac{1}{C_H}\right)$$

$$Q_{ch} = C_{ch}[\phi_H-(V_{IN}+V_T)]$$

where

$$C_{ch} = C_{ox}\cdot W\cdot L_{ELEC} = C_{ox}(L-2L_D)W$$

$$\Delta V = \left(\frac{C_{ov}}{C_{ov}+C_H}\right)(\phi_H-\phi_L)+\frac{1}{2}\left(\frac{C_{ch}}{C_H}\right)(\phi_H-\phi_L-V_T)$$

Therefore, in the HOLD condition

$$V_O = V_{IN}-\Delta V = (1+\varepsilon)V_{IN}+V_{os}$$

where

$$\varepsilon = \frac{1}{2}\left(\frac{C_{ch}}{C_H}\right) = \frac{1}{2}\left(\frac{C_{ox}WL_{ELEC}}{C_H}\right)$$

$$V_{os} = -\left(\frac{C_{ov}}{C_{ov}+C_H}\right)(\phi_H-\phi_L)-\frac{1}{2}\left(\frac{C_{ch}}{C_H}\right)(\phi_H-V_T)$$

EXAMPLE

W/L = 10 μm / 1 μm	V_T = 0.7 V
C_H = 1 pF	C_{ox} = 3.54 fF/μm^2
φ_H = 3.3 V	C_{ov} = 0.3 fF/μm^2
φ_L = 0 V	L_D = 0.1 μm

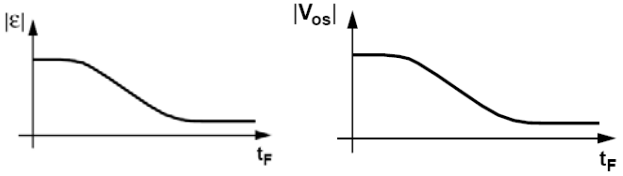
$C_{ch}=W(L-2L_D)C_{ox}=(10)(0.8)(3.54)= 28.3fF$

$$\varepsilon = \frac{1}{2}\left(\frac{28.3fF}{1pF}\right) = 1.4\%$$

$$V_{os} = -\left(\frac{3fF}{3fF+1pF}\right)(3.3V-0V)-\frac{1}{2}\left(\frac{28.3fF}{1pF}\right)(3.3V-0.7V)$$

$$\cong -9.9\ mV-36.8\ mV = -46.7\ mV$$

- In practice, $|\varepsilon|$ and $|V_{os}|$ decrease as the fall time of φ increases



S&H SPEED/ACCURACY TRADEOFF

•To first order, the worst case pedestal error is approximately

$$\Delta V_{error} = \frac{1}{2}\left(\frac{Q_{ch}}{C_H}\right)$$

while

$$BW \cong \frac{1}{\tau} = \frac{1}{R_{on}C_H}$$

where

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs}-V_T)} = \frac{L^2}{\mu C_{ox}WL(V_{gs}-V_T)} = \frac{L^2}{\mu Q_{ch}}$$

Thus

$$\frac{\Delta V_{error}}{BW} = \tau \cdot \Delta V_{error}$$

$$= \left(\frac{L^2 C_H}{\mu Q_{ch}}\right)\left(\frac{Q_{ch}}{2C_H}\right) = \frac{L^2}{2\mu}$$

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• EXAMPLE

W/L = 10 μm / 1 μm
C_H = 1 pF
V_{IN}= 0 V
φ_H = 3.3 V

VT = 0.7 V
μC_{ox} = 155.2 μA/V^2
μ = 450 cm^2/V-sec

$$BW \cong \frac{1}{\tau} = \frac{1}{R_{on}C_H} = 5.05\times10^9 \text{rad/s} = 804\text{MHz}$$

$$\tau \cdot \Delta V_{error} \cong \frac{(1\mu\text{m})^2}{1450\text{cm}^2/\text{V}-\text{s}} = 0.71\times10^{-12}\text{sec}-\text{V}$$

- Droop in Hold Mode
  - discharge of capacitor during hold mode
  - depends on leakage currents drawn by parasitic DC paths

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- Feedthrough
  - percentage of input signal that appears at output during hold mode
  - due to parasitic capacitive path between switch input and output terminals
- Dynamic Tracking Nonlinearity
  - input-dependent switch on-resistance introduces distortion
  - primarily a concern in high-speed sampling circuits
- Signal-Dependent Sampling Instant
  - due to finite clock transition time
  - primarily a concern when clock transition time is comparable with input signal slew rate

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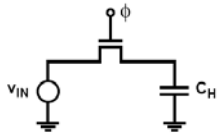
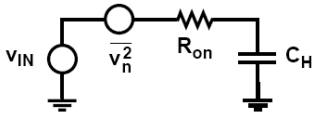
kT/C Noise

For a simple MOS sample & hold circuit



the equivalent circuit in the sample (track) mode is:



$$\overline{v_n^2} = 4kTR_{on}\Delta f$$

The total noise appearing across C_H is then

$$\overline{v_{oT}^2} = \int_0^\infty \overline{v_n^2}|H(f)|^2 df$$

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where $H(f) = \frac{1}{1+j2\pi f\tau} = \frac{1}{1+j2\pi R_{on}C_H f}$

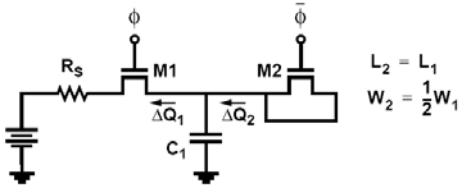
Thus, $\overline{v_{oT}^2} = 4ktR_{on}\int_0^\infty \frac{1}{1+(2\pi R_{on}C_H f)}df$

$$= 4ktR_{on}\left(\frac{1}{2\pi R_{on}C_H}\right)\int_0^\infty\left(\frac{1}{1+x^2}\right)dx = \frac{2kT}{\pi C_H}\left(\frac{\pi}{2}\right) = \frac{kT}{C_H}$$

Reduction of S&H Nonidealities

S&H Offset Cancellation

- **Dummy Switch**



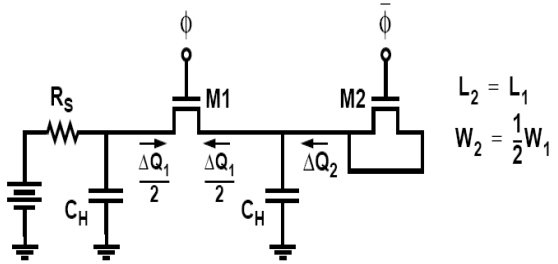
but

$$\Delta Q_2 = \Delta Q_{ov1} + \frac{1}{2}\Delta Q_{CH1}$$

$$\Delta Q_1 = \Delta Q_{ov1} + \alpha\left(\frac{\Delta Q_{CH1}}{2}\right)$$

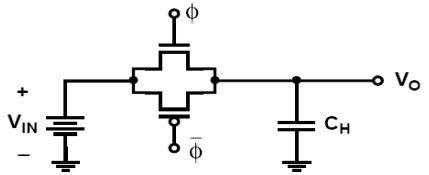
Problem: α not exactly = 1, especially if R_S is small

- **Dummy Switch w/ Equalizing Capacitor *(Bienstman & De Man, JSSC 12/80)***



- **Better cancellation**
- **Limits bandwidth in sample mode**

CMOS Sampling Switch



In the limiting "fast gating" case:

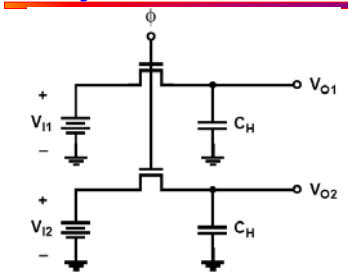
$$\frac{1}{2}|Q_{chN}| = \frac{1}{2}(\phi_H - V_{IN} - V_{TN})W_N L_N C_{ox}$$

$$\frac{1}{2}|Q_{chP}| = \frac{1}{2}(V_{IN} - \phi_L - |V_{TP}|)W_P L_P C_{ox}$$

$$\Delta V_O = -\frac{1}{2}\frac{|Q_{chN}|}{C_H} + \frac{1}{2}\frac{|Q_{chP}|}{C_H}$$

•Partial cancellation of the channel charge is achieved, but the cancellation is signal dependent.

Fully Differential Sampling



$$V_{O1} - V_{O2} = [V_{I1}(1+\varepsilon_1) + V_{os1}] - [V_{I2}(1+\varepsilon_2) + V_{os2}]$$

$$= (V_{I1} - V_{I2})\left[1 + \left(\frac{\varepsilon_1 + \varepsilon_2}{2}\right)\right] + V_{os1} - V_{os2} + (V_{I1} + V_{I2})\left(\frac{\varepsilon_1 - \varepsilon_2}{2}\right)$$

Thus

$$V_{O1} - V_{O2} = (V_{I1} - V_{I2})(1 + \varepsilon_D) + V_{os} + (V_{I1} + V_{I2})\varepsilon_C$$

$$\varepsilon_D = \frac{\varepsilon_1 + \varepsilon_2}{2} = \text{Differential-Mode Gain Error}$$

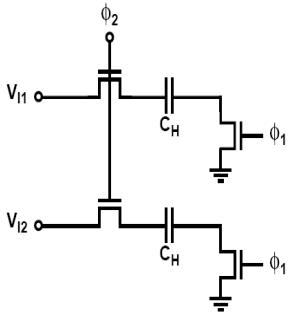
$$\varepsilon_C = \frac{\varepsilon_1 - \varepsilon_2}{2} = \text{Common-Mode Gain Error}$$

$$V_{os} = V_{os1} - V_{os2} = \text{Offset}$$

- V_{os} and common-mode gain error determined by mismatch
- Good CMRR and PSRR
- Insensitive to clock waveform
- Even with no mismatch, $V_{O1} - V_{O2} = (1 + \varepsilon_D)(V_{I1} - V_{I2})$

Bottom Plate Sampling

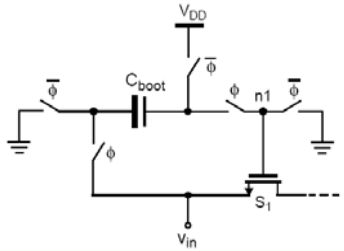
- Used to eliminate input-dependent charge injection error, which is present in differential S&H circuits.



- with φ_1 and φ_2 HIGH, VI1 and V_{I2} are tracked (sampled)
- first φ_1 –> LOW
  - V_{I1} and V_{I2} are held on CH's
  - charge injection is independent of V_{I1} and V_{I2}
- next φ_2 –> LOW
  - no charge injection since CH's are floating

Bootstrapping (Abo & Gray, JSSC 05/99)

- Used to eliminate dynamic tracking nonlinearities by reducing signal dependency of switch on-resistance.



- when φ LOW:
  - C_{boot} is precharged to V_{DD}
  - sampling switch is off
- when φ HIGH:
  - constant voltage, equal to V_{DD} is established between gate and source terminal of sampling switch

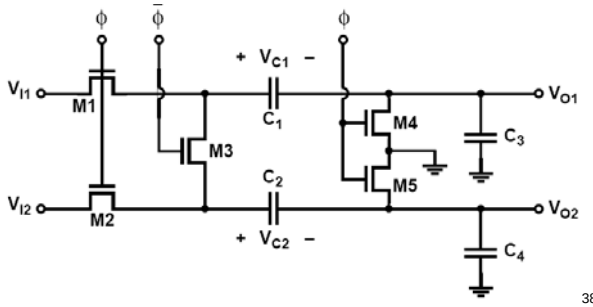
- ideally: switch on-resistance is independent of input signal
- in practice: parasitic capacitance at node n_1, C_{n1}, and dependence of VT on input voltage limit linearity that can be achieved

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W_1}{L_1}\left(\frac{C_{boot}}{C_{boot}+C_{n1}}V_{DD} - \frac{C_{n1}}{C_{boot}+C_{n1}}v_{in} - V_T\right)}$$

Switched-Capacitor Circuit

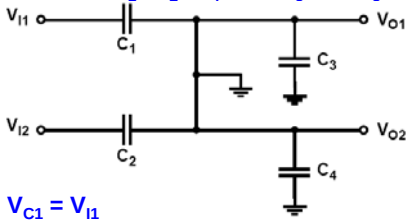
Common-Mode Cancellation

- In a fully differential sample & hold circuit, the common-mode input level can be removed with the following circuit (*Yen & Gray, JSSC 12/82*)



TRACK (SAMPLE) MODE (φ high)

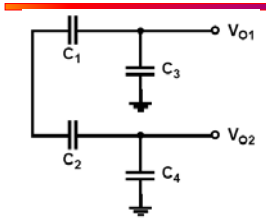
- Switches M_1, M_2, M_4 and M_5 on, M_3 off



$V_{C1} = V_{I1}$
$V_{C2} = V_{I2}$
$V_{O1} = V_{O2} = 0$

HOLD MODE (φ low)

First $\varphi 1$ ---> LOW, turning off M1, M2, M4 and M5
Then $\varphi 2$ ---> HIGH, turning on M3



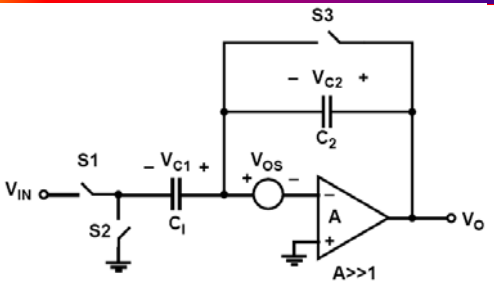
If $C_1 = C_2$ and $C_3 = C_4$, while transistor pairs M_1-M_2 and M_4-M_5 match, then

$$V_{O1} - V_{O2} = -(V_{I1} - V_{I2})\left(\frac{C_1}{C_1 + C_3}\right)$$

and

$V_{O1} + V_{O2} = 0$

Charge Redistribution Amplifiers



SAMPLE $S_1 = S_2 = 1$ (on)

$S_2 = 0$ (off)

$V_{C1} = V_{os} - V_{IN}$

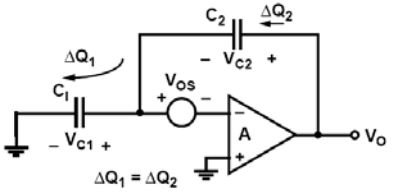
$V_{C2} = 0$

$V_O = V_{os}$

AMPLIFY

$S_1, S_3 \rightarrow 0$

$S_2 \rightarrow 1$



$V_{C1} \rightarrow V_{os}$

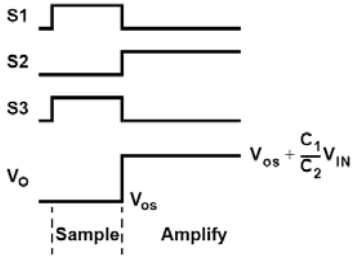
$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$

$\Delta Q_1 = C_1 \Delta V_{C1}) = C_1 V_{IN}$

$\Delta Q_2 = C_2 \Delta V_{C1}) = \Delta Q_1$

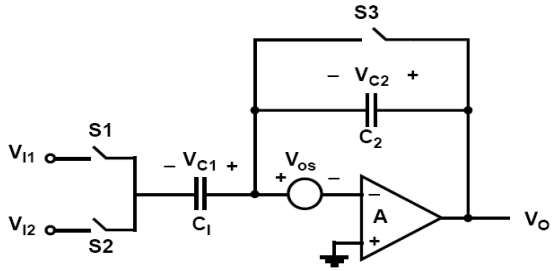
$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right) V_{C2} = V_{C2}$$

$$V_O = V_{C2} + V_{os} = \left(\frac{C_1}{C_2}\right) V_{IN} + V_{os}$$



- Offset is not cancelled, but it is NOT AMPLIFIED
- Input-referred offset = $(C_1/C_2)V_{os}$, where usually $C_2 < C_1$

INPUT DIFFERENCE AMPLIFIER



SAMPLE

$S_1 = S_3 = 1$, $S_2 = 0$

$V_{C1} = Vos - V_{I1}$

$V_{C2} = 0$

$V_O = Vos$

SUBTRACT & AMPLIFY

$S_1 = S_3 = 0, \quad S_2 = 1$

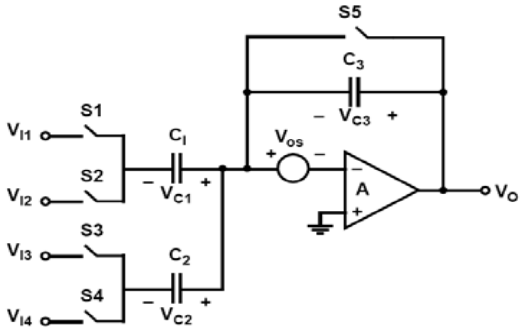
$V_{C1} = V_{os} - V_{I2}$

$\Delta V_{C1} = (V_{os2} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$$

$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$

SUMMING AMPLIFIER



SAMPLE $S1 = S3 = S5 = 1, S2 = S4 = 0$

$V_{C1} = V_{os} - V_{I1}$, $V_{C2} = V_{os} - V_{I3}$, $V_{C3} = 0$

$V_O = V_{os}$

AMPLIFY

$S1 = S3 = S5 = 0, S2 = S4 = 1$

$V_{C1} = V_{os} - V_{I2} \Rightarrow \Delta V_{C1} = V_{I1} - V_{I2}$

$V_{C2} = V_{os} - V_{I4} \Rightarrow \Delta V_{C2} = V_{I3} - V_{I4}$

$\Delta Q_1 = \Delta Q_1 + \Delta Q_2 = C_1 \Delta V_{C1} + C_2 \Delta V_{C2}$

$$\Delta V_{C3} = \frac{\Delta Q_3}{C_3} = \left(\frac{C_1}{C_3}\right)(V_{I1} - V_{I2}) + \left(\frac{C_2}{C_3}\right)(V_{I3} - V_{I4})$$

$$V_O = \left(\frac{C_1}{C_3}\right)(V_{I1} - V_{I2}) + \left(\frac{C_2}{C_3}\right)(V_{I3} - V_{I4}) + V_{os}$$

System Considerations

- Introduction
- Spectra of Sampled Signals
- Prefiltering
- Postfiltering
- Oversampling Approach
- Conventional Switched-Capacitor Approach
- Examples

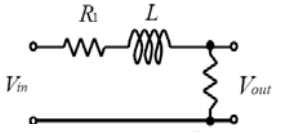
Filters

- Continuous-time filter
  - –RLC passive
  - –Active RC
- Sampled-Data filter
  - –Switched-Capacitor filter
- Digital filter

Continuous-Time Filters

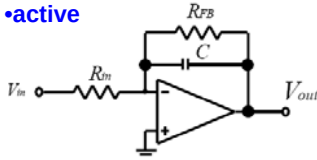
Example: 1 pole low pass filter

•passive



$$\frac{V_{out}}{V_{in}} = \frac{R_L}{R_1 + R_L}\left(\frac{1}{1+\frac{SL}{R_1+R_L}}\right)$$

•active



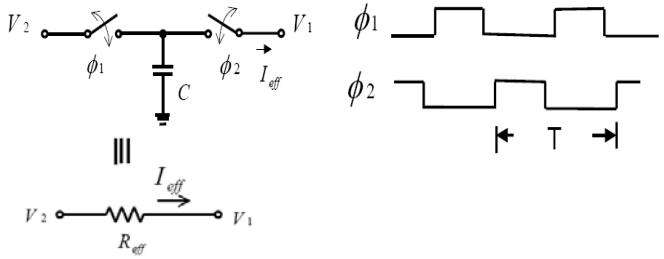
$$\frac{V_{out}}{V_{in}} = -\frac{R_{FB}}{R_{in}}\left(\frac{1}{1+SR_{FB}C}\right)$$

•Equivalence conditions:

$$R_{in} = R_1, \quad R_{FB} = \frac{R_1 R_L}{R_1 + R_L}, \quad C = \frac{L}{R_1 R_L}$$

Switched-Capacitor Filter

•Basic concept



$$\Delta Q = C(V_2 - V_1) \quad => \quad I_{eff} = \frac{\Delta Q}{T} = \frac{V_2 - V_1}{R_{eff}} \quad => \quad R_{eff} = T/C$$

SCF (Cont.)

•Example: SC integrator

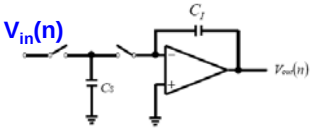
$$V_{out}(n) - V_{out}(n-1) = -\frac{C_S}{C_I}V_{in}(n-1)$$

$$=> \quad V_{out}(n) = V_{out}(n-1) - \frac{C_S}{C_I}V_{in}(n-1)$$

$$=> \quad V_{out}(z) = z^{-1}V_{out}(z) - \frac{C_S}{C_I}z^{-1}V_{in}$$

$$=> \quad H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_S}{C_I}\frac{z^{-1}}{1-z^{-1}} \quad where\ z = e^{j\omega T}$$

$V_{in}(n)$



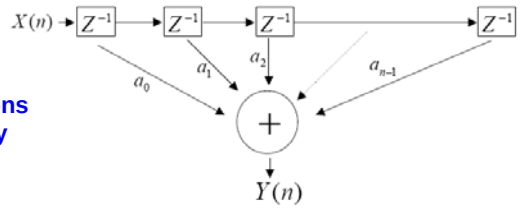
•If $\omega T << 1$

$$\lim_{\omega T<<1}\left[e^{j\omega T}\right] = -\frac{C_S}{C_I}\frac{e^{-j\omega T}}{1-e^{-j\omega T}} = -\frac{C_S}{C_I}\frac{\left[1 - ST + \frac{(ST)^2}{2} - \cdots\right]}{ST - \frac{(ST)^2}{2} + \cdots}$$

$$\approx -\frac{C_S}{C_I}\frac{1}{ST} = -\frac{1}{S\left(\frac{T}{C_S}\right)C_I} = -\frac{1}{SR_{eff}C_I}$$

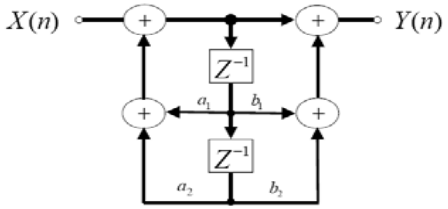
Digital Filter

•FIR

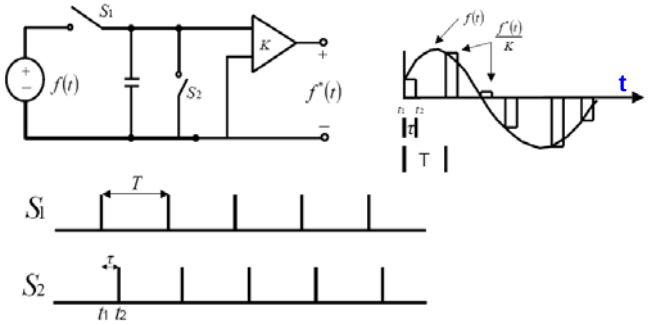


Operations
–multiply
–delay
–add

•IIR



Analog Sampling Circuit



- Original continuous-time signal f(t)
- Sampled/Held Signal f*(t)

Signal Spectra of Zero-Width Samples

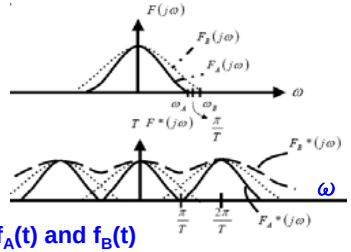
- For $\tau \longrightarrow 0$ (zero-width sampling)

$f(t) \longrightarrow F(jw)$ ..... original signal

$f^*(t) \longrightarrow F^*(jw)$ ..... sampled-data signal

•Spectrum of Sampled Signal

$$F^*(j\omega)=\frac{1}{T}\sum_{k=-\infty}^{\infty}F\left(j\omega-jk\frac{2\pi}{T}\right)$$



•Continuous-time signals $f_A(t)$ and $f_B(t)$
•Sampled-Data signals *(t) and $f_B^*(t)$

Nyquist Theorem

•There is a one-to-one relation between values

$$F_{A/B}(j\omega) \quad and \quad F_{A/B}{}^*(j\omega)$$

–Replicas forming $F_B(j\omega)$ overlap (This phenomenon is called aliasing or folding. It is a nonlinear distortion.)

•Low-pass Filter

$$F_A{}^*(j\omega)H(j\omega)=F_A(j\omega) \quad \text{where } H(j\omega)=\begin{cases}1 & ; \ |\omega|\le\frac{\pi}{T}\\ 0 & ; \ |\omega|>\frac{\pi}{T}\end{cases}$$

=>The continuous-time signal $f_A(t)$ is recovered.
But no such operation can regain $F_B(j\omega)$ from $F_B^*(j\omega)$

- Nyquist first observed this phenomenon
  =>Nyquist Theorem

Signal Spectra of S/H Samples

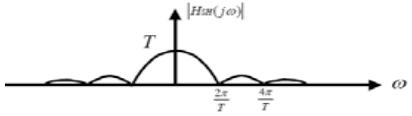
•Assume τ =T (Nonzero-width sampling)

$$F_{SH}(j\omega) = H_{SH}(j\omega)F^*(j\omega)$$

Where F*(jω) is the spectra of zero-width sample (refer to the second previous page)

$$H_{SH}(j\omega) = \frac{1-e^{-j\omega T}}{j\omega} = Te^{-\frac{j\omega T}{2}}\left(\frac{\sin\frac{\omega T}{2}}{\frac{\omega T}{2}}\right)$$

=> H_{SH}(jω) has a linear phase. Its amplitude has SinX/X response which is characteristic of S/H signal spectra

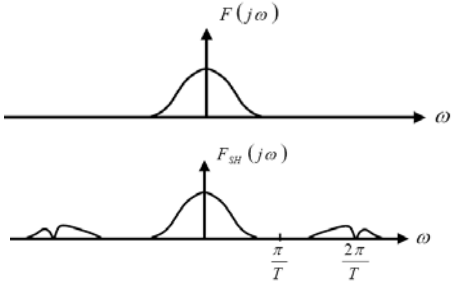


S/H Effect

$$F_{SH}(j\omega) = H_{SH}(j\omega)F^*(j\omega)$$

F(jω)* is formed by replicas of *F(jω)*

F(jω) is replicated and multiplied by theSinX/X response.



S/H Effect (Cont.)

- We look at the frequency response that occurs when we change a discrete-time signal back into an analog signal with the use of a sample-and-hold circuit. Note that here we plot a frequency response for all frequencies (as opposed to only up to f_s/2) since the output signal is continuous-time signal rather than a discrete-time one .
- A sample-and-hold signal, $x_{sh}(t)$, is related to its sampled signal by the mathematical relationship.

$$x_{sh}(t) = \sum_{-\infty}^{\infty} x_c(nT)\left[\vartheta(t-nT) - \vartheta(t-nT-T)\right] \qquad (9.37)$$

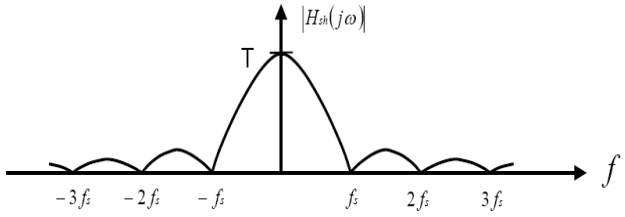
•Note that, once again, X_{SH}(s) is well defined for all time, and thus the Laplace transform can be found to be equal to

$$X_{sh}(s) = \frac{1-e^{-sT}}{s}\sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT} = \frac{1-e^{sT}}{s}X_s(s) \qquad (9.38)$$

S/H Effect (Cont.)

- This result implies that the hold transfer function , H_{sb}(s), is equal to

$$H_{sh}(s) = \frac{1-e^{-sT}}{s}$$



Sample-and-hold response (also called thesinc response).

S/H Effect (Cont.)

- It should be mentioned here that this transfer function usually referred to as the sample-and-hold response although, in fact it only accounts for the hold portion.
- The spectrum for $H_{sh}(s)$ is found by substituting, $s = j\omega$ into (9.39) resulting in

$$H_{sh}(j\omega) = \frac{1 - e^{-j\omega T}}{j\omega} = T \times e^{-j\omega T/2} \times \frac{\sin(\omega T/2)}{\omega T/2} \quad (9.40)$$

S/H Effect (Cont.)

- The magnitude of this response is given by

$$|H_{sh}(j\omega)| = T \frac{|\sin(\omega T/2)|}{|\omega T/2|}$$

or

$$|H_{sh}(f)| = T \frac{|\sin(\pi f/f_s)|}{|(\pi f)/f_s|}$$

and is often referred to as the (sinx)/x or sinc response. This magnitude response is illustrated in Fig . 11-13 .

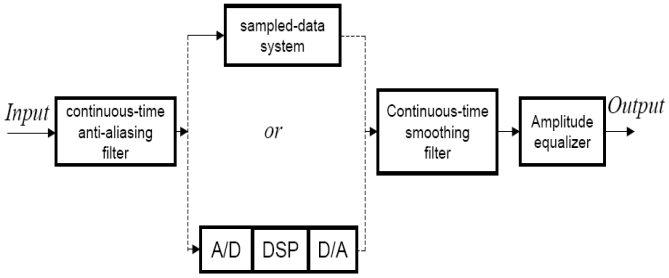
Sampled-Data System with Continuous-time Input & Output Signals

- The distortion due to $H_{SH}(j\omega)$ is linear as opposed to the nonlinear distortion which aliasingintroduces.
- $F(j\omega)$ can be recovered from $F_{SH}(j\omega)$ by two steps

1. Low-pass filter
2. Amplitude equalizer with a transfer function

$$H_{EQ}(j\omega) = 1/H_{SH}(j\omega)$$

Sampled-Data System with Continuous-time Input & Output Signals (Cont.)



- The anti-aliasing and smoothing filters can be identical lowpass filters, and should ideally have sharp cutoff frequency (except oversampling rate signal processing where Decimation and interpolation are used) .

Prefiltering

- Nyquist rate
  - –prefilter = anti-alias filter (AAF)
  - –Brick wall AAF
- Oversampling rate

prefilter= anti-alias filter + Decimation filter

(AAF) *(DF)*

AAF : continuous-time filter

DF : SCF or Digital filter

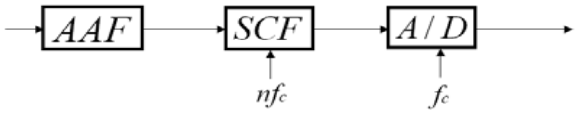
– usually < 60 dB or 10 bit
– small size

– usually used for resolution > 60 dB or 10 bit
– large size

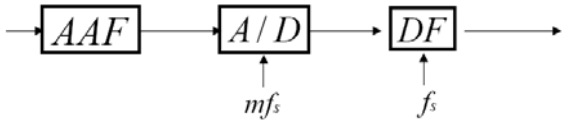
Prefiltering (Cont.)

- Examples: (For Data Acquisition)

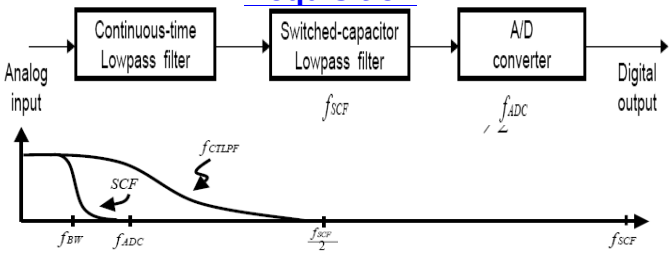
– conventional Nyquist-rate A/D converter



– oversampling A/D converter

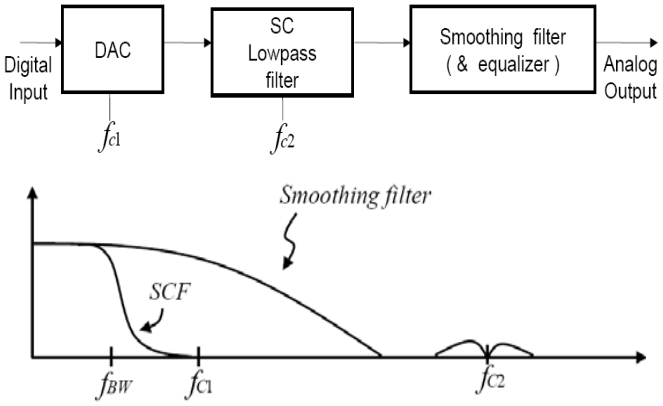


Prefilter Strategy for Conventional Data Acquisition

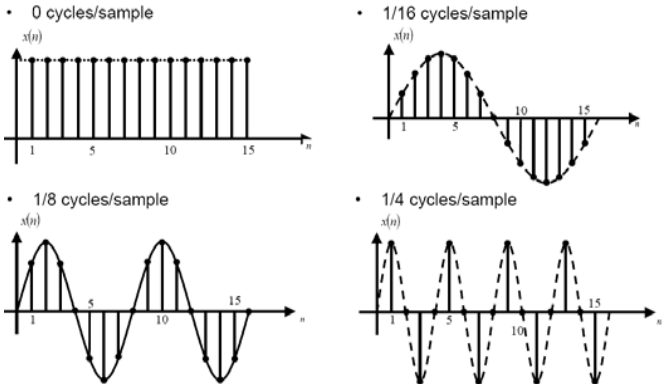


- Since $f_{SCF} >> f_{ADC}$ => decimation occurs without aliasing effect since SCF performs decimation and A/D conversion.
- Hence, ADC performs decimation and A/D conversion.
- Sometimes, SCF instead of ADC performs filtering and decimation. For either way, control clocks had better be synchronized.

Conventional Postfiltering



Some discrete-time sinusoidal signals with different sampling rates



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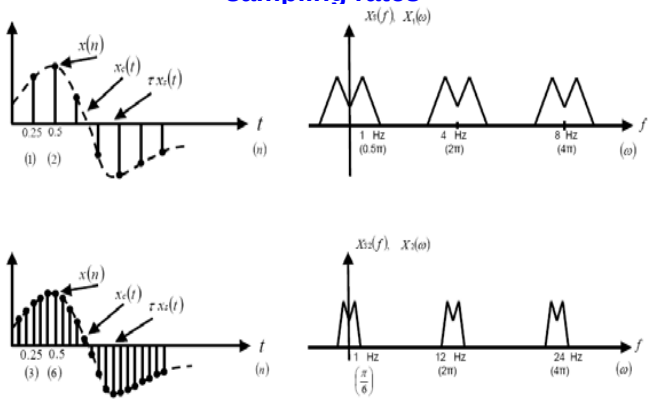
Comparison time and frequency of two sampling rates



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Use of OversamplingApproach to Relax Requirements of Prefilterand Postfilter

- **Front End**
  - **–Use oversamplingA/D converter**
  - **–Use decimation after A/D conversion**
- **Back End**
  - **–Use interpolation before D/A conversion**
  - **–Use oversampling D/A converter**

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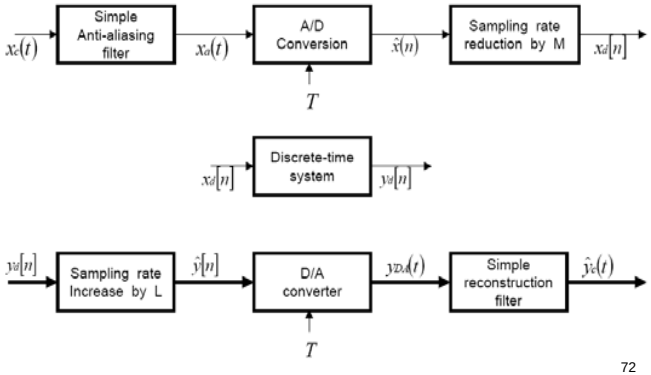
Use of OversamplingApproach to Relax Requirements of Prefilter and Postfilter (Cont.)

•Example: Block diagram of a signal processing system



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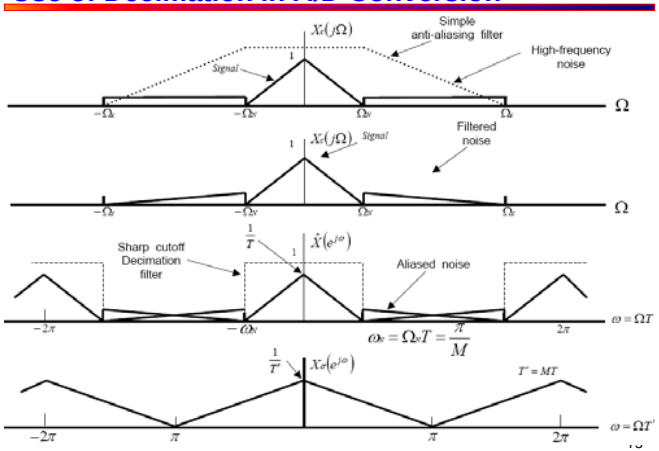
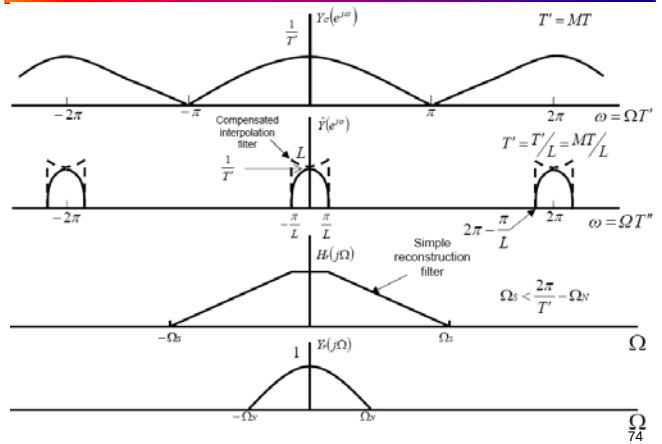
Use of Decimation in A/D Conversion



Use of Interpolation in D/A conversion



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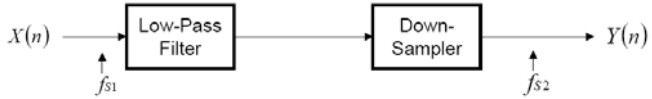
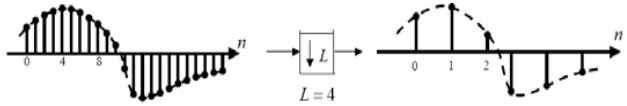
Decimation

- Lowpass filtering + downsampling



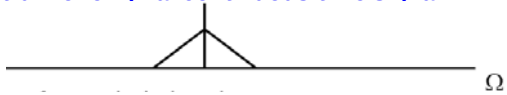
- Downsampling (by 4)
  - time-domain



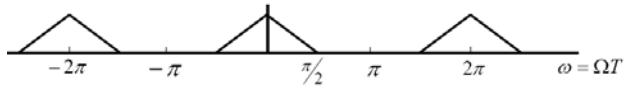
  - frequency domain

Decimation (Cont.)

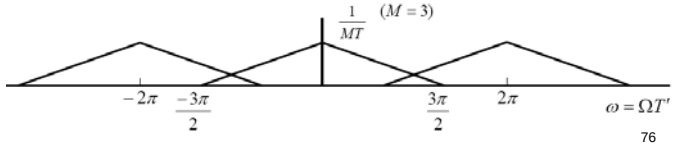
(a) spectrum of original continuous-time signal



(b) spectrum of sampled signal



(c) spectrum after decimation



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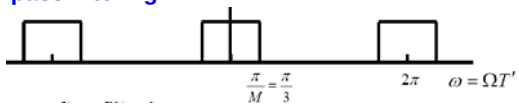
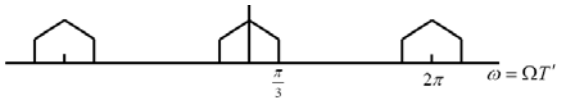
Decimation (Cont.)

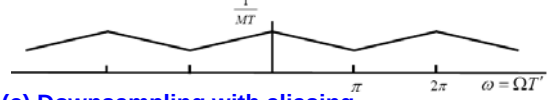
(d) Low-pass filtering



(e) Spectrum after filtering



(f) Spectrum after decimation



–(a)-(c) Downsampling with aliasing .

–(d)-(f) Downsampling with prefiltering to avoid aliasing

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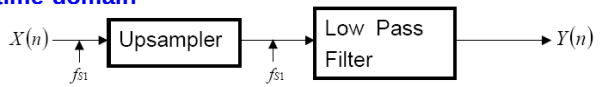
Interpolation

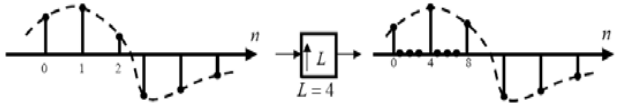
•Upsampling + lowpass filtering

–time-domain

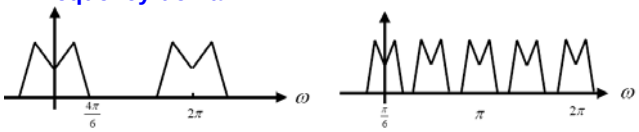


•Upsampling (by 4)

– time-domain

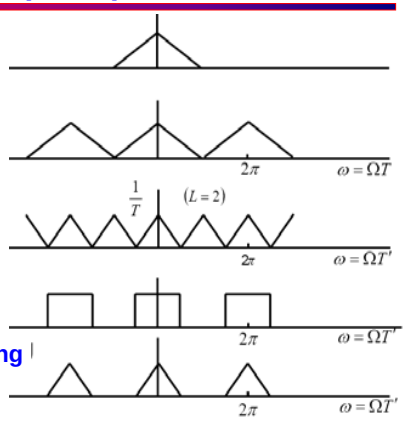


– Frequency-domain



Interpolation (Cont.)

- Baseband signal (Analog)
- Original signal (Digital)
- upsampling
- Low-pass filtering
- Specrumafter filtering



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Decimate-By-N Filter

- Example: with sincfunction

Input rate f_c

Output rate $f_c/N = f_d$

Y(n)=1/N[x(Nn)+x(Nn-1)+x(Nn-2)+……+x(Nn-N+1)]

$$Y(z)=\frac{x(z)}{n}\sum_{0}^{N-1}Z^{-i}=\frac{x(z)}{N}\left[\frac{1-z^{-N}}{1-z^{-1}}\right]$$

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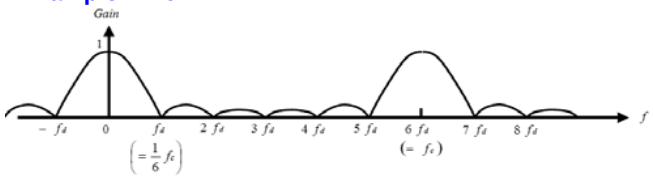
Decimate-By-N Filter (Cont.)

•Gain of sinc filter

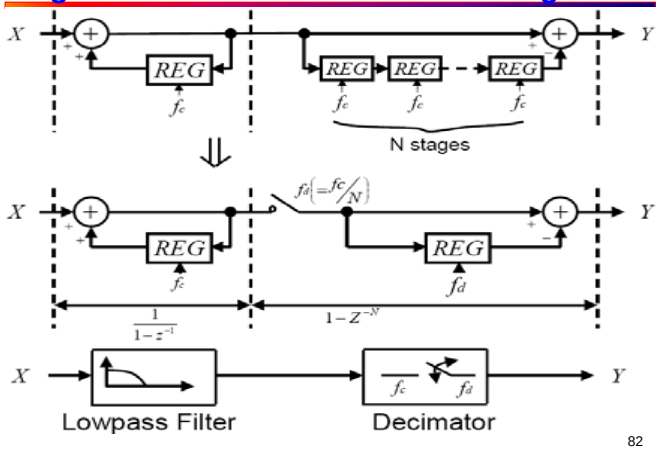
$$\frac{1}{N}\left|\frac{1-z^{-N}}{1-z^{-1}}\right| = \frac{1}{N}\left|\frac{\sin\frac{N\omega\tau}{2}}{\sin\frac{\omega\tau}{2}}\right| \quad ; \quad z = e^{j\omega\tau} \quad and \quad \tau = \frac{1}{f_c}$$

$$= \left|\frac{sinc\frac{N\omega\tau}{2}}{sinc\frac{\omega\tau}{2}}\right| \quad ; \quad sincX = \frac{\sin X}{X}$$

•Example: N=6

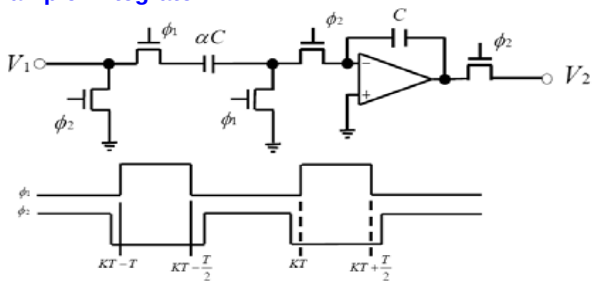


Digital Decimator with Sinc Filtering



SC Sampling Stage Without Decimation

•Example: Integrator

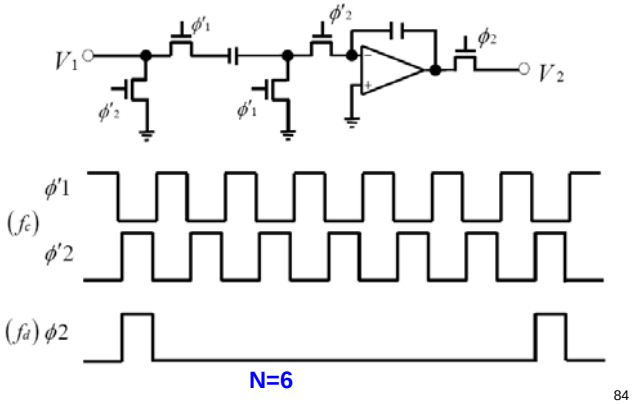


$$V_2(kT) - V_2(kT-T) = \alpha V_1\left(kT - \frac{T}{2}\right)$$

$$H_I(z) = \frac{V_2(z)}{V_1(z)} = \frac{\alpha z^{-\frac{1}{2}}}{1-z^{-1}}$$

SC Sampling Stage With Decimation

•Example: Modified Integrator



N=6

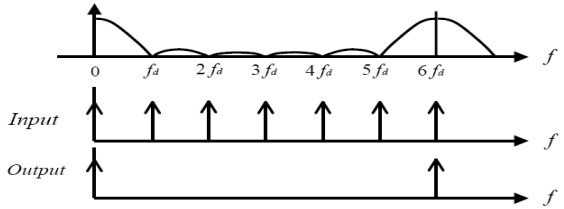
SC Sampling Stage With Decimation (Cont.)

$$H(z) = H_I(z) H_D(z)$$

where $H_D(z)$ is a sinc transfer function

$$\left|H_D\left(e^{j\omega\tau}\right)\right| = \left|\frac{\sin\frac{N\omega\tau}{2}}{\frac{\omega\tau}{2}}\right| \quad ; \quad \tau = \frac{1}{f_c} = T$$

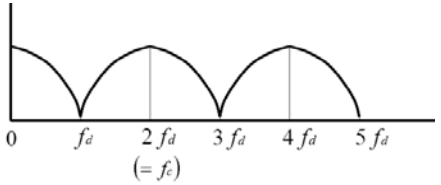
•Example : N=6



Cosine Filter

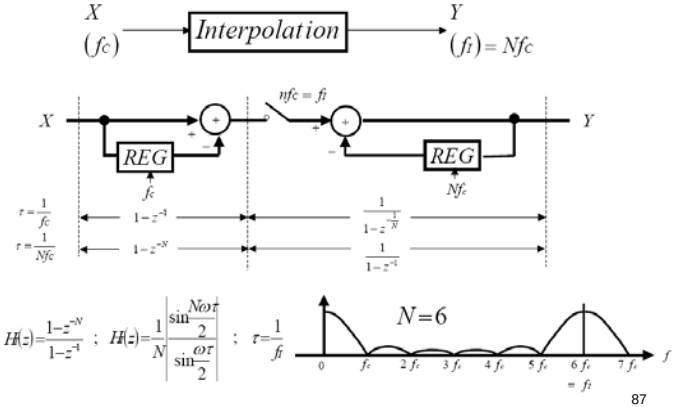
N = 2

$$\left|H_I\left(e^{j\omega\tau}\right)\right| = \left|\frac{\sin\omega\tau}{\sin\frac{\omega\tau}{2}}\right| \quad ; \quad \tau = \frac{1}{f_c}$$

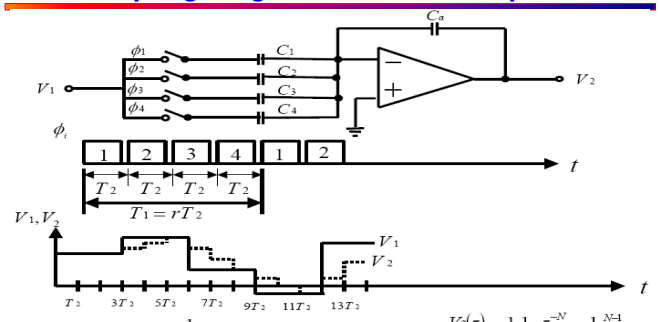


Interpolation Filter

•Example: Linear Interpolation (sincfunction)



SC Sampling Stage With Linear Interpolation

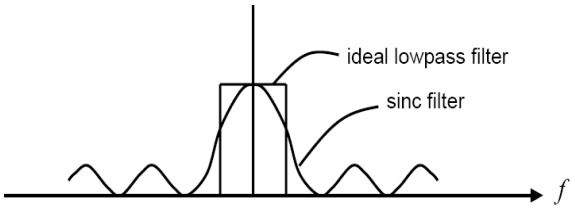


$$V_2(nT_2) - V_2(nT_2 - T_2) = \frac{1}{N}\left[V_1(nT_2) - V_1(nT_2 - NT_2)\right] \qquad H(z) = \frac{V_2(z)}{V_1(z)} = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} = \frac{1}{N}\sum_{i=0}^{N-1} z^{-i}$$

$$\left|H_I\left(e^{j\omega\tau}\right)\right| = \frac{1}{N}\left|\frac{\sin\frac{N\omega\tau}{2}}{\sin\frac{\omega\tau}{2}}\right| \quad ; \quad \tau = \frac{1}{f} = T_2$$

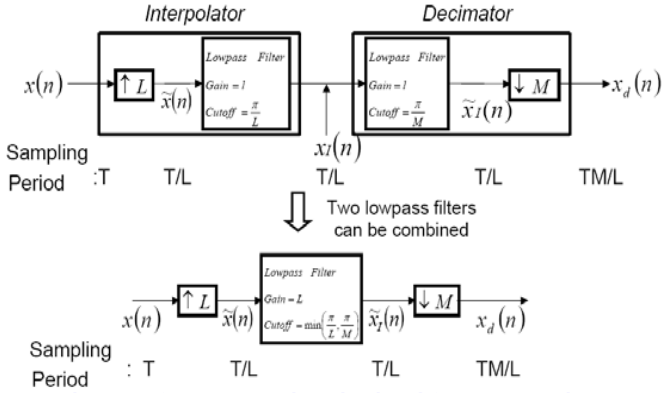
Sinc Filtering Function

- Not ideal lowpass
- FIR



- To implement ideal lowpass function, other approaches can be used.

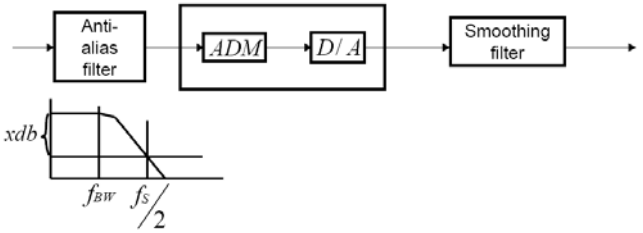
Changing The Sampling Rate By A Noninteger Factor



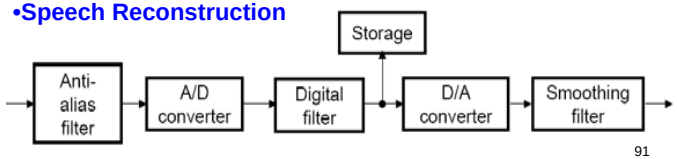
–Noninteger factors can be obtained from properly choosing M and L .

Examples

- Talking Back



- Speech Reconstruction



Examples (Cont.)

- Approach 1: better LPF can be used other than sinc one

continuous-time + oversampling + digital + DAC + SMF
AAF ADC Decimator and LPF

–oversampling ADC and digital decimator may be combined

- Approach 2:

continuous-time + SCF + conventional + digital + DAC + SMF
AAF ADC (Nyquist rate) Decimator and LPF

No cost factor is considered.

Ex14_SamplingandHold

1. A basic track and hold circuit is shown in the following figure. It consists of an NMOS switch S1 and a hold capacitance, C_H. Assume V_{DD}= 3.3V and that the substrate is tied to V_{SS}= 0V. Also assume the input signal Vi has a full scale range from 0 to 2V. You are to model the transistors using the Level 1 model and assume that T = 25˚C. Ignore any parasitic capacitances in your calculation unless otherwise mentioned.

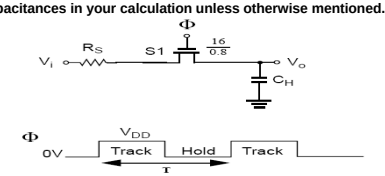


Fig. 1

(a) Consider the case when the voltage clock signal goes high to initiate the tracking phase. The holding capacitor CH starts charging through RS and the NMOS switch. What is the minimum value of the sampling capacitor so that the rms noise contribution of the MOS switch becomes less than 1/4LSB after sampling, if this circuit is used in a 14-bit A/D converter?

(b) The finite bandwidth of the track and hold circuit introduces a minimum acquisition time for the voltage at the output to track the voltage at the input to within a given accuracy (1/2 LSB of the resolution envisioned). If the clock has a 50% duty cycle, calculate the maximum frequency at which a steady input can be sampled to within 14 bits of resolution at the end of the tracking phase. In your calculations, use the worst-case value of the MOS switch "on" resistance, i.e., the value that would result in the slowest response. Assume C_H= 5pF and R_S=50Ω.

2. For the op-amp in the circuit, Av=200000, assume Vout = 6 V if V+ > V- , Vout = 0 V, if V+ < V-, and the currents into the + and – inputs are negligible.
(a) When Vin = 0 V, Vout = 6 V, find V+ = ?
(b) Find the values of Vin for which the output high-to-low (Vd) and low-to-high (Vu) transitions occur.
(c) Make a graph of Vout vs. Vin for 0 ≦Vin≦6V indicating the transition voltage Vd and Vu. How would you classify this circuit (i.e. does it have an name) ?