Agilent EEsof EDA

Presentation on Power Amplifier Design using ADS

Agilent Technologies

Power Amplifier Design using ADS

PA Workshop

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Agilent Technologies

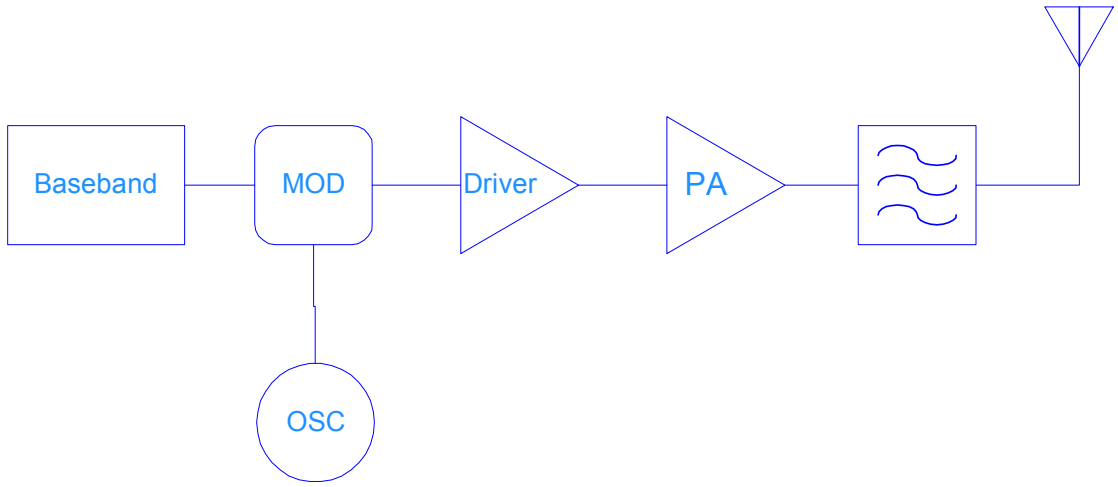
Outline

- Introduction
- DC and Loadline analysis
- Bias and Stability
- LoadPull
- Matching using Smith Chart Utility
- SourcePull
- PA Characterization – Did we meet the specification?
- Optimize/Fine Tune the design
- Test Design with real world modulated signals
- Layout

Why do we need a Power Amplifier?

Power Amplifiers (PA) are in the transmitting chain of a wireless system. They are the final amplification stage before the signal is transmitted, and therefore must produce enough output power to overcome channel losses between the transmitter and the receiver.

Basic Transmitter



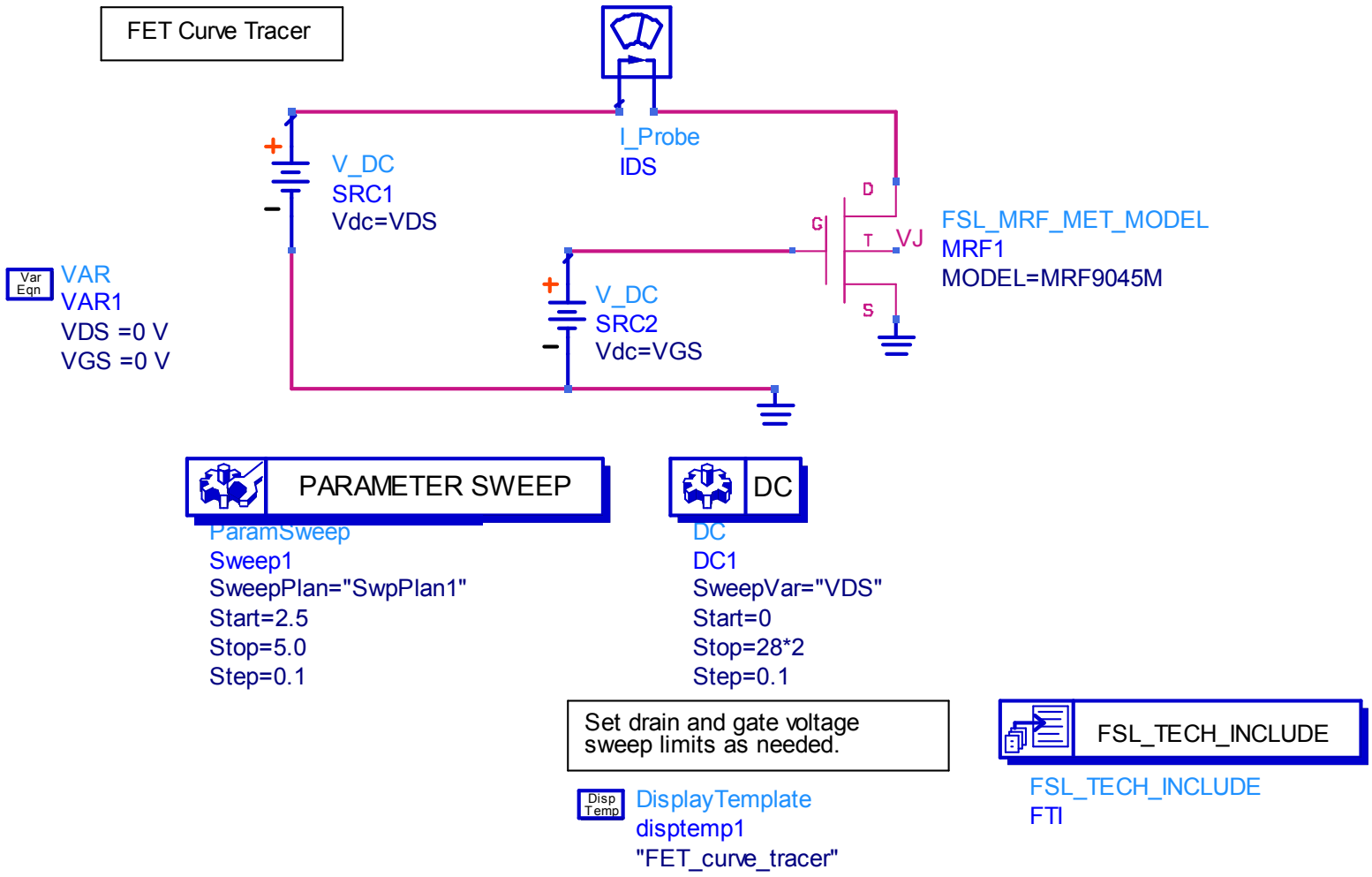
PA requirements

- The PA is typically the primary consumer of power in a transmitter. A major design requirement is how efficiently the PA can convert DC power to RF output power.
- The design engineer has to often concern himself with the Efficiency of the Power Amplifier. Notice that efficiency translates into either lower operation cost (e.g. cellular basestation) or longer battery life (e.g. wireless handheld).
- PA linearity is another important requirement, the input/ output relationship must be linear to preserve the signal integrity.
- The design of PAs often involves the tradeoff of efficiency and linearity.

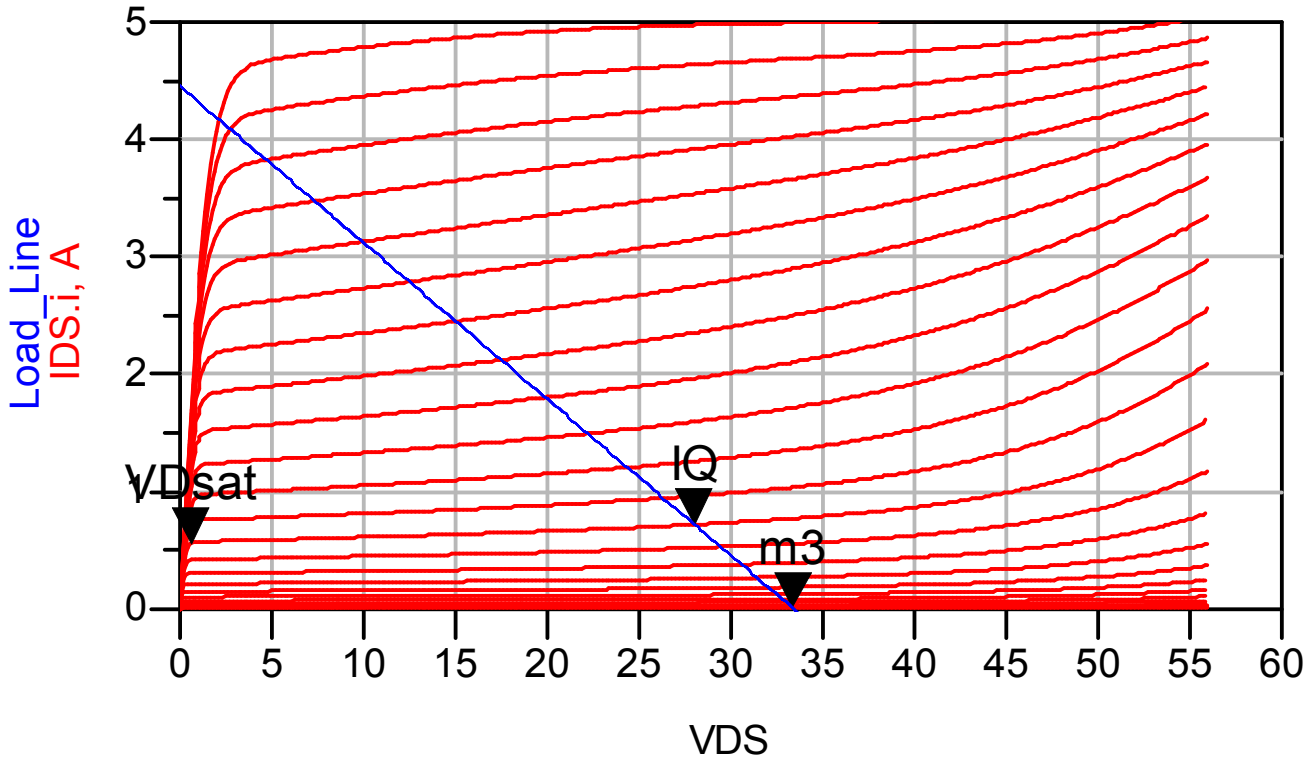
PA Design Requirement

- RF Output Power: 50 W PEP
- Input Drive Level : 1 W
- Output Load (RL): 50 Ω
- Efficiency (η) > 50%
- Bias Voltage: 28 V
- Device: MRF9045M

DC Curves

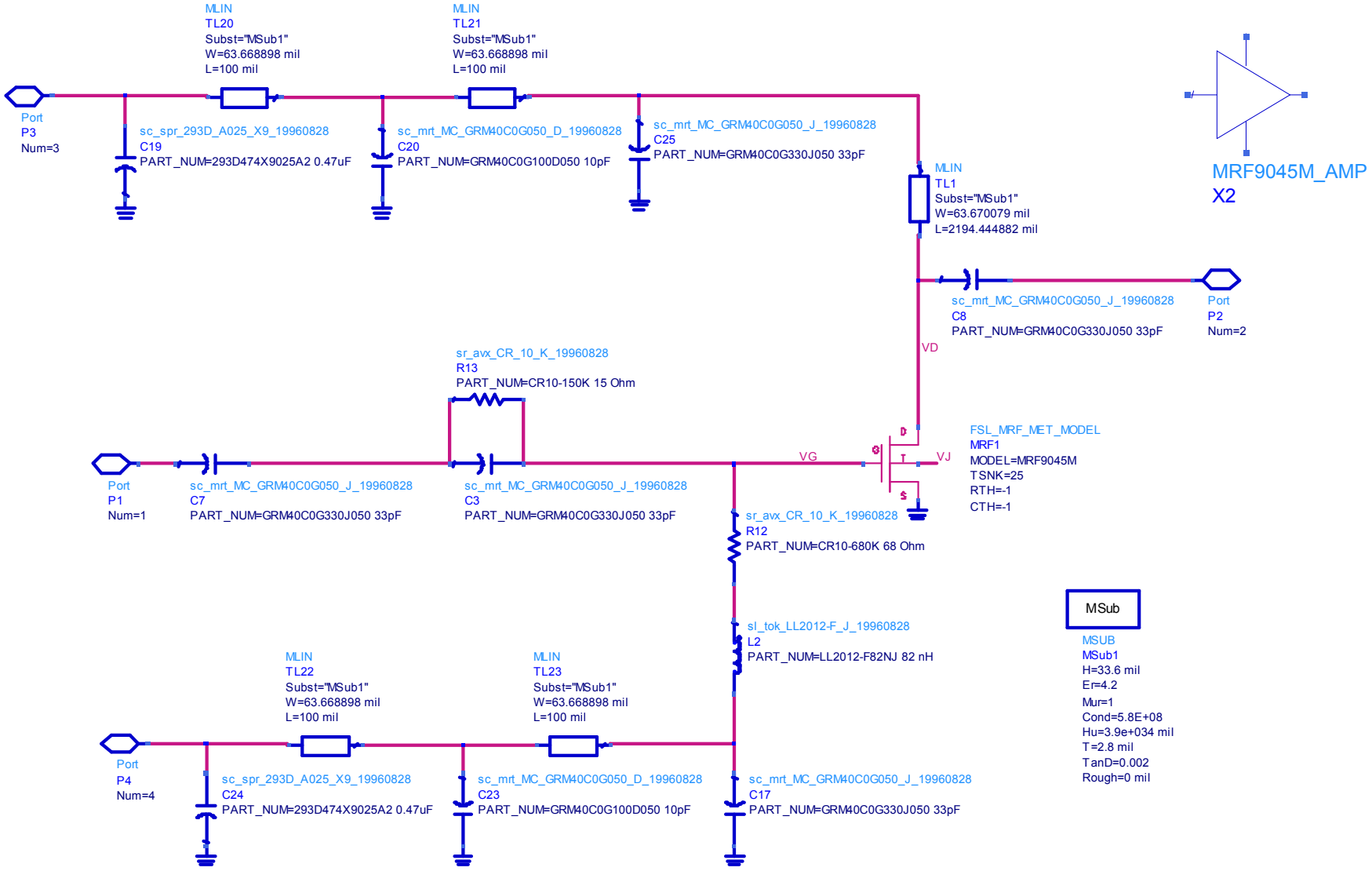

FET Curve Tracer
I_Probe
IDS
V_DC
SRC1
Vdc=VDS
D
G
T
VJ
S
FSL_MRF_MET_MODEL
MRF1
MODEL=MRF9045M
Var Eqn
VAR
VAR1
VDS =0 V
VGS =0 V
V_DC
SRC2
Vdc=VGS
PARAMETER SWEEP
ParamSweep
Sweep1
SweepPlan="SwpPlan1"
Start=2.5
Stop=5.0
Step=0.1
DC
DC
DC1
SweepVar="VDS"
Start=0
Stop=28*2
Step=0.1
Set drain and gate voltage sweep limits as needed.
Disp Temp
DisplayTemplate
disptemp1
"FET_curve_tracer"
FSL_TECH_INCLUDE
FSL_TECH_INCLUDE
FTI

DC Curves

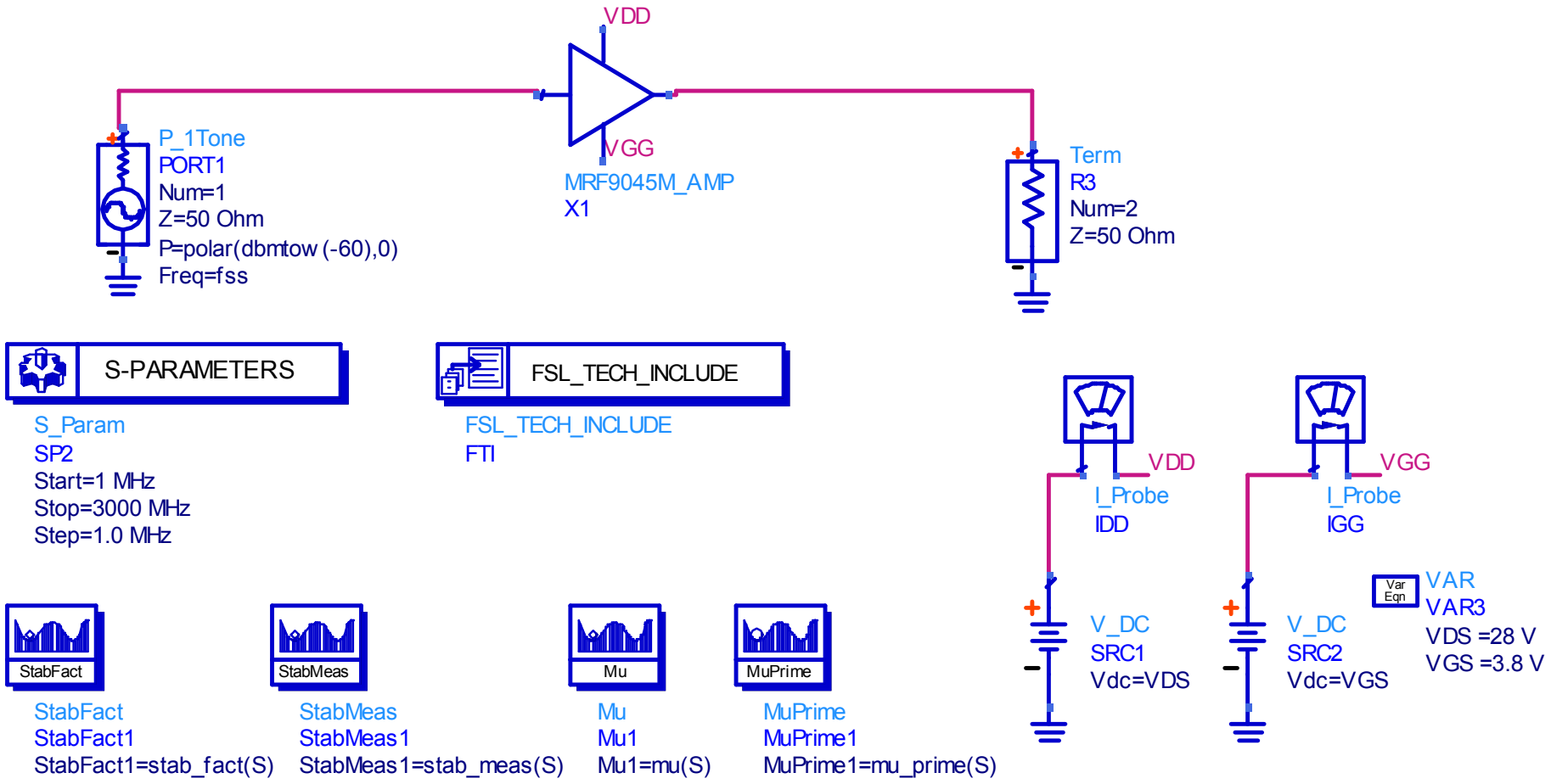


VDsat	IQ	m3
VDS=0.600	VDS=28.000	VDS=33.400
IDS.i=0.562	IDS.i=0.717	IDS.i=0.004
VGS=3.800000	VGS=3.800000	VGS=2.500000

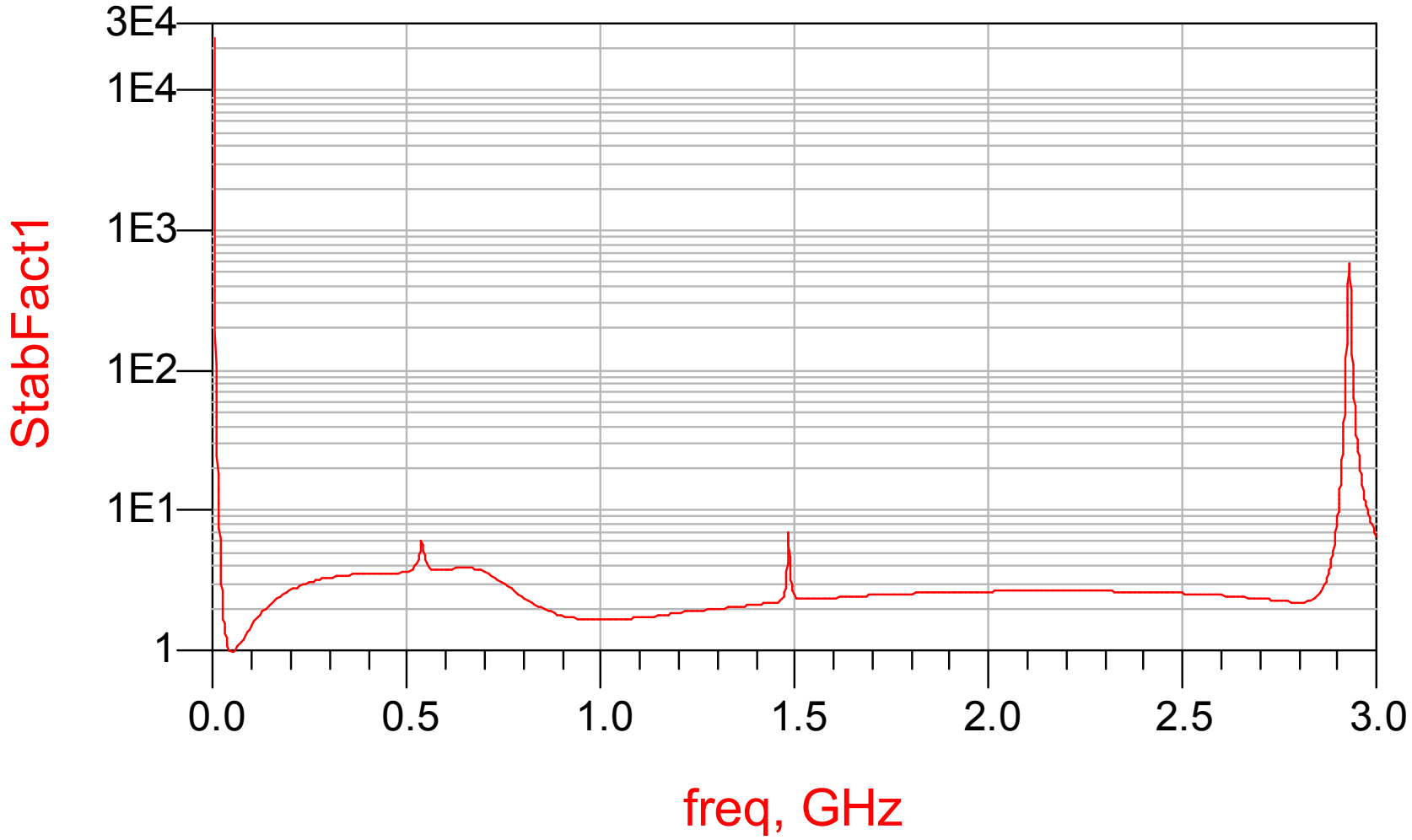
Bias and Stability



Stability Analysis



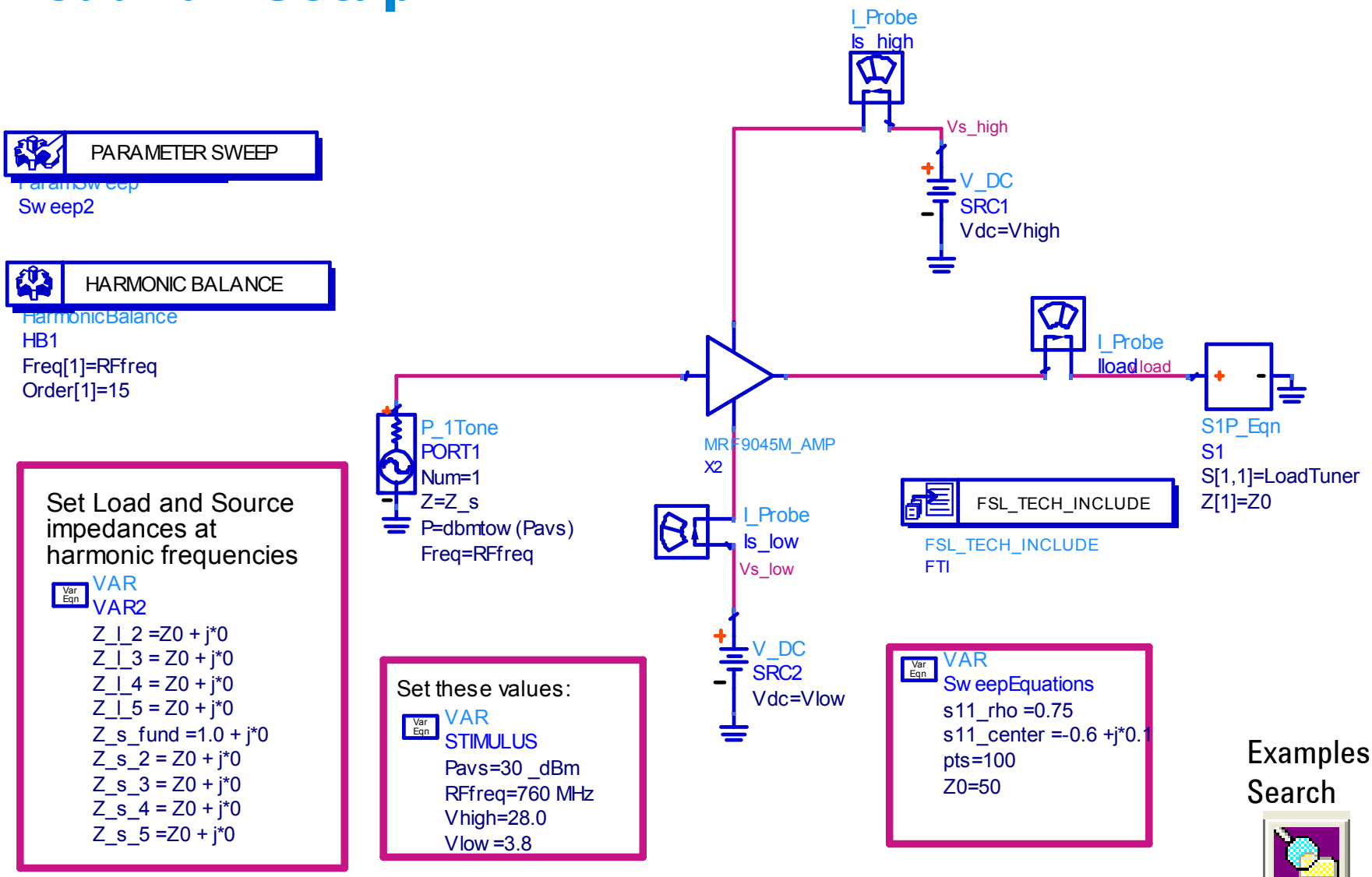
Stability Analysis



Impedance Matching

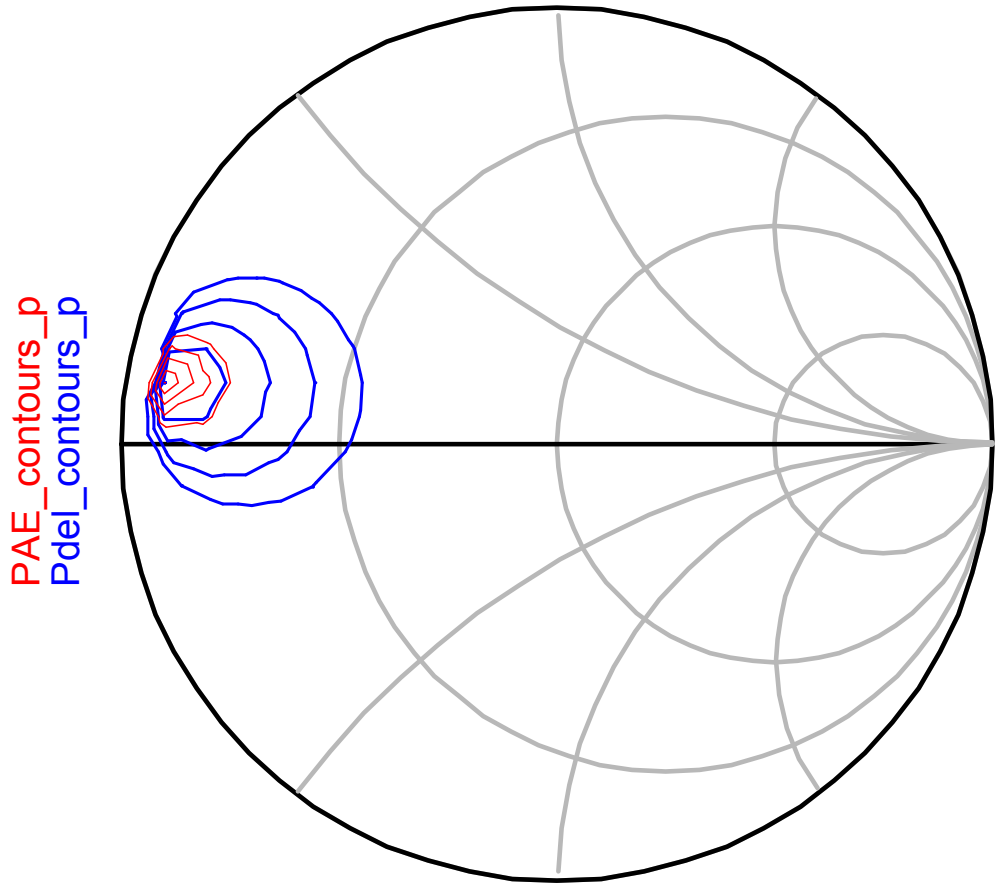
- The need for matching circuits is because amplifiers, in order to perform in a certain way(e.g. maximize output power), must be presented with a certain impedance at both the load and the source ports.
- For example in order to deliver maximum power to the load R_L the transistor must have termination Z_s and Z_L.
- The input matching network is designed to transform the generator impedance R_s to the optimum source impedance Z_s.
- The output matching network transform the load termination R_L (50 Ω) to the optimum load impedance Z_L.
- A LoadPull measurement will help the designer determine the optimum load impedance Z_L.

LoadPull Setup



Examples Search

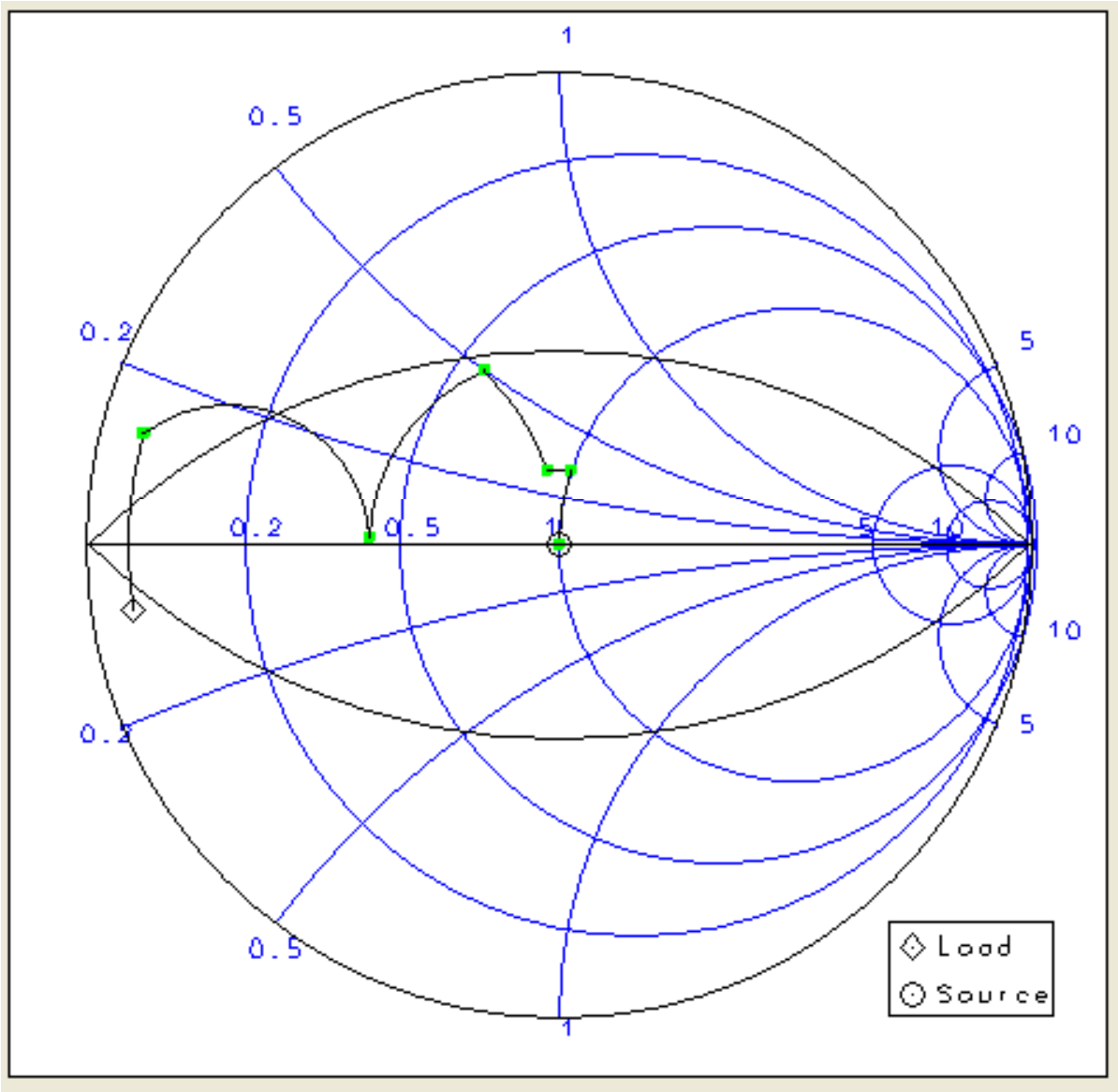
LoadPull Contours



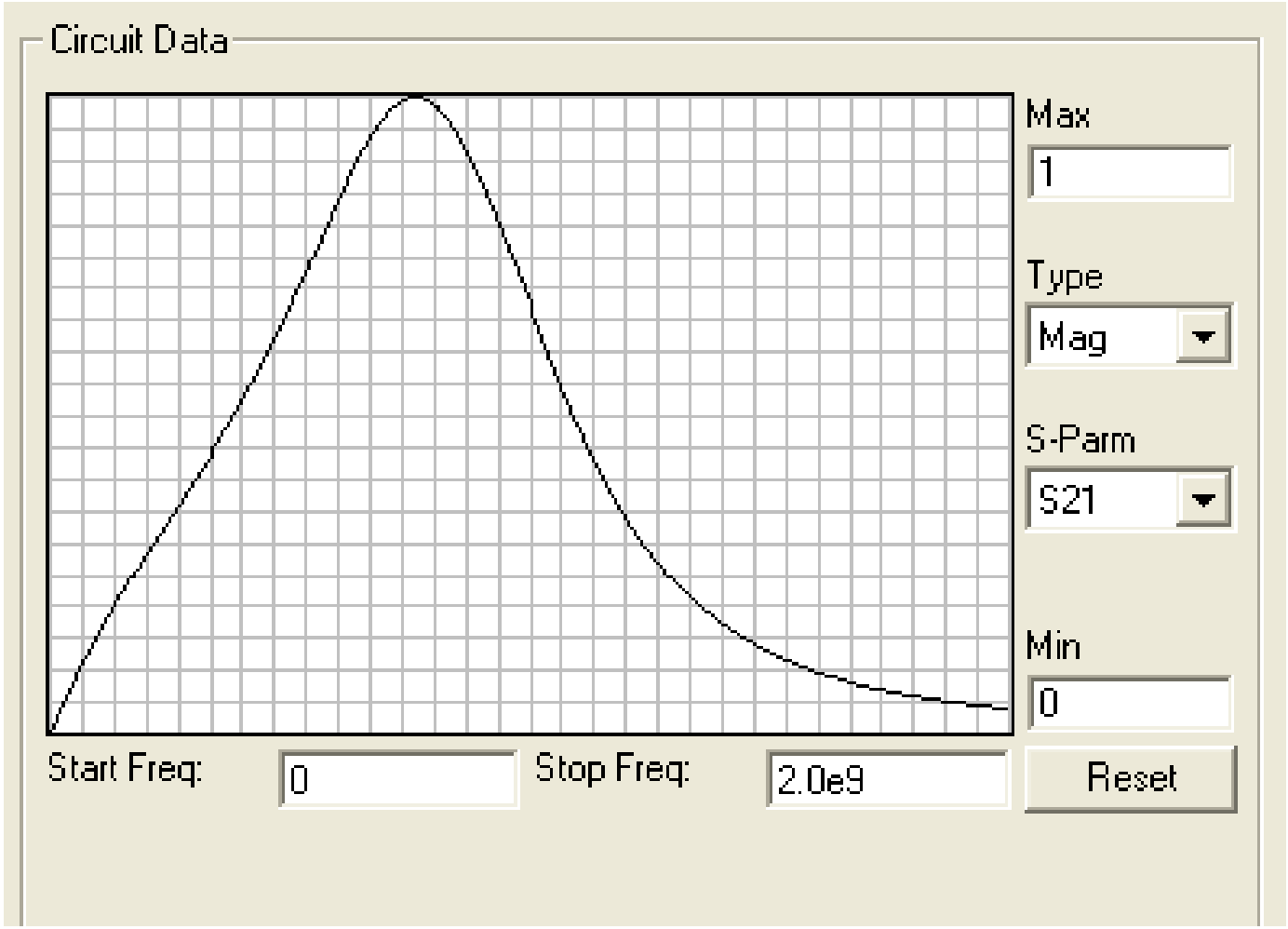
m2
indep(m2)=6
Pdel_contours_p=0.914 / 171.170
level=44.195857, number=1
impedance = 2.265 + j3.852

m1
indep(m1)=6
PAE_contours_p=0.914 / 171.180
level=47.552308, number=1
impedance = 2.265 + j3.848

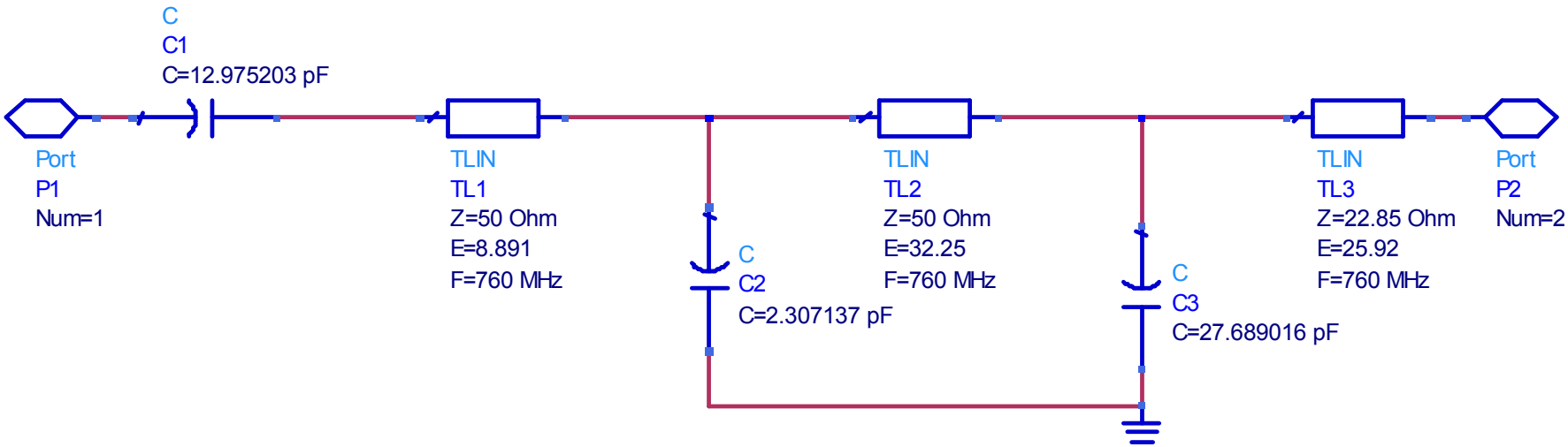
Matching using Smith Chart Utility

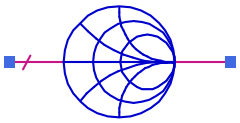


Matching using Smith Chart Utility



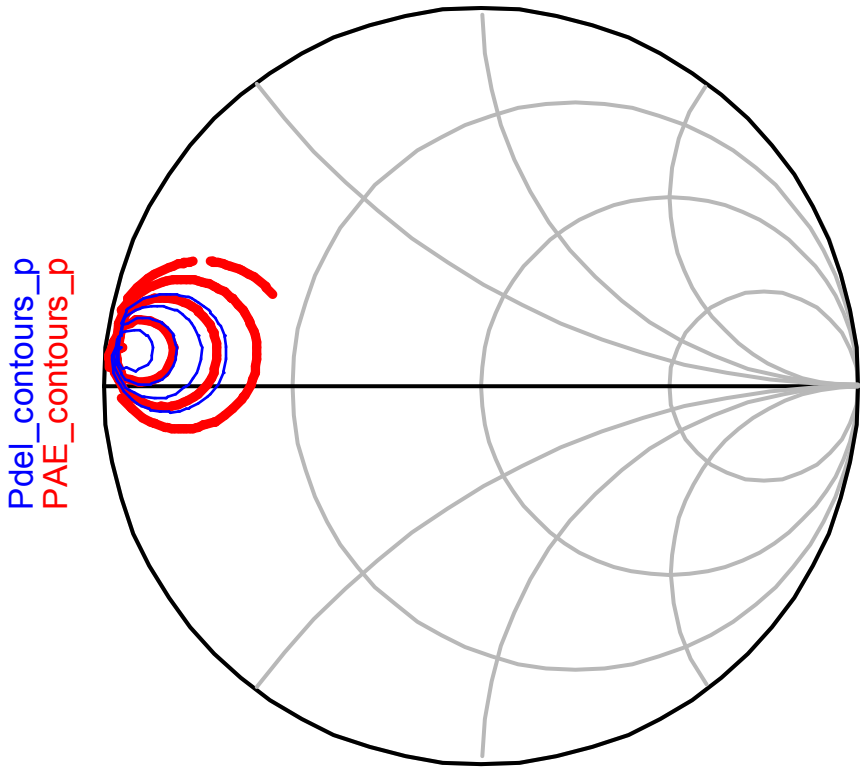
Output Match





DA_SmithChartMatch1_output_match_design
DA_SmithChartMatch1
F=760 MHz
Zs=50 Ohm
Zl=(2.300-j*3.800) Ohm
Z0=50 Ohm

SourcePull Contours

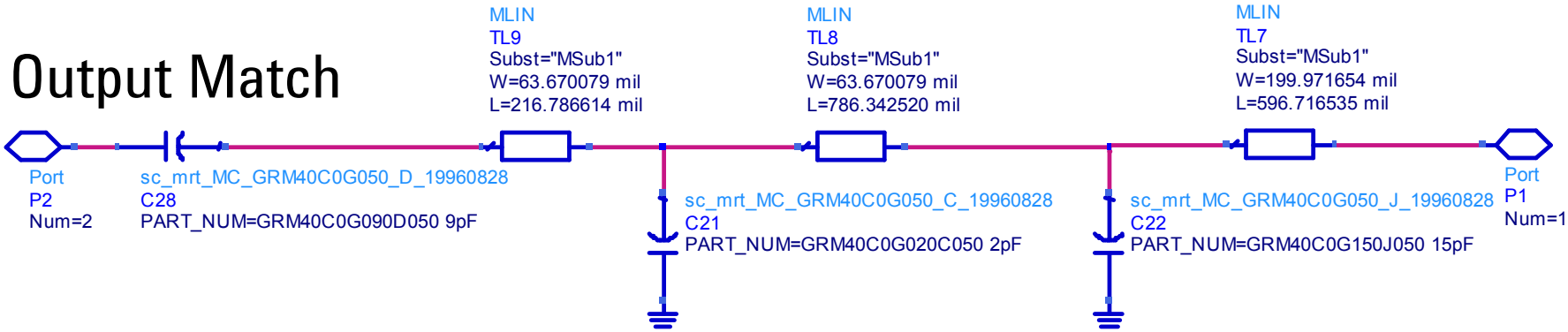


m2
indep(m2)=4
Pdel_contours_p=0.960 / 174.023
level=46.038749, number=1
impedance = 1.016 + j2.609

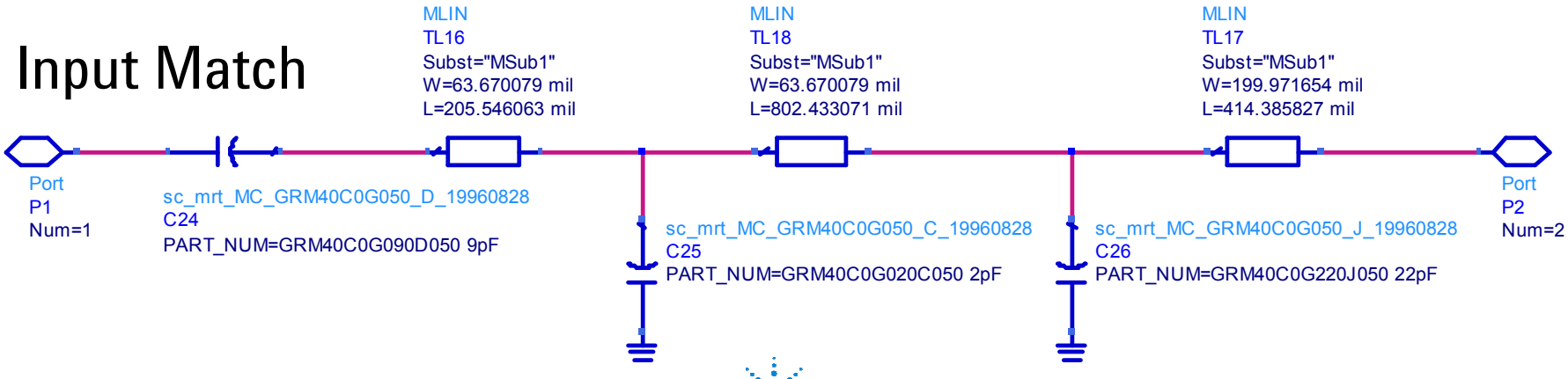
m1
indep(m1)=4
PAE_contours_p=-0.952 + j0.100
level=58.130703, number=1
impedance = 1.096 + j2.618

Matching Circuits

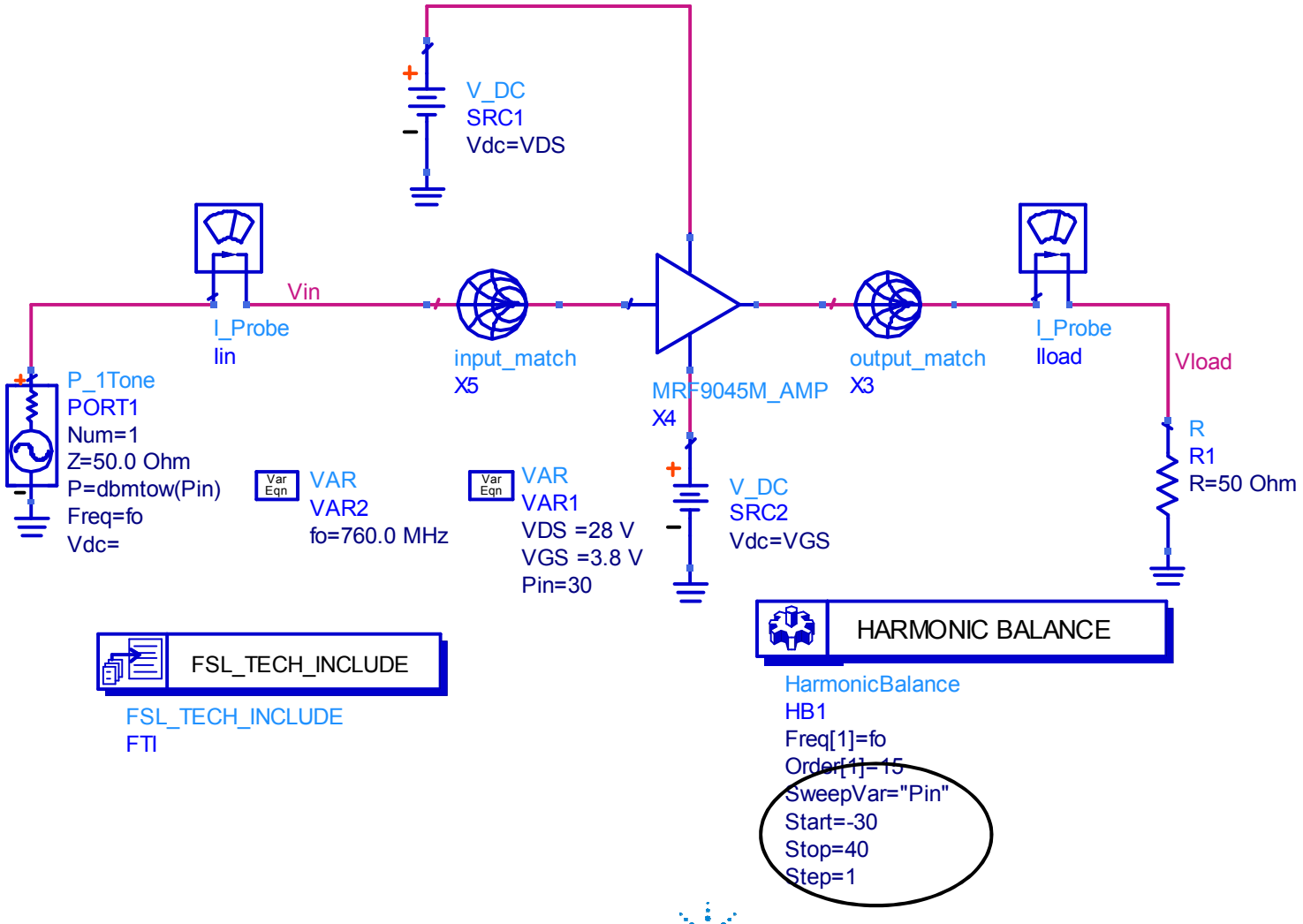
Output Match



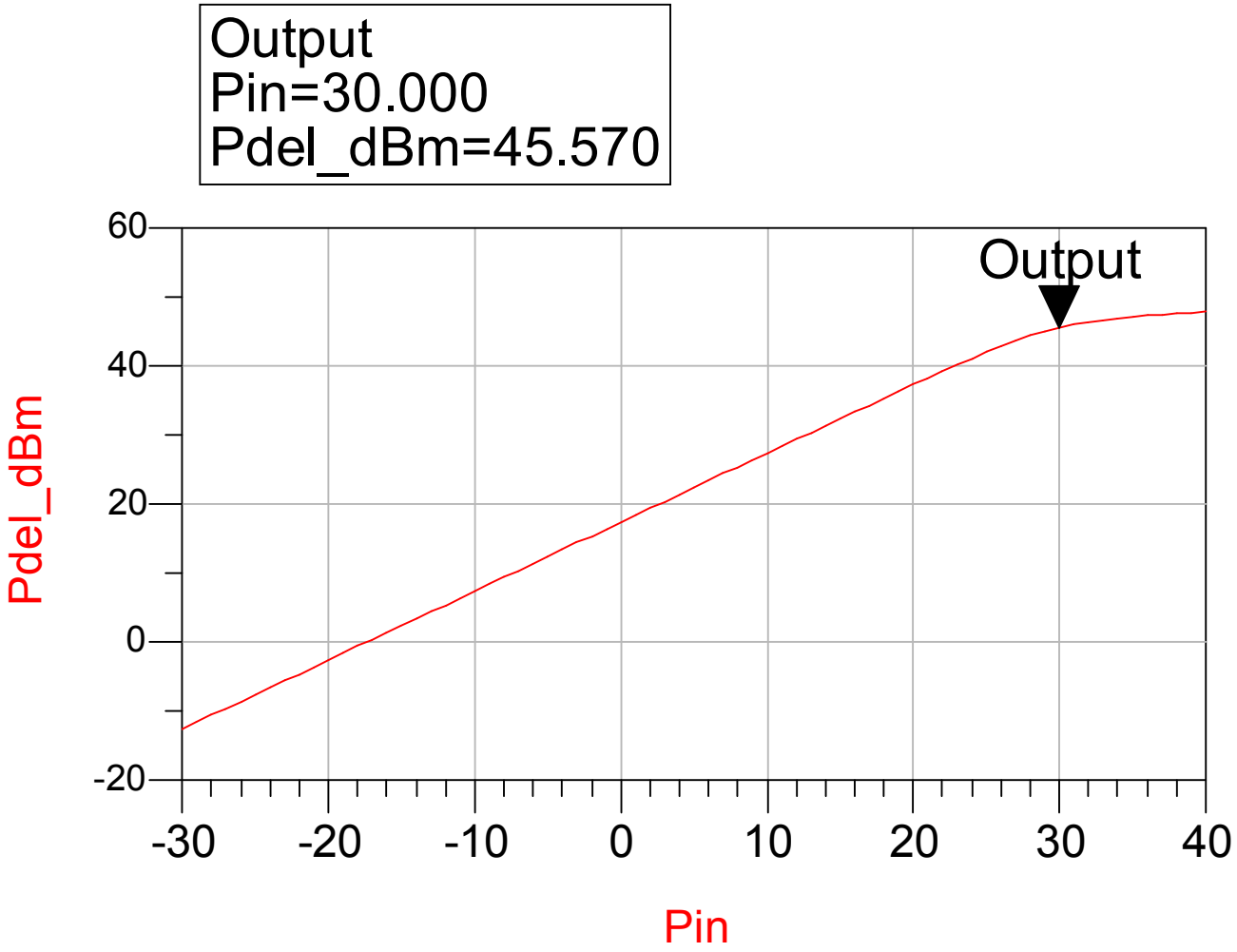
Input Match



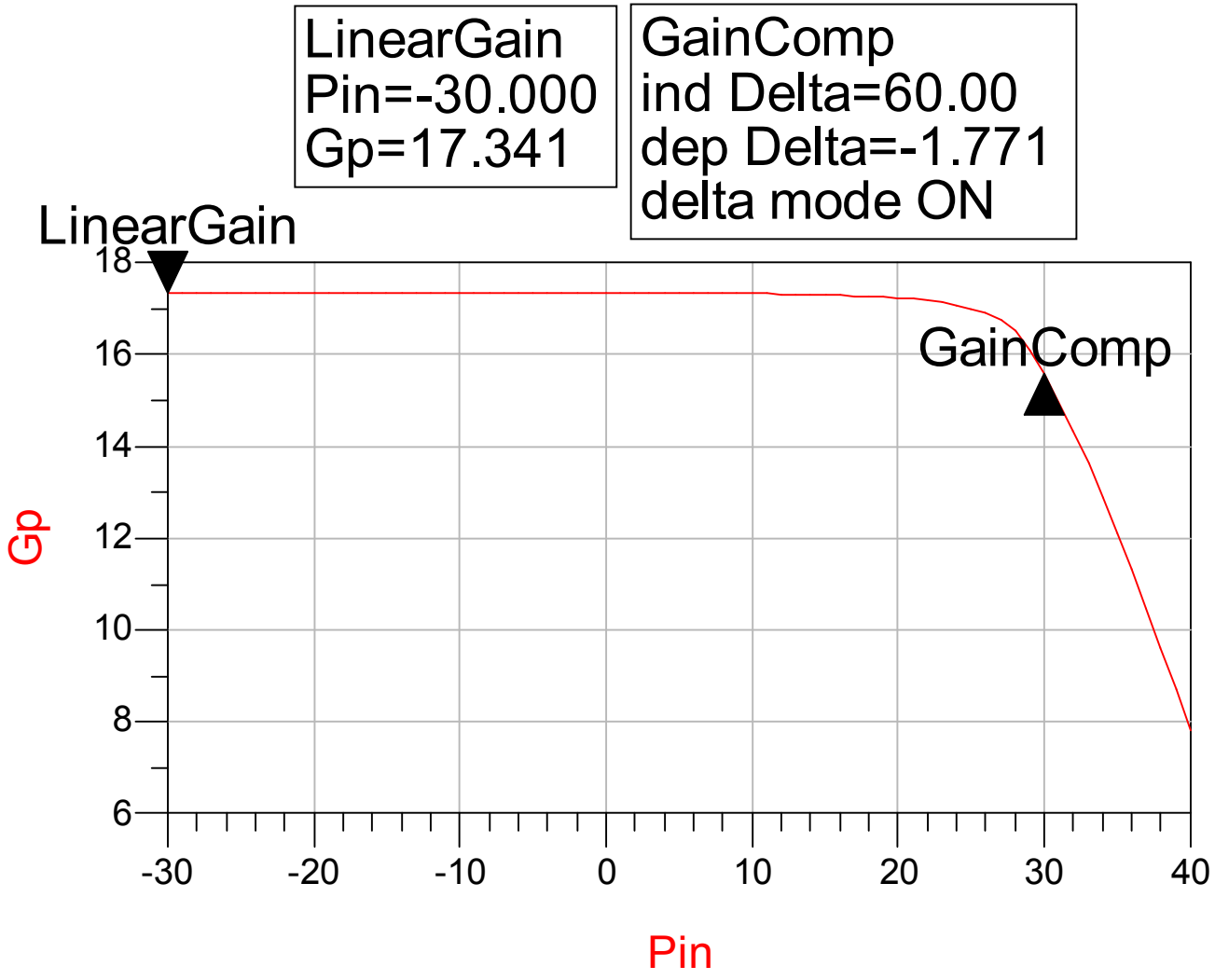
Complete Design Power Sweep



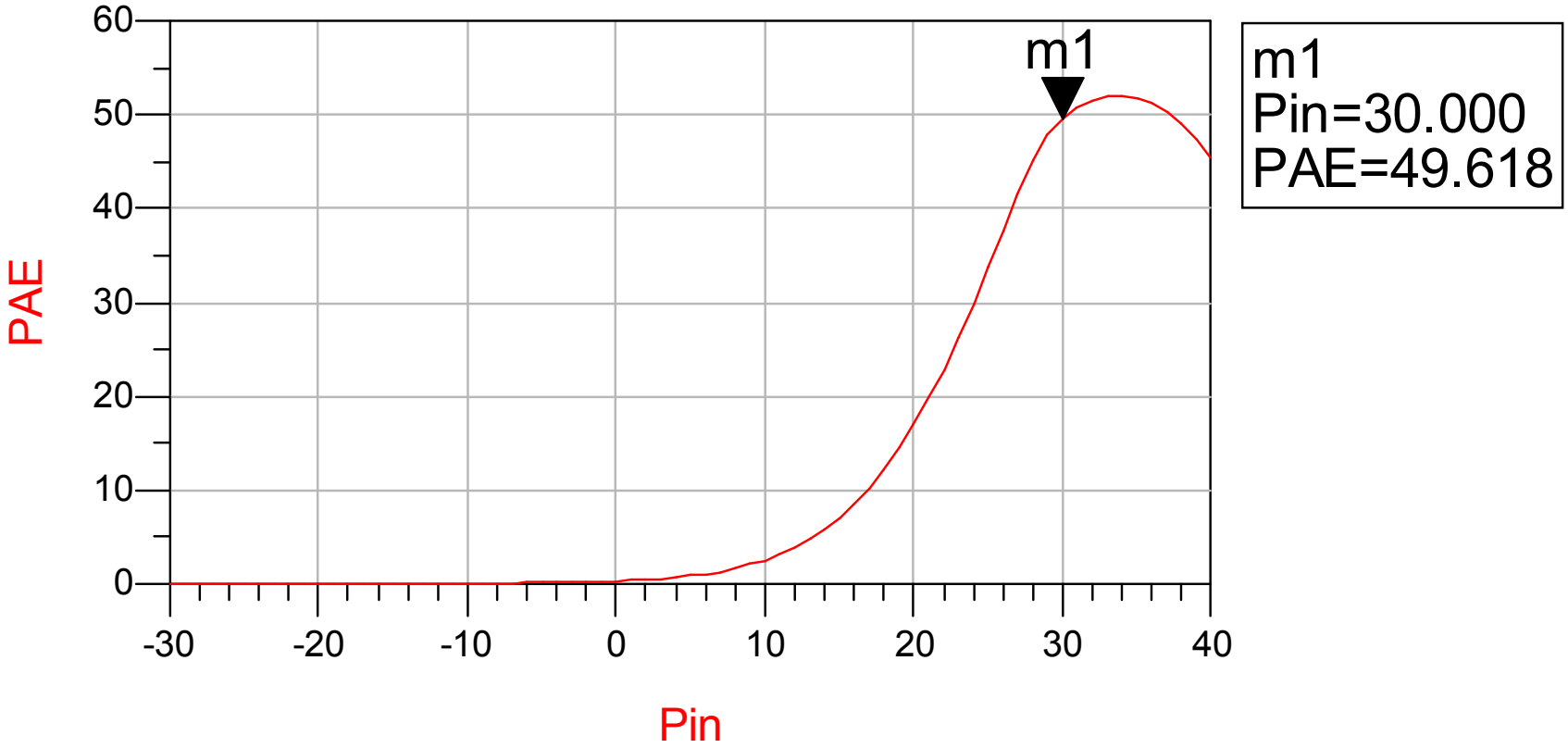
Power Compression Curve



Gain Compression Curve



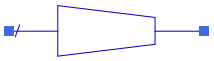
Power Added Efficiency



Getting ready to Optimize the PA

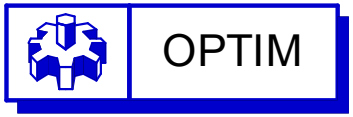
- **The next step is to optimize the design to meet the requirements.**
- **The Designer can take the opportunity to see if other requirements, such as layout will require any changes before proceeding to optimize.**
- **Example: we notice that the transistor pads are rather wide and the Tlines leading up to it are not the same width.**
- **Since the Tlines are much narrower, we could add a taper so we have a nice transition.**
- **We included a MTAPER at the input and output side**

MTAPER
Taper2
Subst="MSub1"
W1=199.971654 mi
W2=63.670079 mil
L=100.0 mil



dBm(Vload[1])
41.549

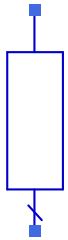
Optimization Setup



Optimization Results

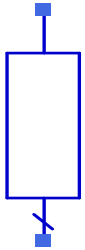
InitialEF	FinalEF
67.187	0.000

optIter	Goal1	Goal2
10	47.003	-40.017



MLIN
TL39
Subst="MSub1"
W=63.670079 mil
L=2194.444882 mil opt{ 250 mil to 3500 mil }

Before



MLIN
TL39
Subst="MSub1"
W=63.670079 mil
L=551.591 mil opt{ 250 mil to 3500 mil }

After

Optimization Values

TL39.L*1e5/2.54
551.591

TL15.L*1e5/2.54
247.144

TL7.L*1e5/2.54
320.449

TL30.L*1e5/2.54
814.900

TL8.L*1e5/2.54
622.341

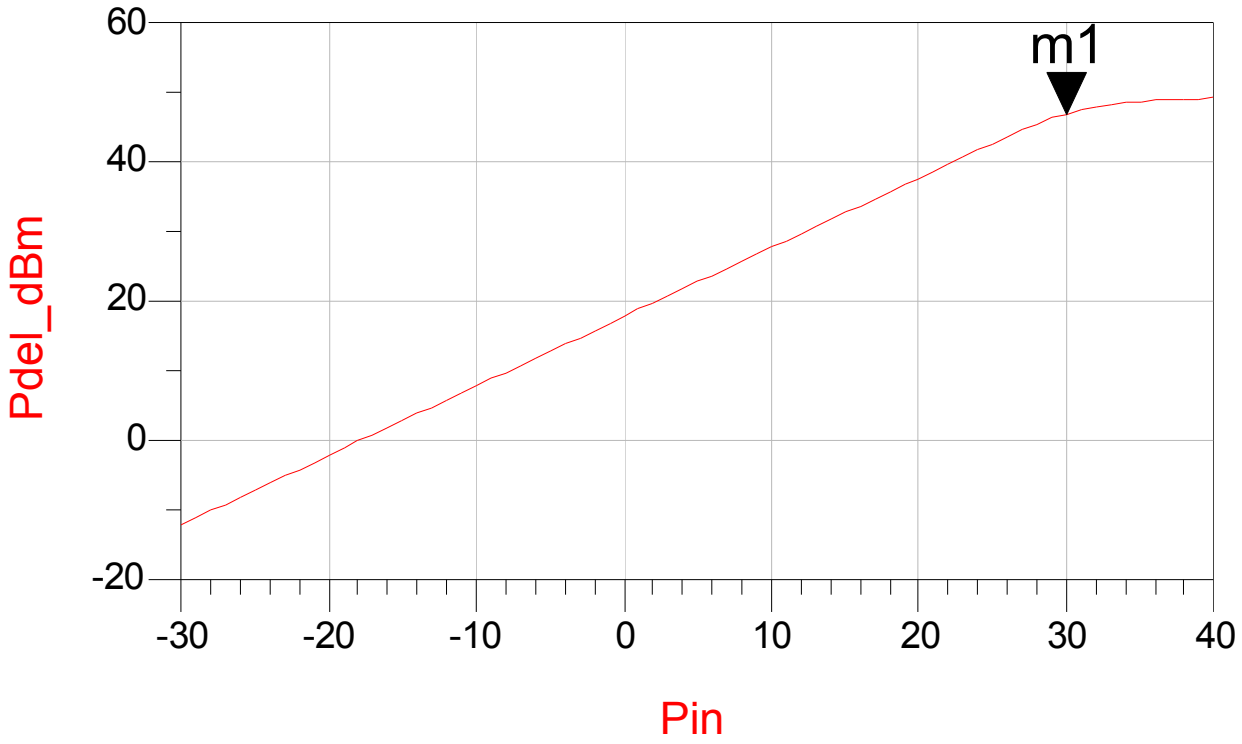
TL31.L*1e5/2.54
202.643

TL9.L*1e5/2.54
248.635

TL32.L*1e5/2.54
184.709

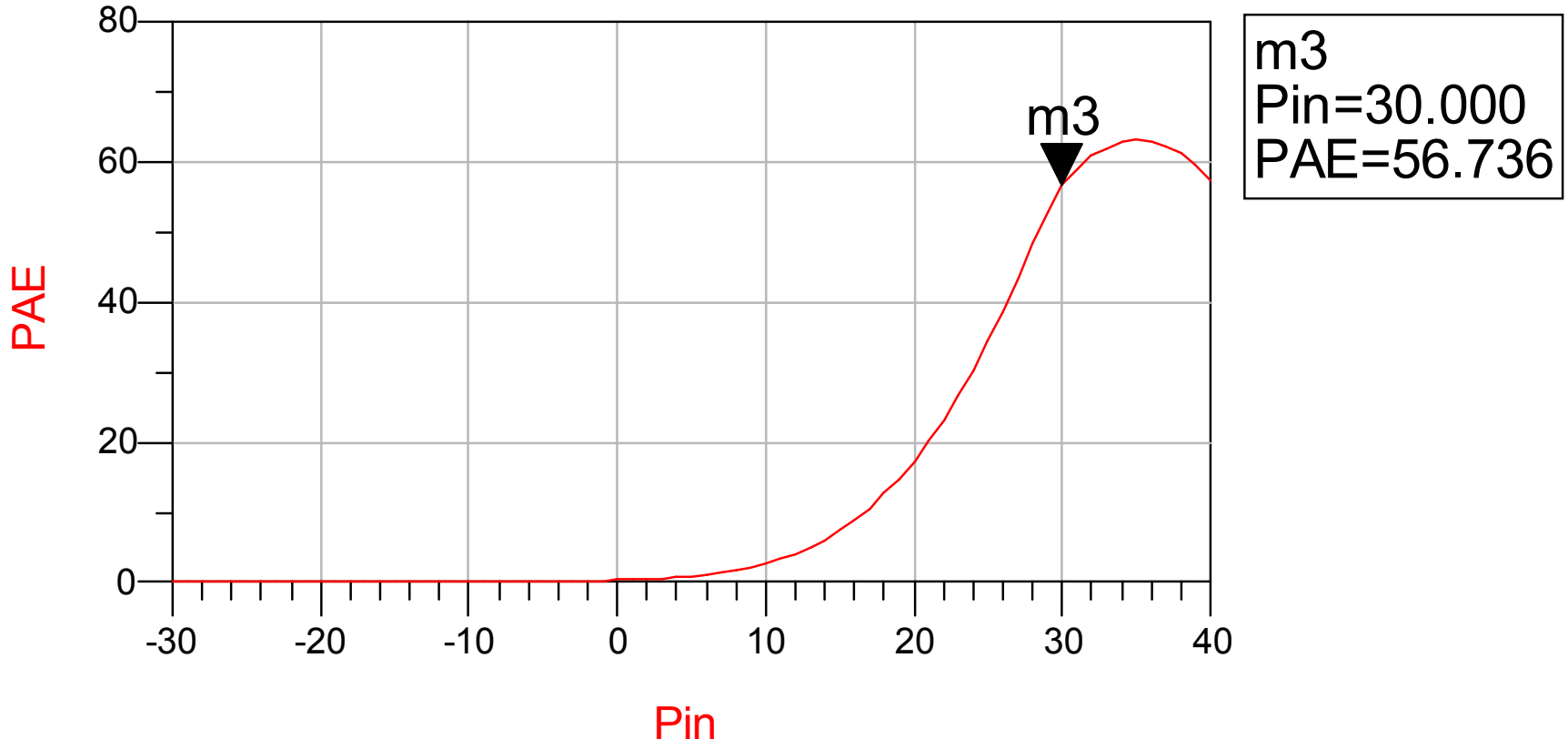
TL10.L*1e5/2.54
244.711

PA Results

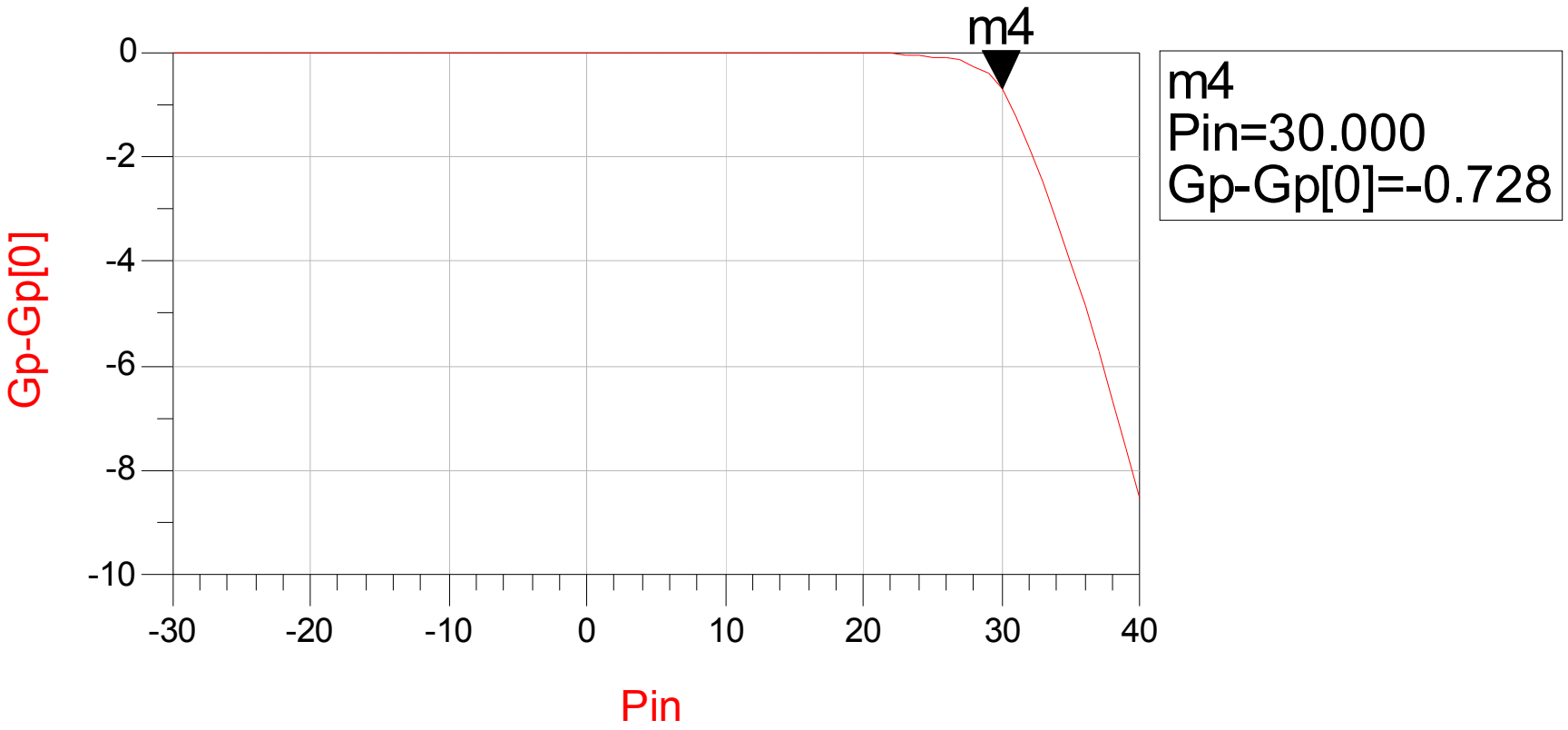


m1
Pin=30.000
Pdel_dBm=47.003

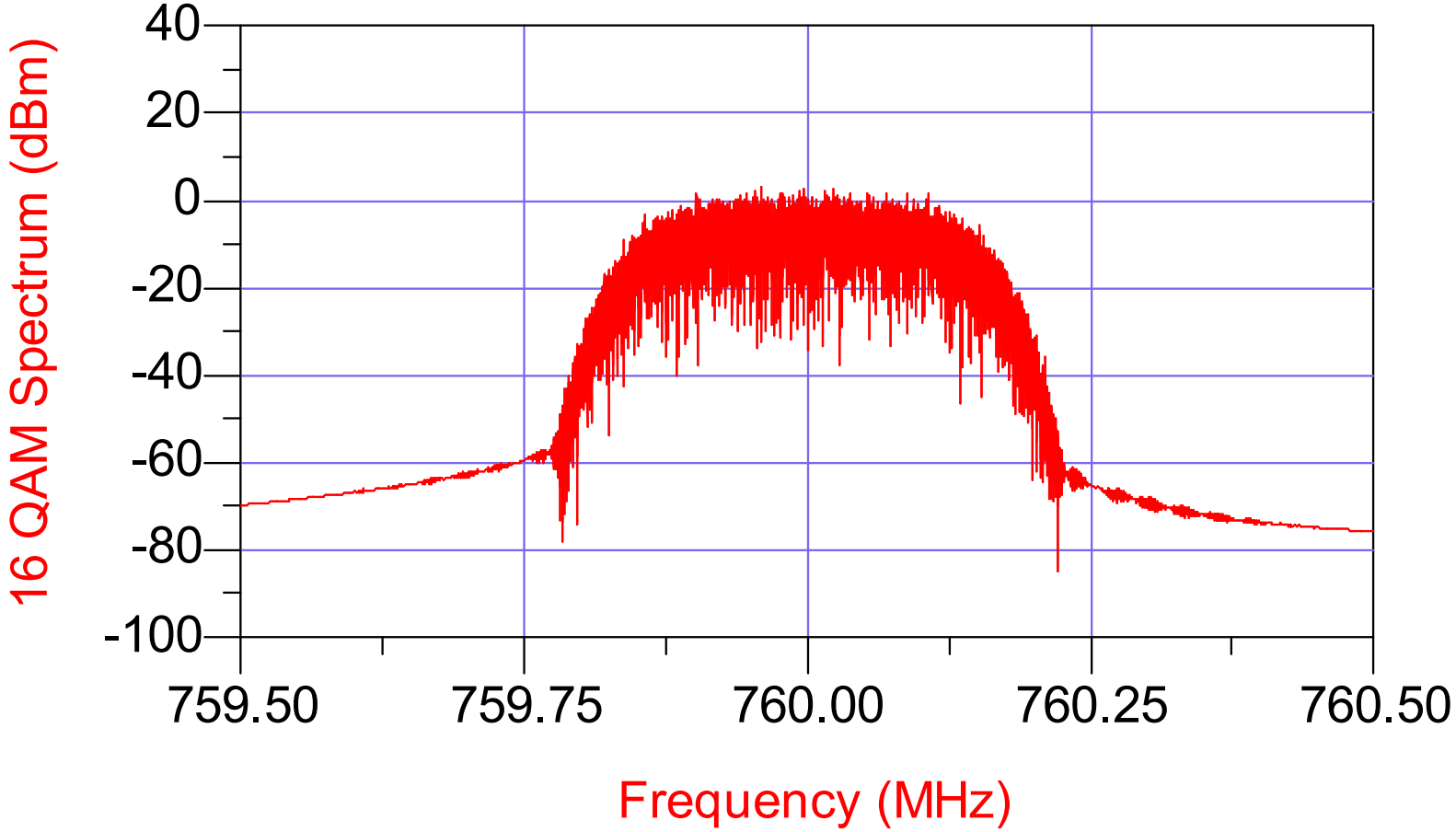
Power Added Efficiency



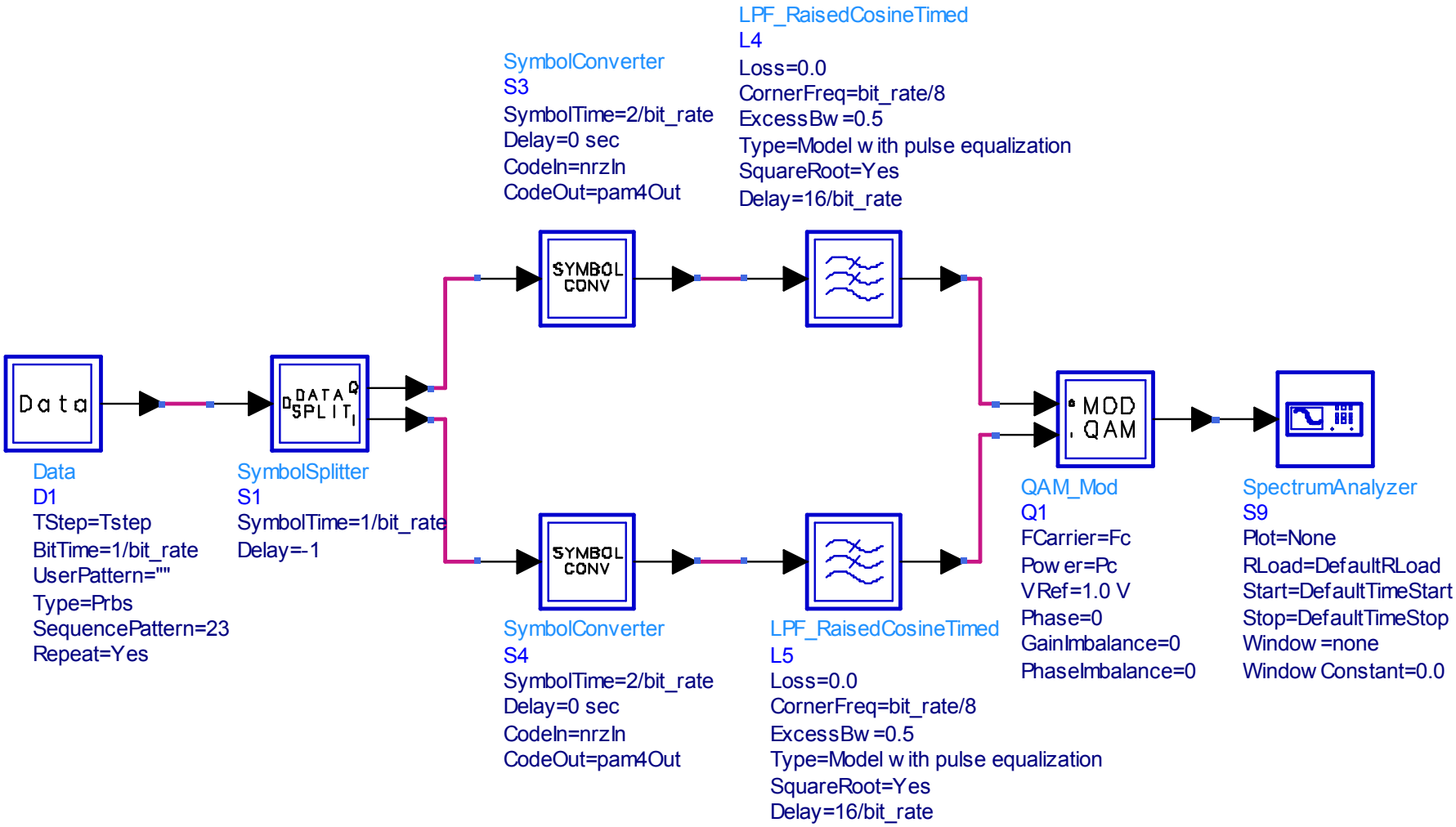
Gain Compression Curve



Complex Modulated Signal



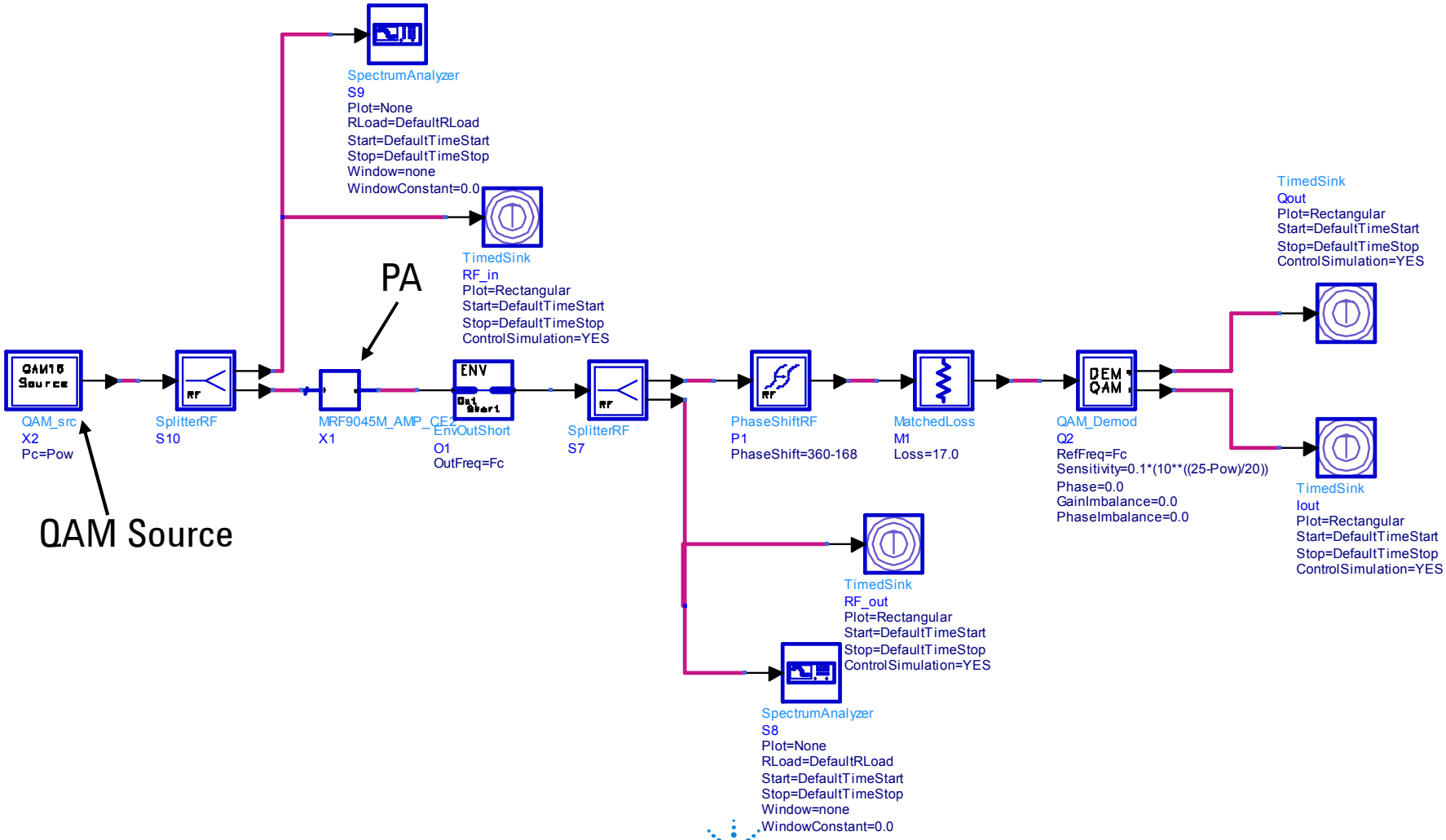
16 QAM Modulated Source



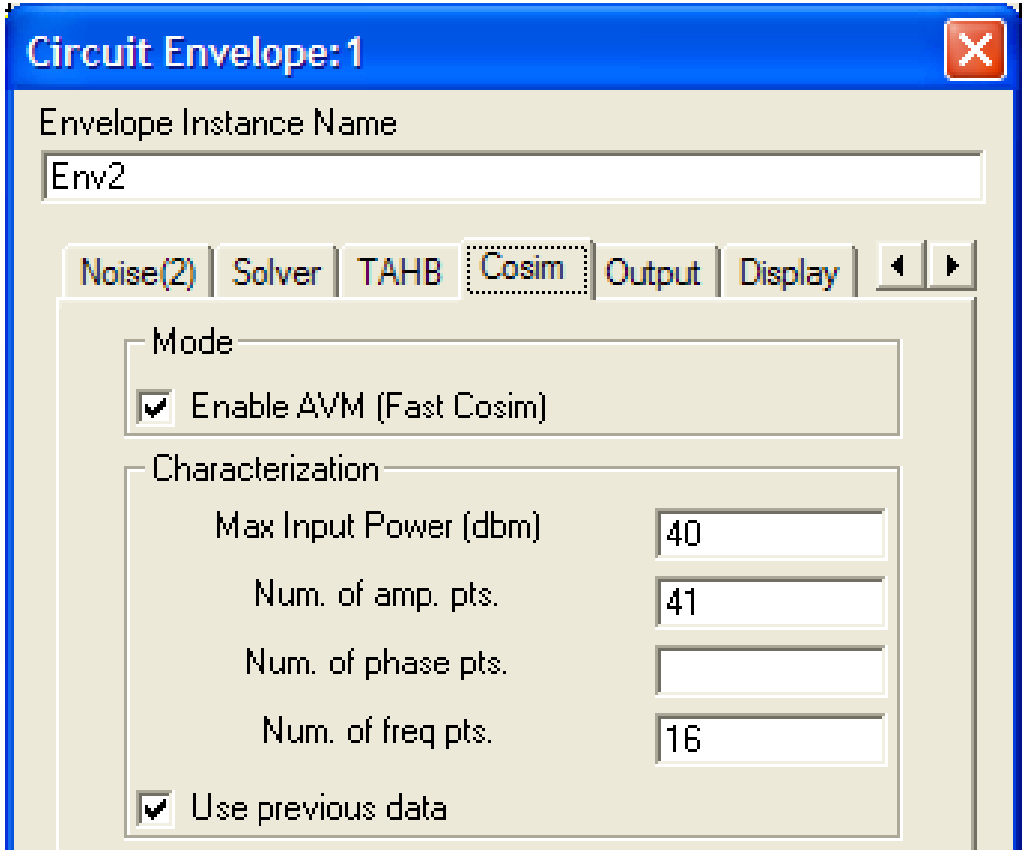
DSP and Analog Circuits Setup

- Create a subcircuit with your analog design.
- You need to add either Circuit Envelope or Transient controller to the analog circuit.
- We use Circuit Envelope specifically with our PA since we have a Modulated Carrier.
- Circuit Envelope will also allow the use of Fast Cosim (Automatic Verification Modeling – AVM). This will dramatically increase the simulation speed.
- In the DSP schematic we will create the Modulated Carrier, feed it to the PA and collect the signal samples and spectrum.
- The DSP schematic contains a Envelope Output Selector component used for interfacing between circuit subnetwork output and the signal processing components.

Ptolemy Cosim Schematic



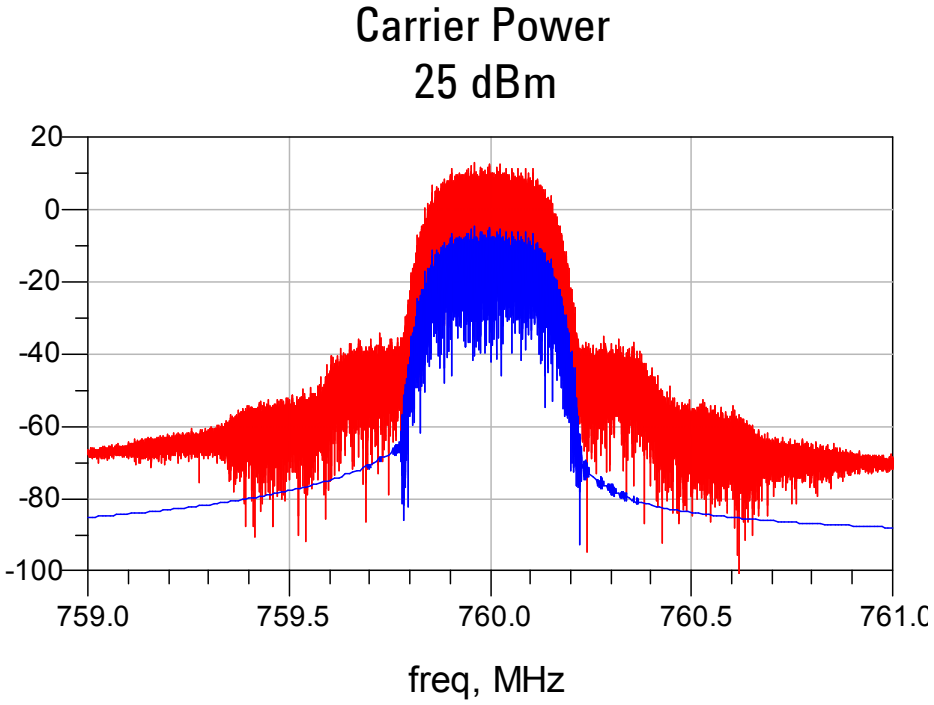
Fast Cosim Improvements

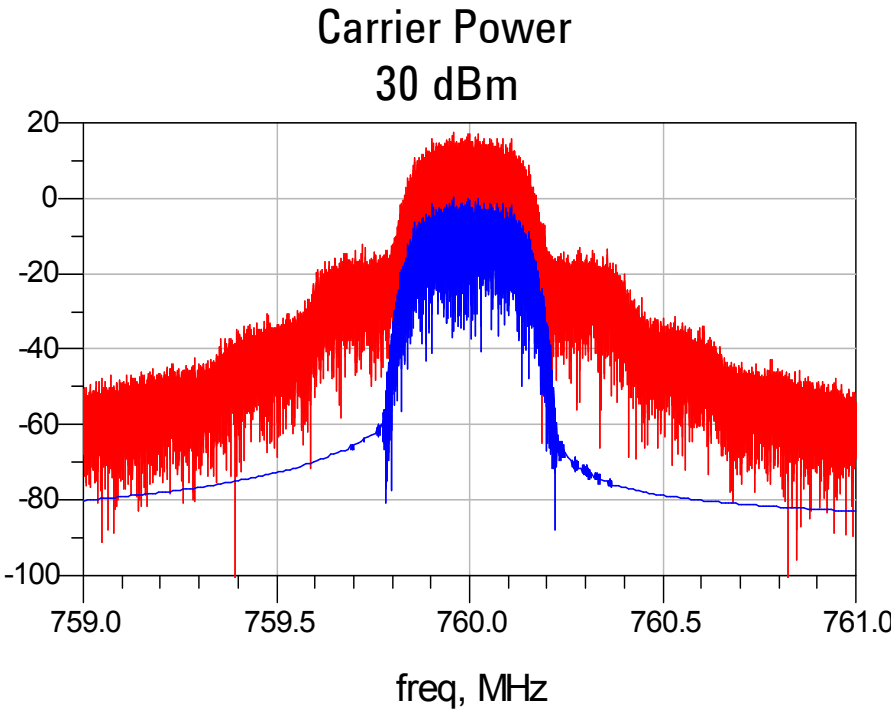


Simulation Time Benchmark:
Total bits: 1024 bits
AVM disabled : 410 sec
AVM enabled: 13 sec
AVM data reuse: 5.5 sec

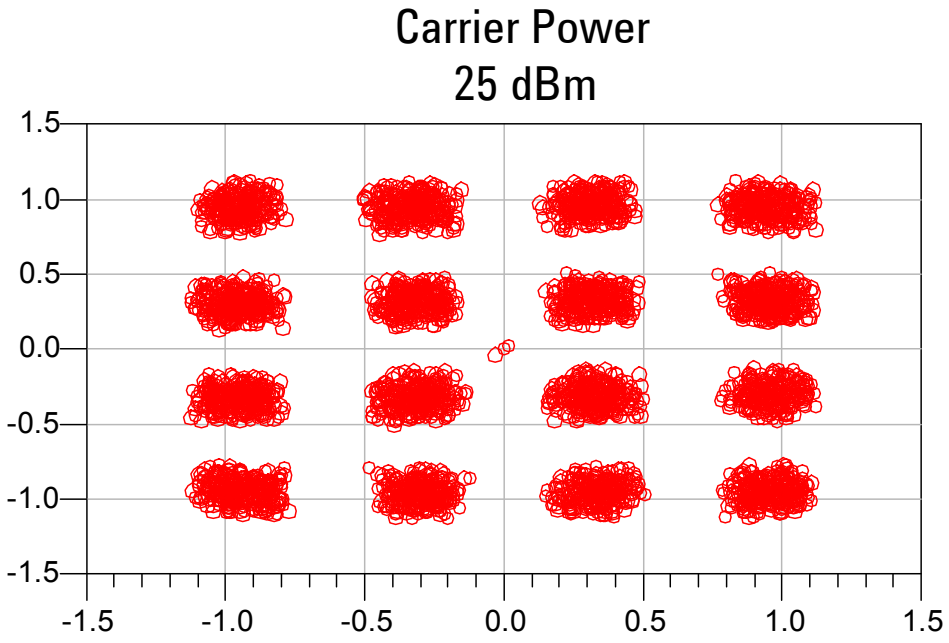
AVM data reuse (16 Kbits): 17.5 sec

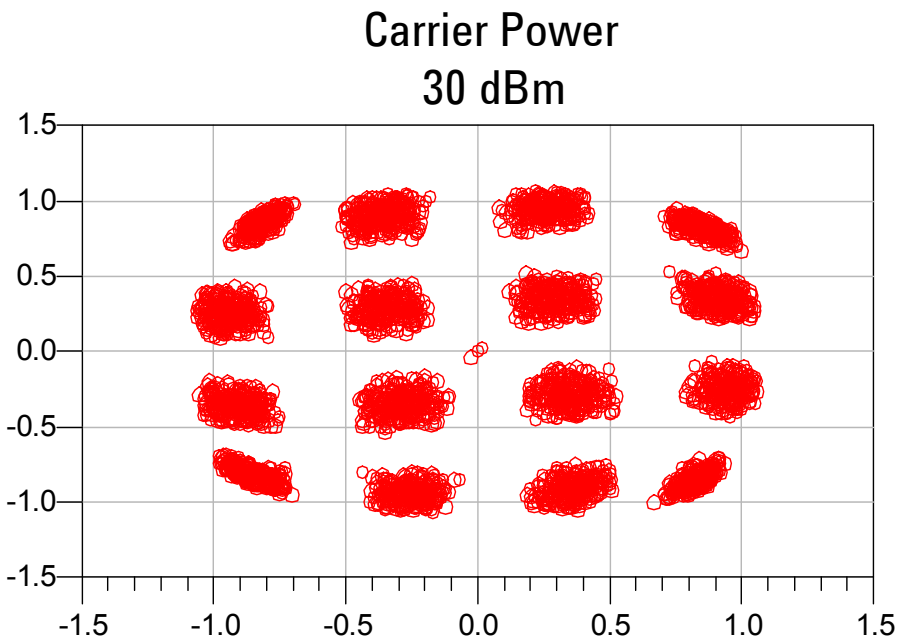
Cosimulation Results - Spectrum





Cosimulation Results - Constellation





Cosimulation Results

Carrier Power
30 dBm

peakP_in	peak_avg_in	avgPin
32.163	4.951	27.212

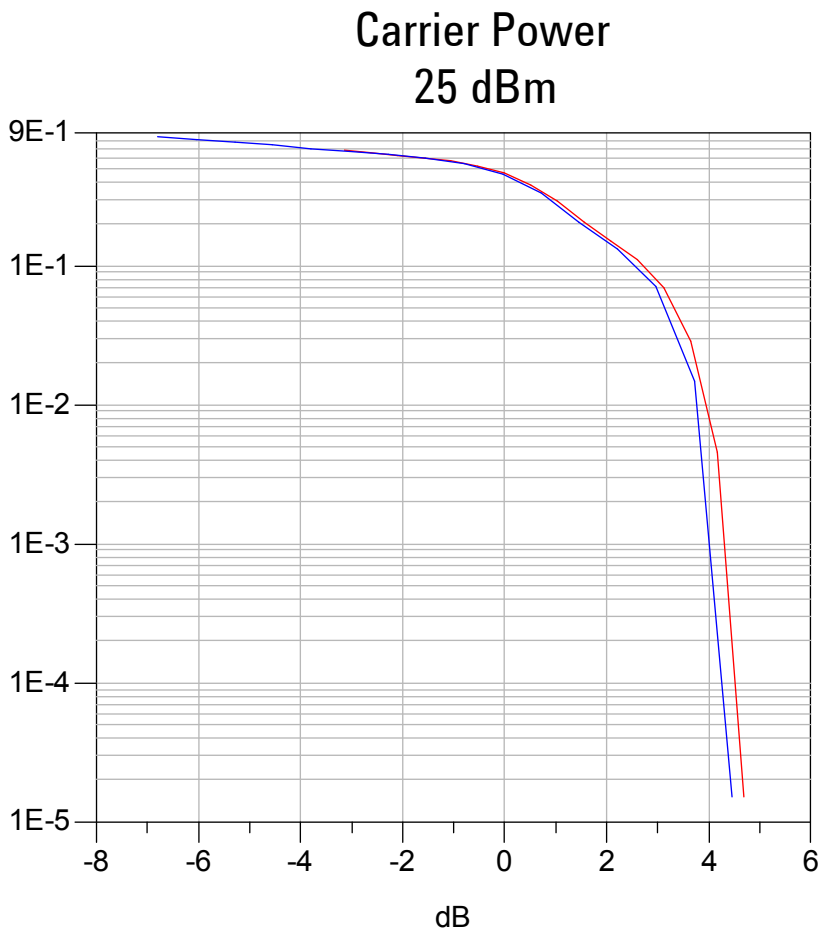
peakP_out	peak_avg_out	avgPout
47.969	3.516	44.453

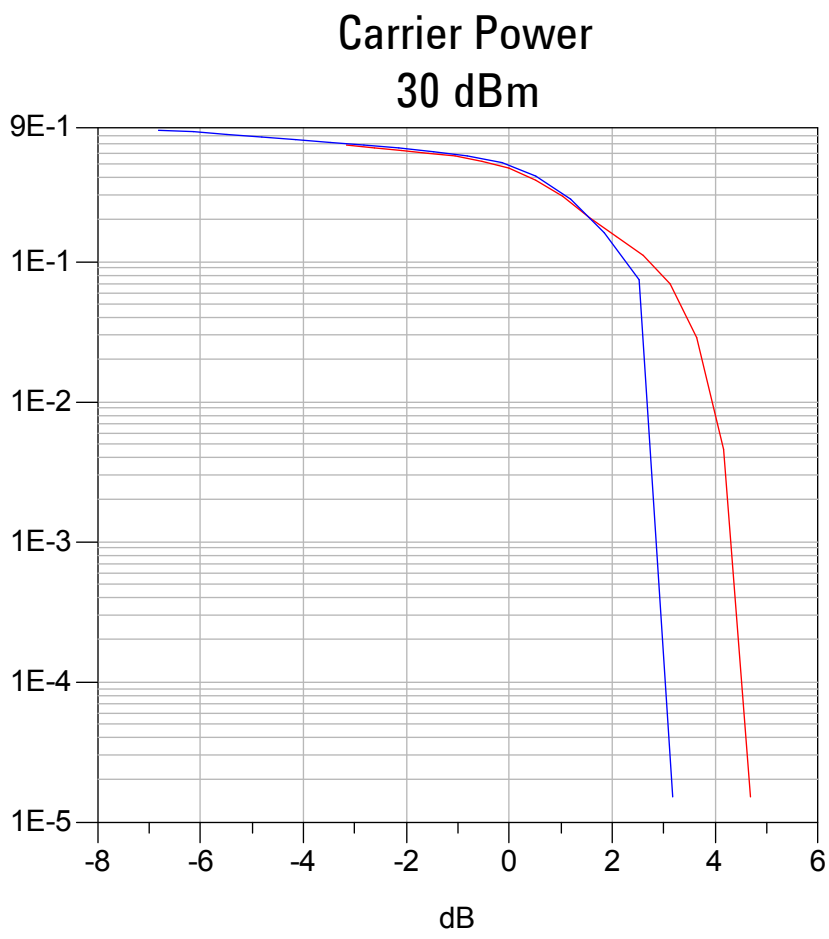
Carrier Power
25 dBm

peakP_in	peak_avg_in	avgPin
30.000	7.788	22.212

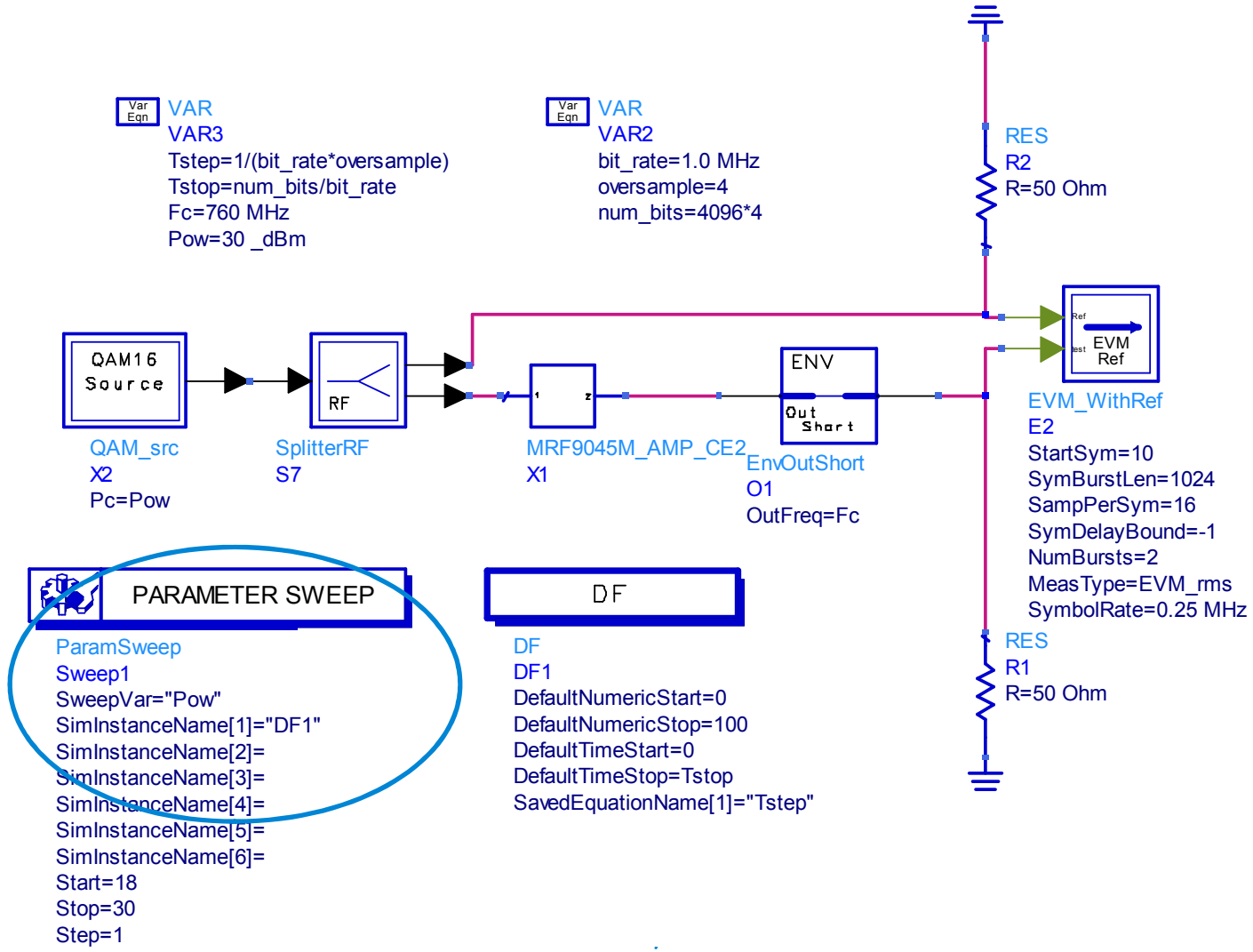
peakP_out	peak_avg_out	avgPout
44.715	4.832	39.883

Cosimulation Results – CCDF

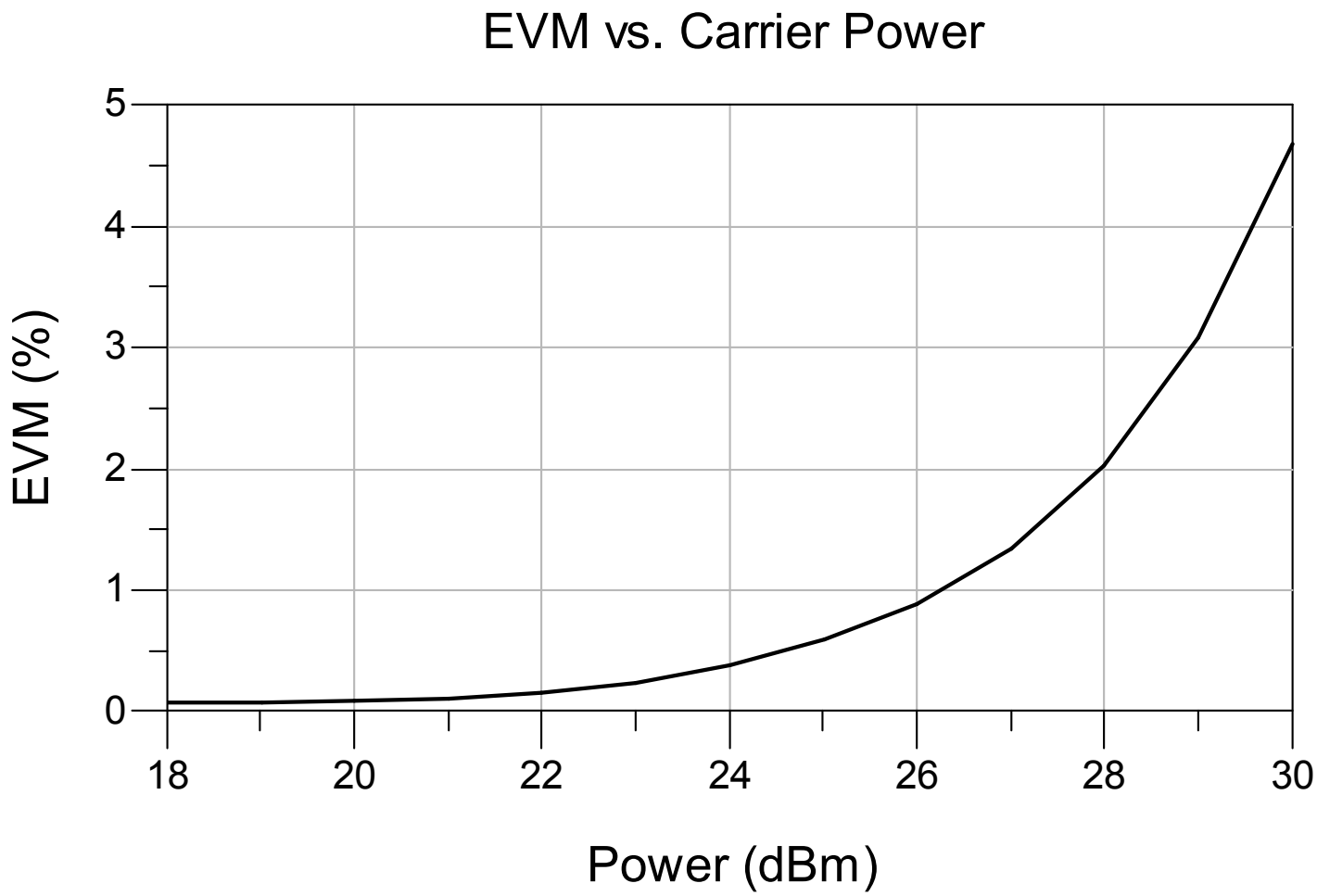




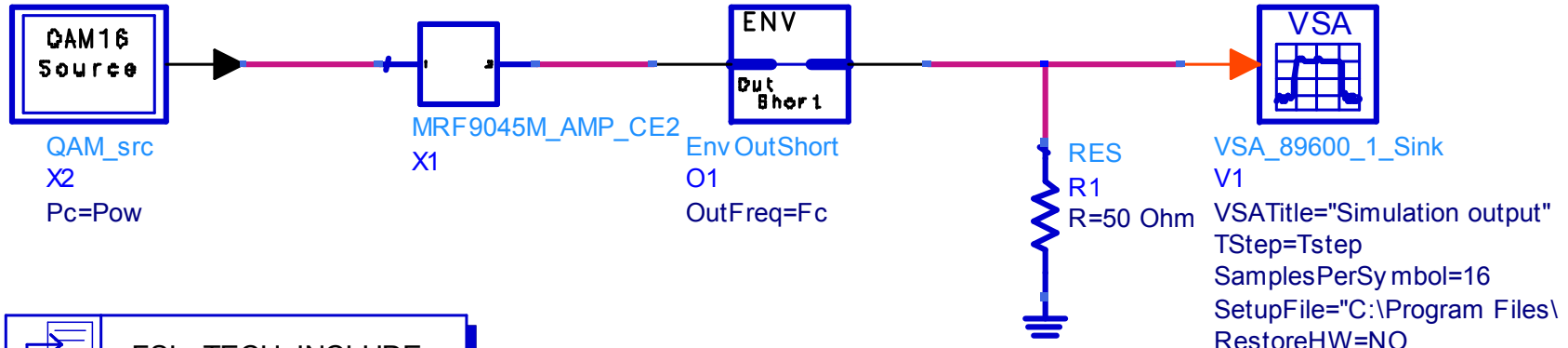
EVM vs. Power Measurement



EVM vs. Power Results



ADS to VSA link



QAM_src
X2
Pc=Pow

MRF9045M_AMP_CE2
X1

Env OutShort
O1
OutFreq=Fc

RES
R1
R=50 Ohm

VSA_89600_1_Sink
V1
VSATitle="Simulation output"
TStep=Tstep
SamplesPerSymbol=16
SetupFile="C:\Program Files\
RestoreHW=NO
SetFreqProp=YES

FSL_TECH_INCLUDE

FSL_TECH_INCLUDE
FTI

Var Eqn

VAR
VAR3
Tstep=1/(bit_rate*oversample)
Tstop=num_bits/bit_rate
Fc=760 MHz
Pow=30 _dBm

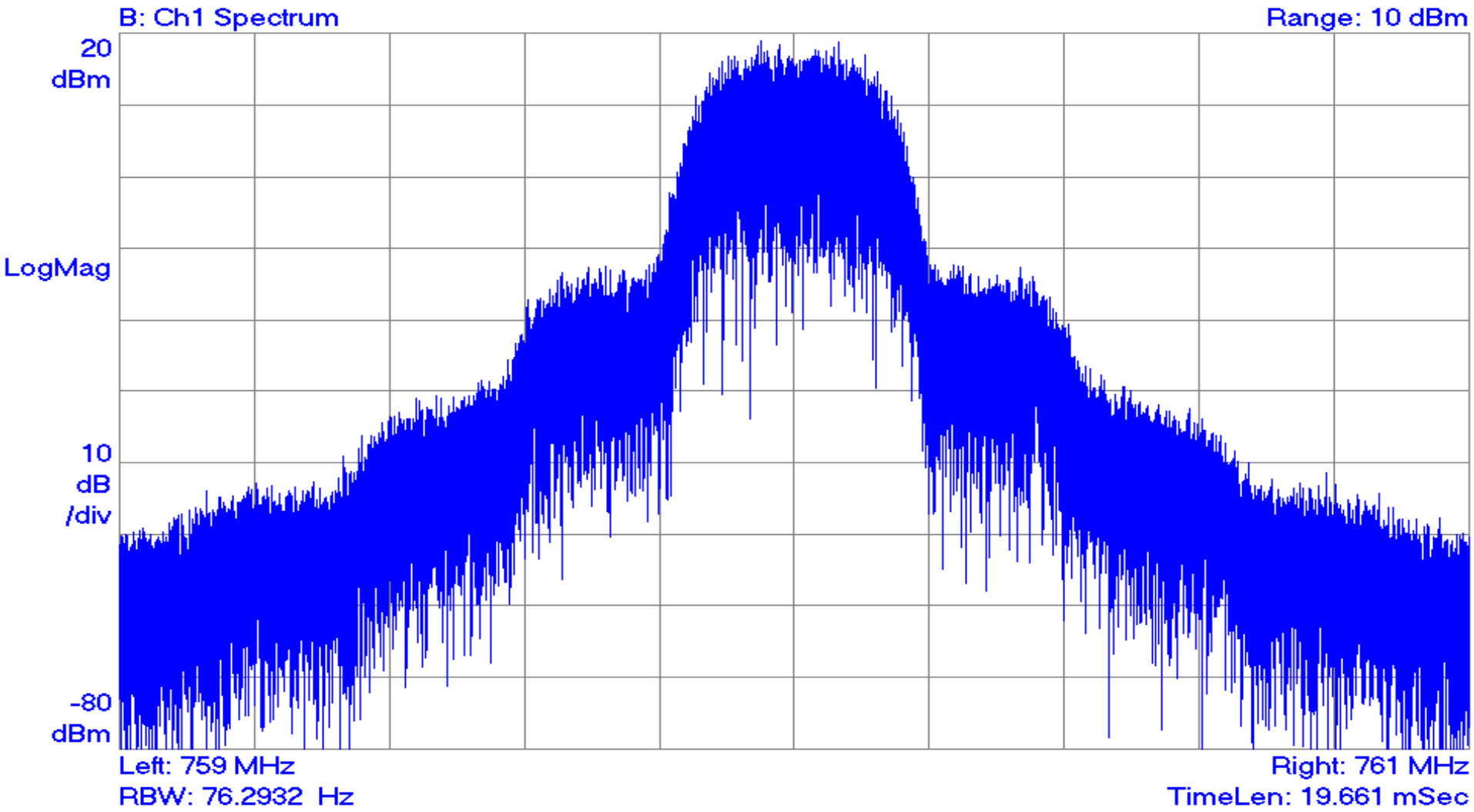
DF

DF
DF1
DefaultNumericStart=0
DefaultNumericStop=100
DefaultTimeStart=0
DefaultTimeStop=Tstop
SavedEquationName[1]="Tstep"

Var Eqn

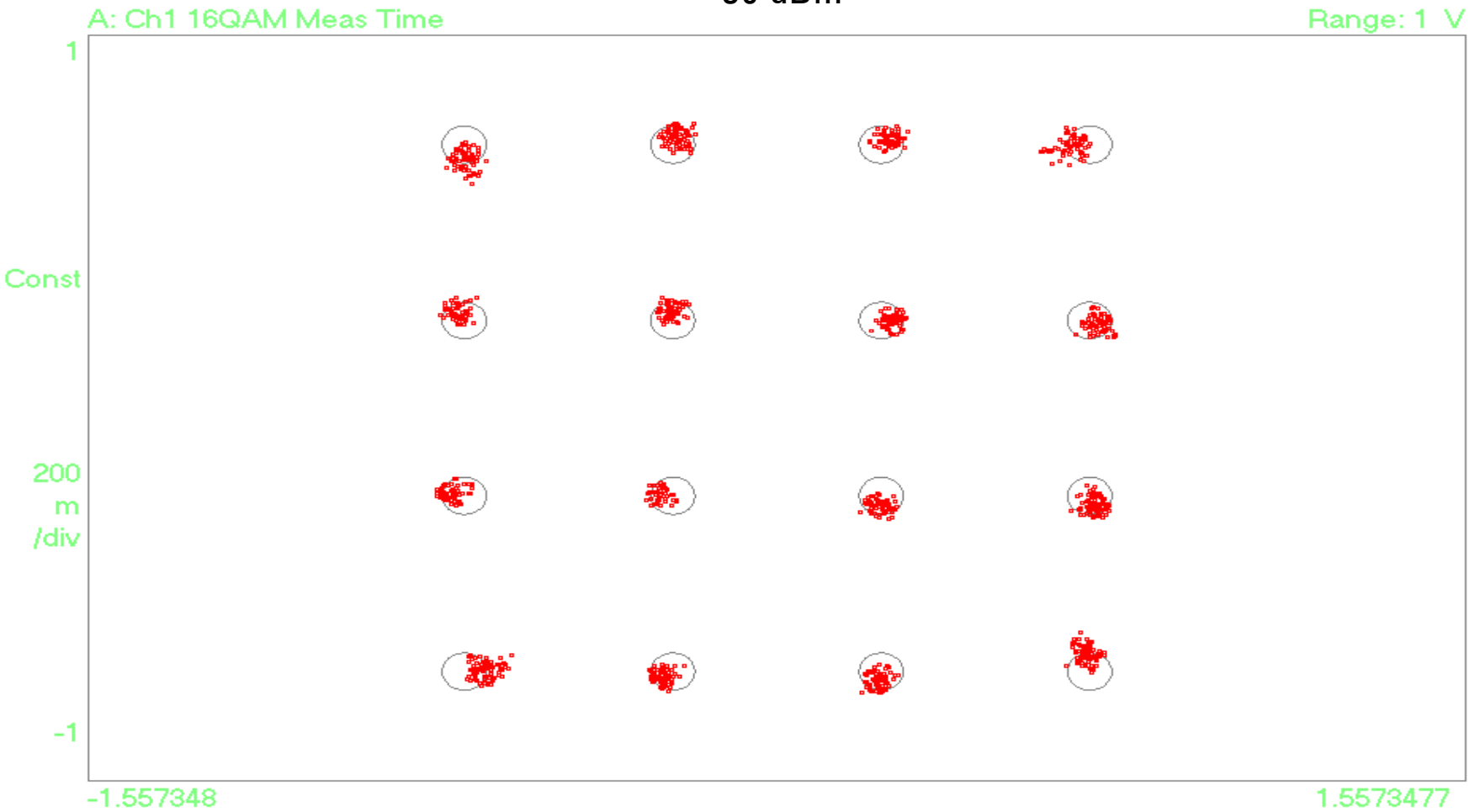
VAR
VAR2
bit_rate=1.0 MHz
oversample=4
num_bits=1024*16

VSA Spectrum from ADS Cosim



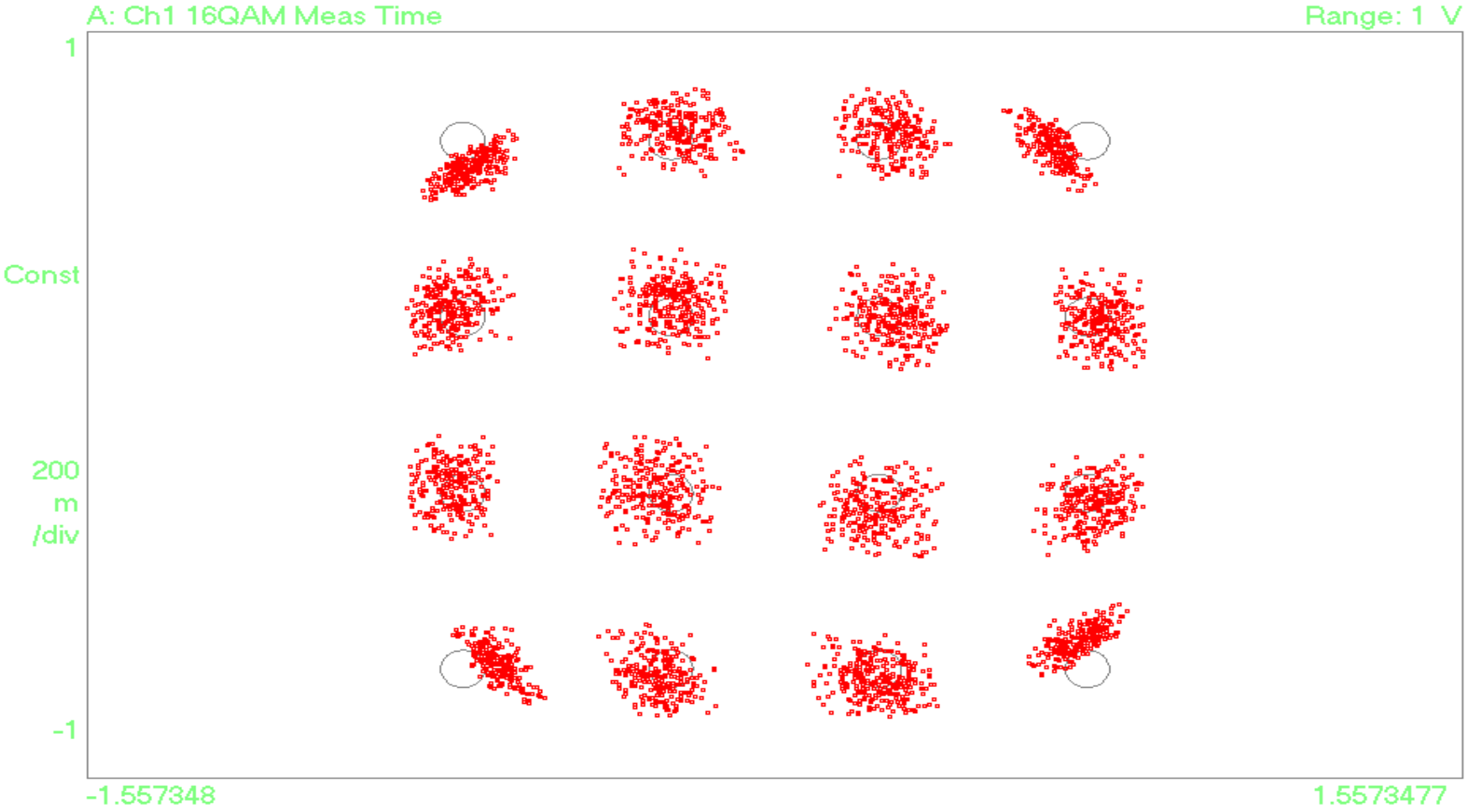
VSA Constellation from ADS Cosim

Carrier Power
30 dBm



VSA Constellation from ADS Cosim

Carrier Power
30 dBm



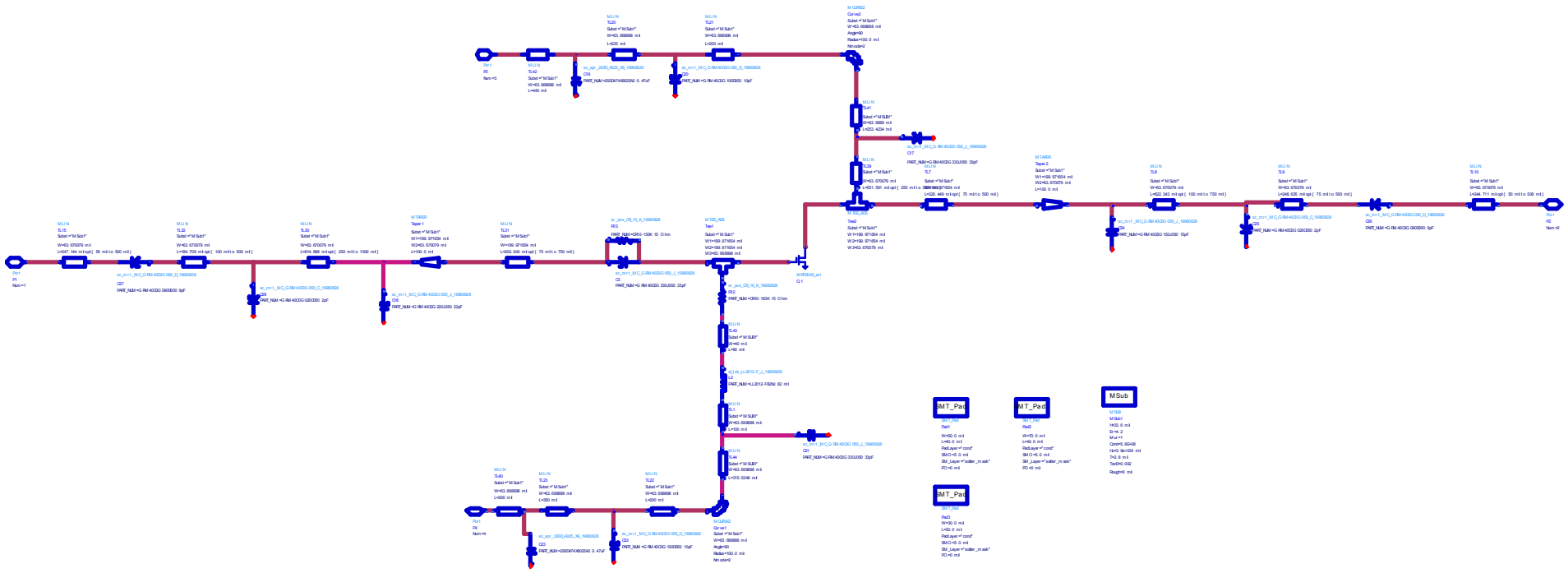
VSA EVM from ADS Cosim

Carrier Power
30 dBm

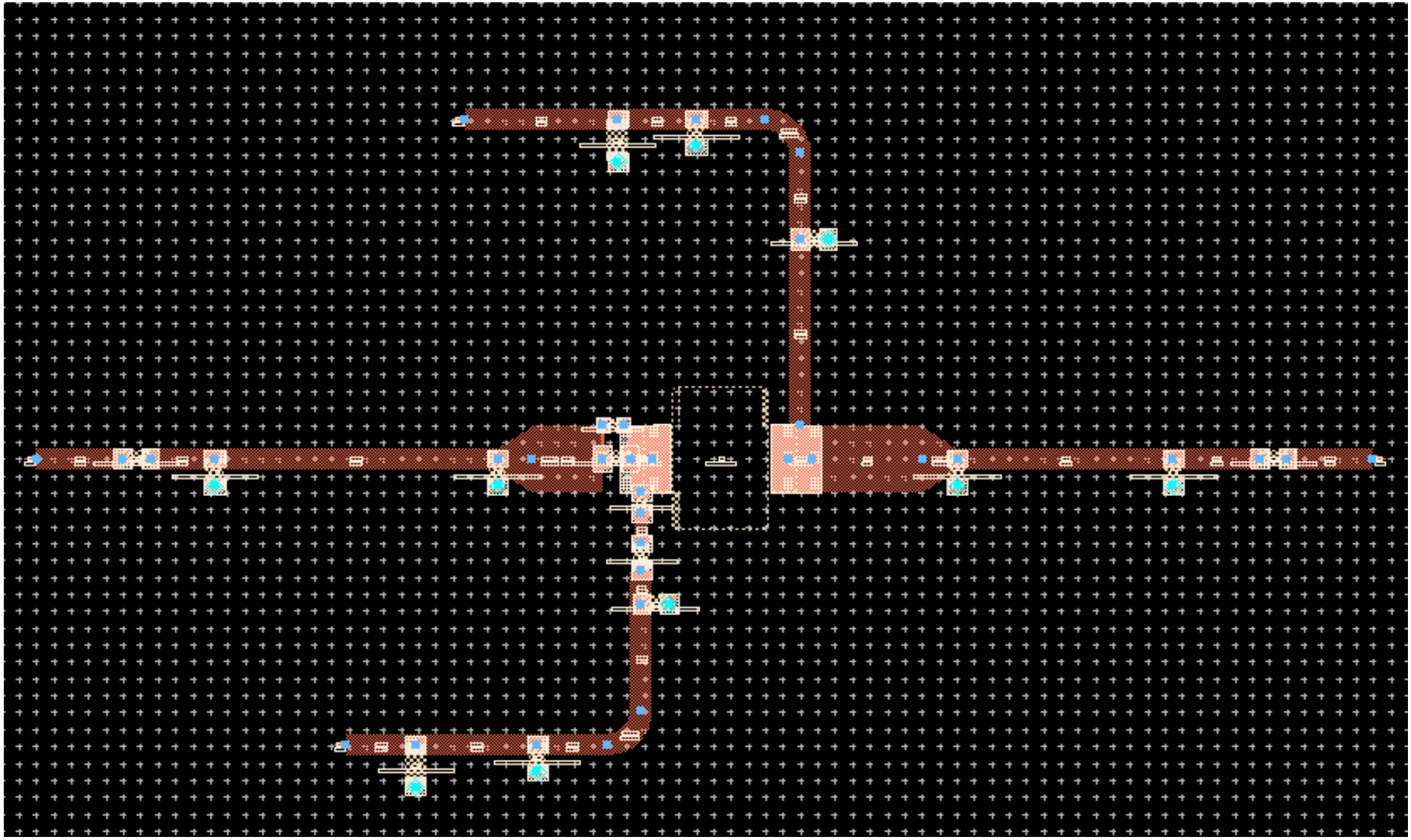
D: Ch1 16QAM Syms/Errs Time:27

EVM	= 4.1676	%rms	12.719	% pk at	sym	1468
Mag Err	= 3.1291	%rms	-11.221	% pk at	sym	2507
Phase Err	= 2.6647	deg	-11.881	deg pk at	sym	3471
Freq Err	= 5.1206	mHz				
IQ Offset	= -65.85	dB	SNR(MER) = 25.051		dB	
Quad Err	= 94.065	mdeg	Gain Imb = 0.01		dB	

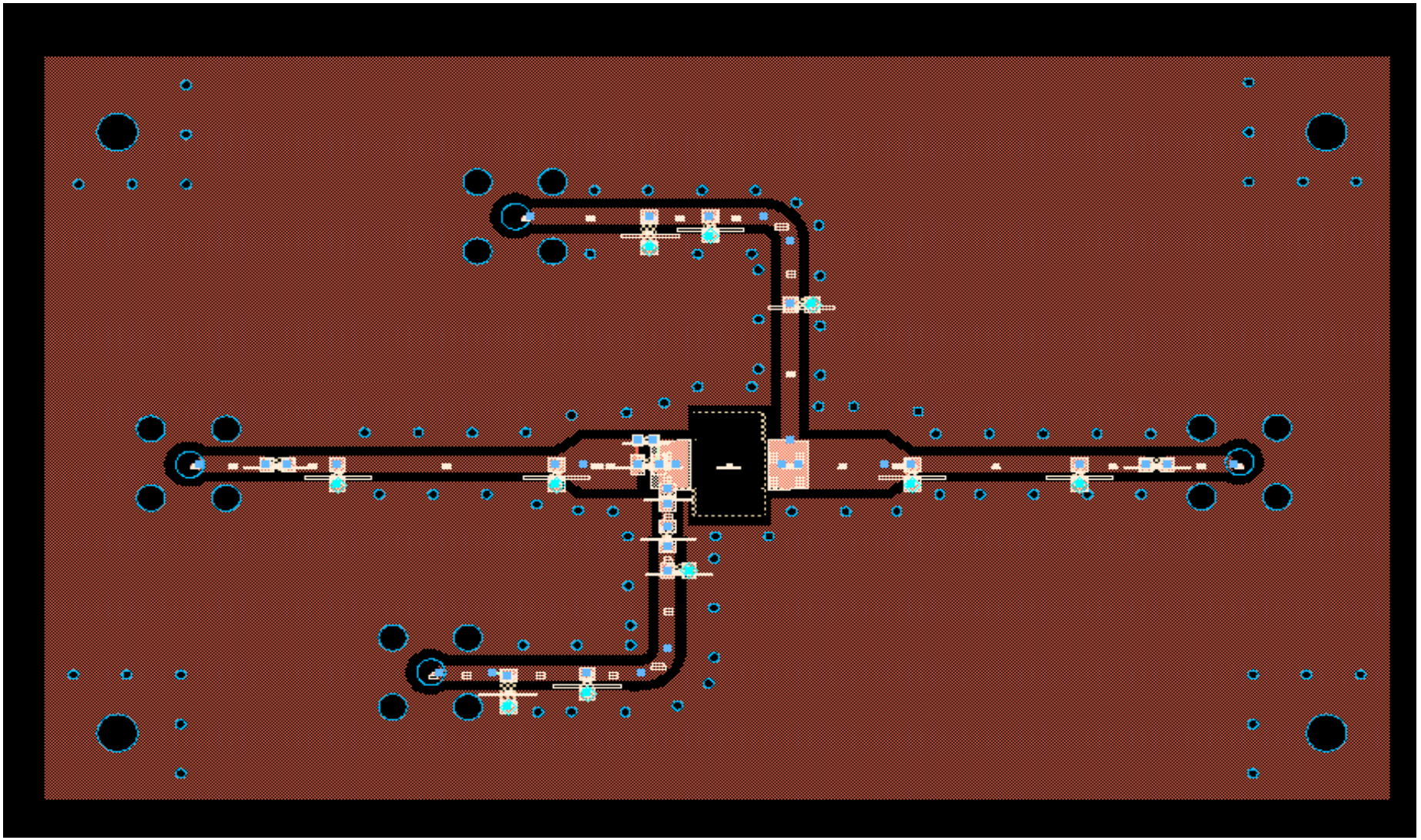
PA Layout



PA Layout – Generated from Schematic



PA Layout – Ground Fill



Other Possibilities

- Run an EM Cosimulation – include layout effects in the simulation. Optimize design if necessary.
- Run Loadpull for IP3 or ACPR. The optimum load would then be a compromise between all the requirements.
- Use Connection Manager and real PA to validate design and compare vs. simulated results.
- Create a behavioral data model that can be used to protect you IP yet give access to your design results.

If there is any topic about PA Design and ADS you wish to discuss email me: wilfredo_rivas-torres@agilent.com

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