

Oak Trail Platform – Alpine Bay

Customer Reference Board Schematics

December 2010

Revision 1.5

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Revision History

Document Number	Revision Number	Description	Revision Date
448204	0.7	Initial release	May 2010
448204	1.0	<ul style="list-style-type: none">• Updated Lincroft processor, Whitney Point chipset and PMIC Connector symbol• Added relevant notes for validation specific circuit sheets• Added note on external VR back up option for VCC180 rail for Lincroft processor• Added note on HDMI audio reserved SDI port• Removed duplicate circuitry for GTREF and CREF for Whitney Point chipset• Corrected SDIO1 net names• Updated RSVD pin connections for Whitney Point chipset and Lincroft processor	October 2010
448204	1.1	<p>Page 3</p> <ul style="list-style-type: none">• Corrected no_stuff notes for DDR2 terminations <p>Page 4</p> <ul style="list-style-type: none">• Changed R2 to R5G5 (to minimize layout work)• Changed R1 package to 0402 (to minimize layout work)• Added notes on RSVD pin terminations <p>Page 16</p> <ul style="list-style-type: none">• Added notes on RSVD pin terminations <p>Page 48</p> <ul style="list-style-type: none">• Changed 10 kOhms R3H1 package to 0603 to retain the same package as before when 100 kOhms was used. <p>Page 36</p> <ul style="list-style-type: none">• Added notes on pull up voltage change for SMC_EXTSMI# signal <p>Page 37</p> <ul style="list-style-type: none">• Added notes on pull up voltage change for SMC_WAKE_RUNTIME_SCI# signal <p>Page 6,7,45</p> <ul style="list-style-type: none">• Added notes on Lincroft VCCPDDR sighting <p>Overall Schematics</p> <ul style="list-style-type: none">• Updated Lincroft and Whitney Point symbol	November 2010



Document Number	Revision Number	Description	Revision Date
448204	1.5	Page 1 <ul style="list-style-type: none">• corrected USB port numbering in the block diagram	December 2010

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OAK TRAIL REFERENCE AND VALIDATION PLATFORM (RVP)

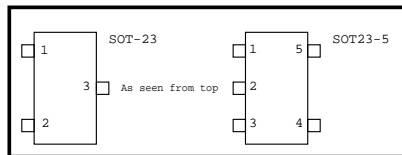
LED

LED REFDES	DESCRIPTION
CR2F4	NUM LOCK
CR2F5	CAPS LOCK
CR2F6	SCROLL LOCK
CR2F7	SYS PWR GOOD
CR2F8	S0
CR1F2	S3
CR1F3	S4
CR1F4	S5
CR6H1	POWER MODE1
CR6H2	POWER MODE0
CR6H3	POWER MODE2
CR9G2	PMIC PWR GOOD
CR9G3	RESET OUT
CR9G4	THERM TRIP
CR9G5	PROCHOT
CR9H1	IERR

SWITCHES

Switch	Default	Description
SW2D1	1 - 2	VIRTUAL BATTERY
SW1D1	1 - 2	LID SWITCH

PCB Footprints



Jumper Settings

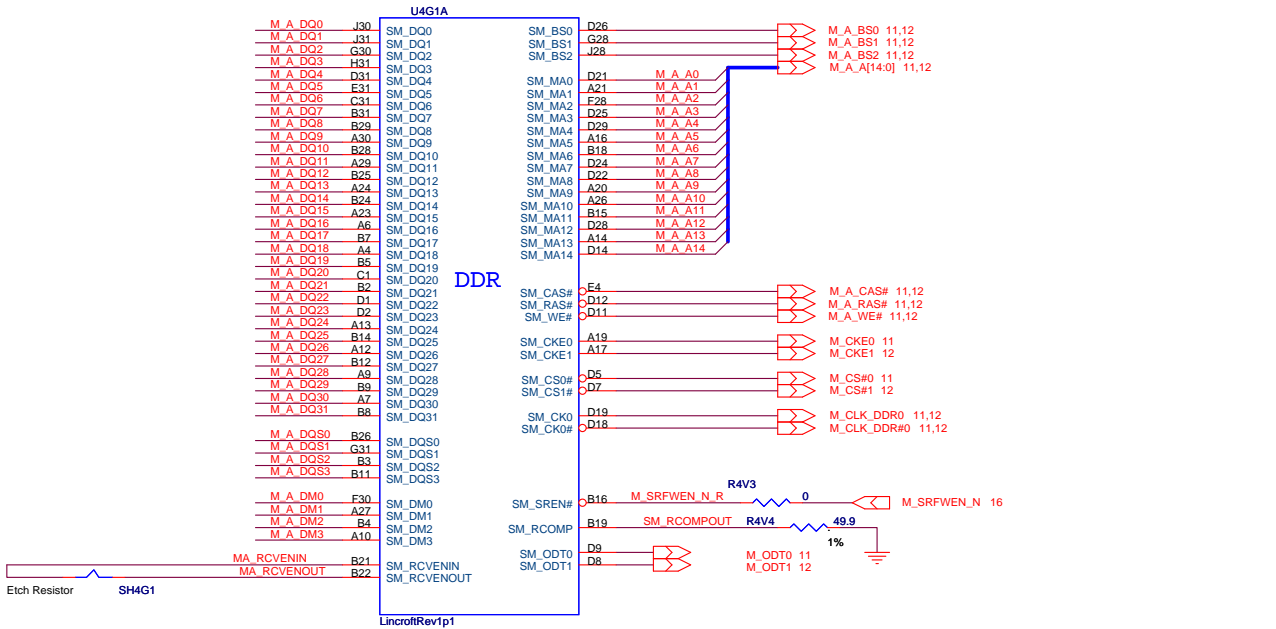
Jumper	Default	Description
J1D1	1-X	Virtual Battery
J1F1	1-X	Force SMC shutdown
J2B2	1-X	Programming EC SPI Flash
J2D1	1-X	EC disable
J2D2	1-X	EC JTAG enable
J2D3	1-X	LVDS PWN selection (Normal PWM or Inverted PWM)
J2D4	1-X	LID switch
J2F1	1-X	Backlight select - I2C based or Pwm based
J7A1	1-X	Programming WPT SPI Flash
J3D1	1-X	Enable SV setup
J3D4	1-X	EC Reserved 1
J6G2	1-X	WPT JTAG select
J7C3	1-X	DDR Ratio select
J9F1	1-X	Force VID Enable
J9F2	1-X	Force VID Enable
J2A2	2-3	EC debug on RS232
J2B1	2-3	EC debug on RS232
J6C3	1-2	1.8V or 3.3V selection for SD interface
J7C1	1-X	GPIO expander
J7C2	1-X	GPIO expander
J7C5	2-3	PMIC GPIO voltage selection
J8A1	1-X	Manufacturing mode
J9A1	1-X	GPIO Expander
J9B1	1-X	GPIO Expander
J9B2	1-X	GPIO Expander
J9B4	2-3	PCIe slot power control -- 3.3U or 3.3S
J9D2	2-3	PCIe slot power control -- 3.3U or 3.3S

SMBUS/I2C ADDRESSES

I2C/SMBUS	DEVICE	ADDRESS
WPT		
I2C0	ACCELEROMETER	30H
I2C0	COMPASS	3CH
I2C0	XDP	
I2C1	LVDS	
I2C2	HDMI	
EC		
SMB_THRM	LINCROFT THERMAL SENSOR	98H
SMB_THRM	SKIN THERMAL SENSOR	96H
SMB_THRM	ALS	52H
SMB_GEN	BOARD ID	30H
SMB_GEN	DRIVER FOR 7 SEG	70H
SMB_BS	BATTERY CHARGER	-

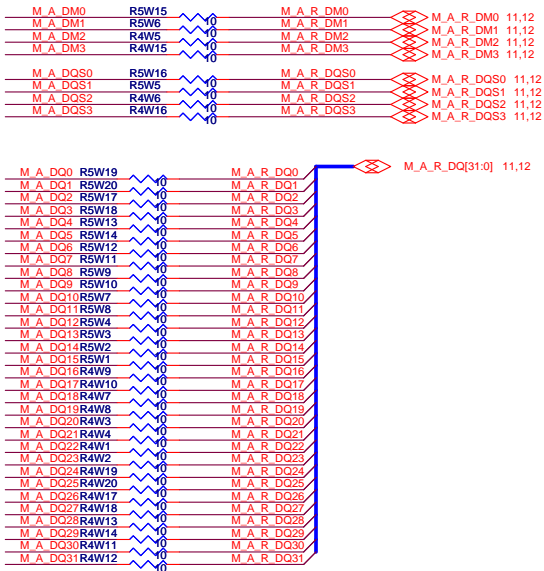
ALPINE BAY			Intel Confidential
Title			NOTES
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	2 of 58

Lincroft North Complex (1 of 6)



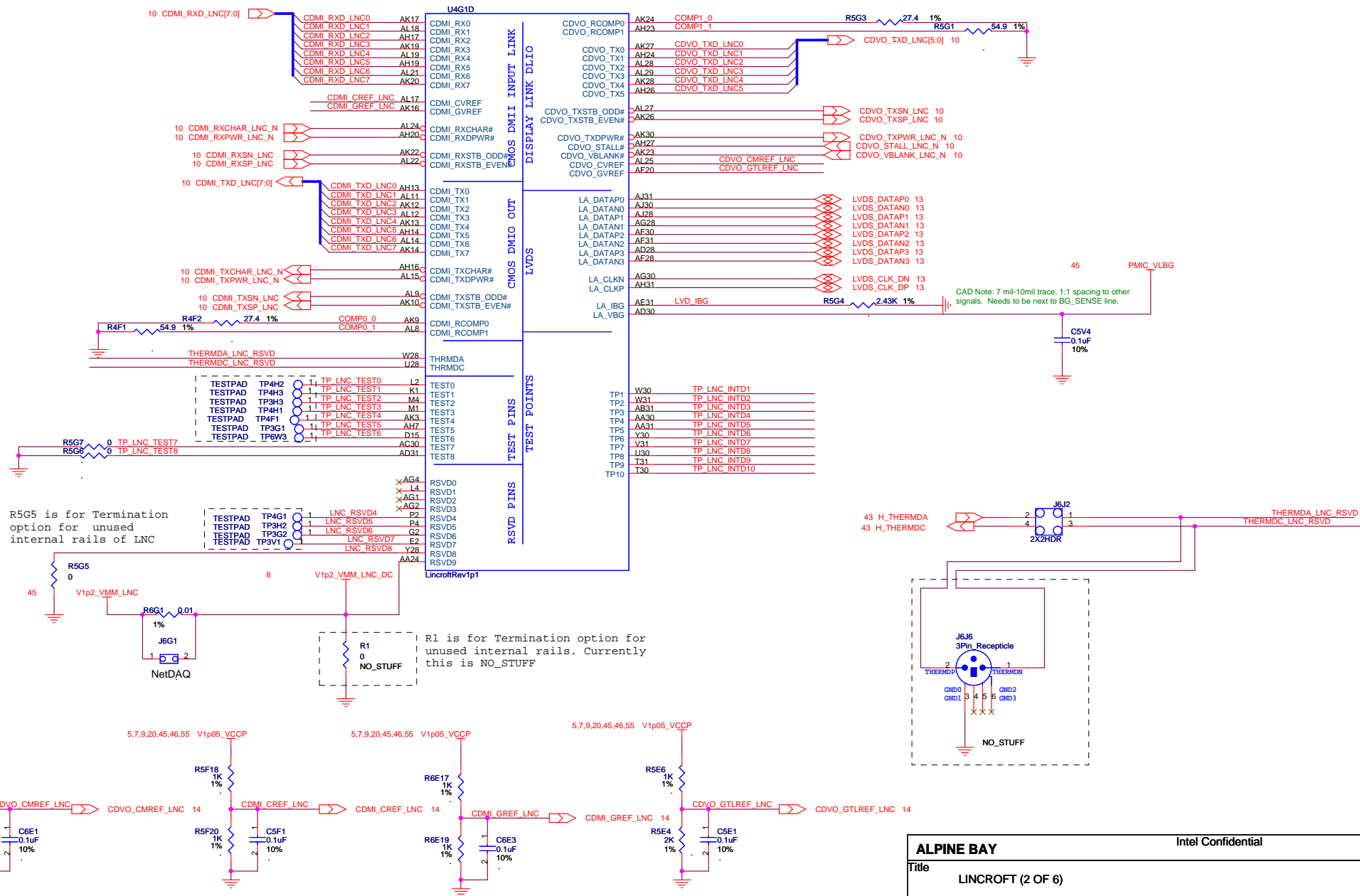
DDR2 terminations

Only DDR Control and data signal terminations are stuffed



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Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	3 of 58

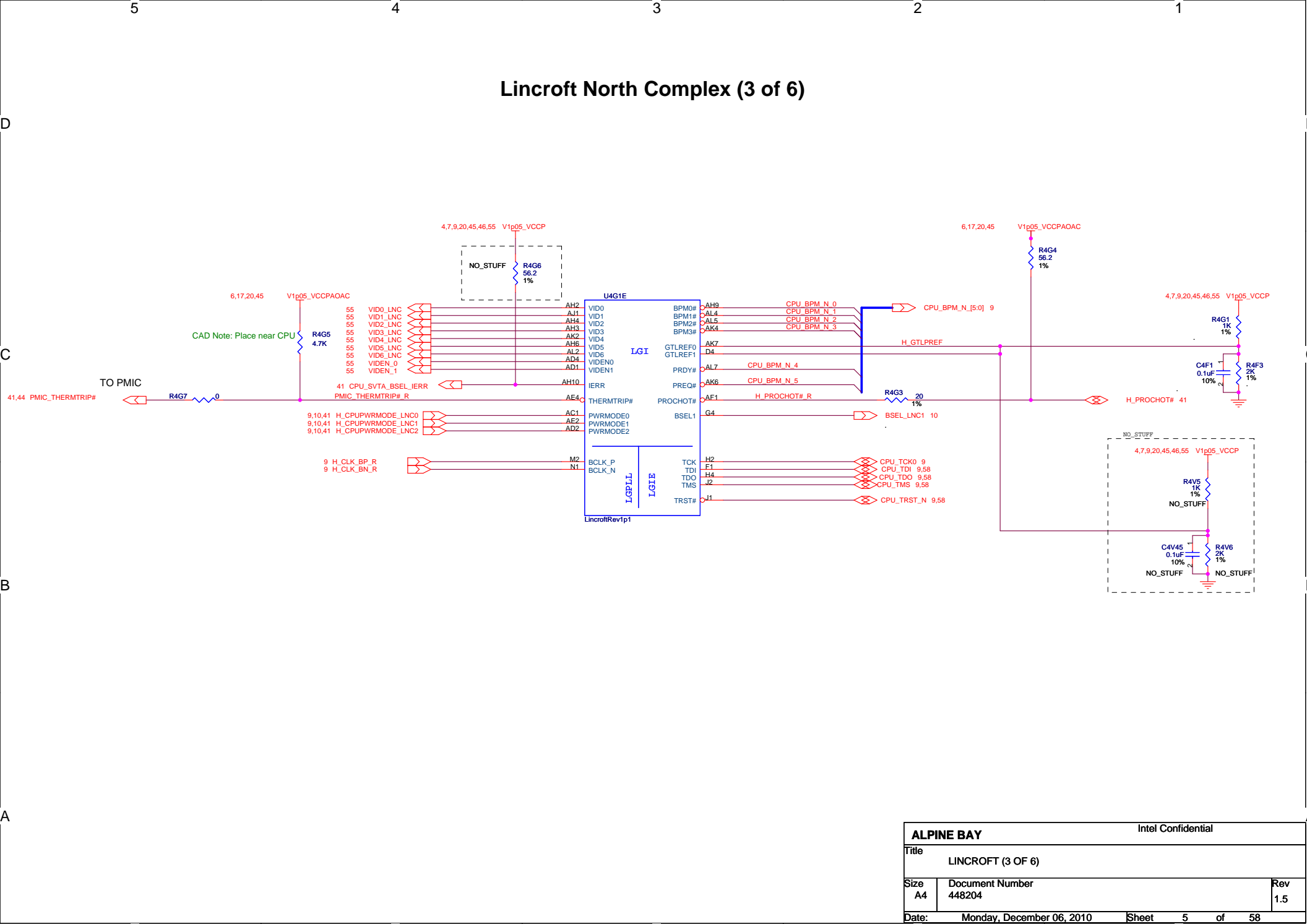
Lincroft North Complex (2 of 6)



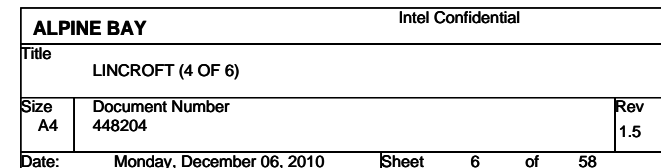
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Size A4	Document Number 448204	Rev 1.5	
Date:	Monday, December 06, 2010	Sheet	4 of 58

Lincroft North Complex (3 of 6)

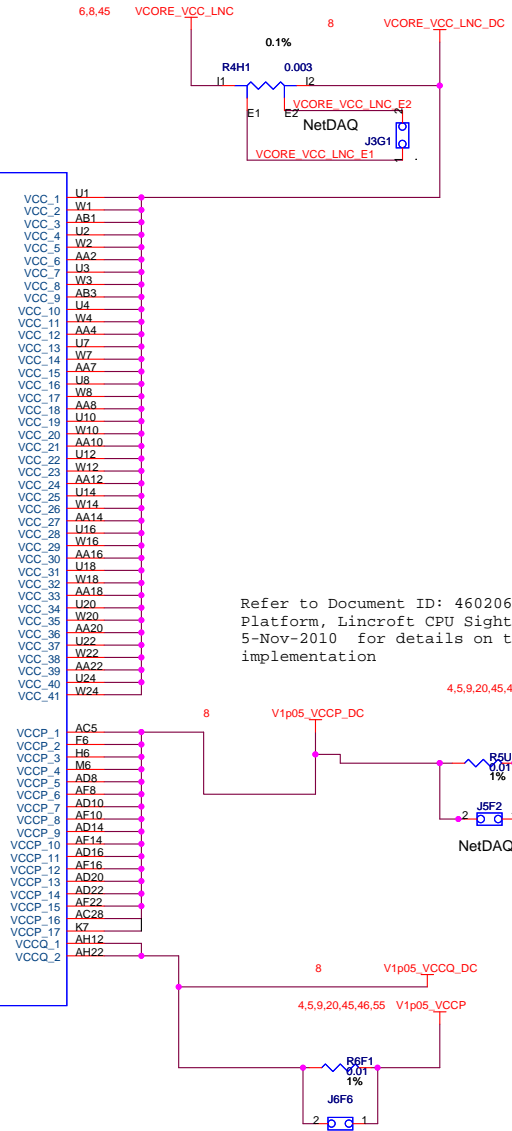
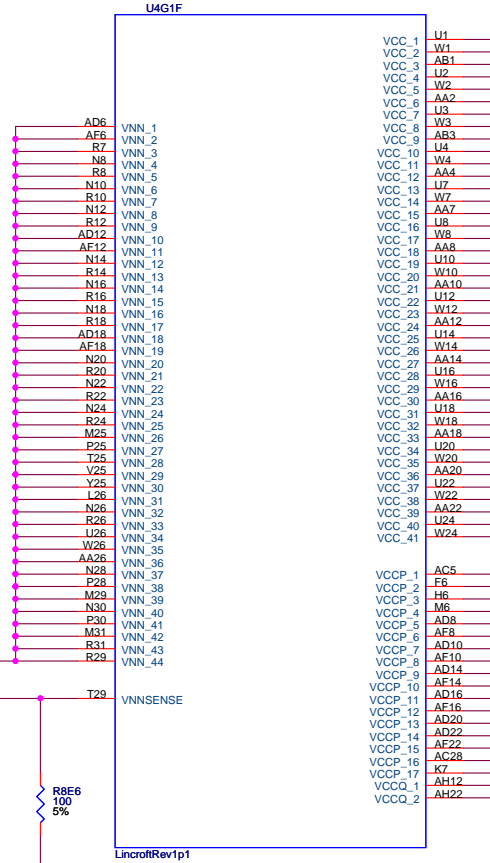
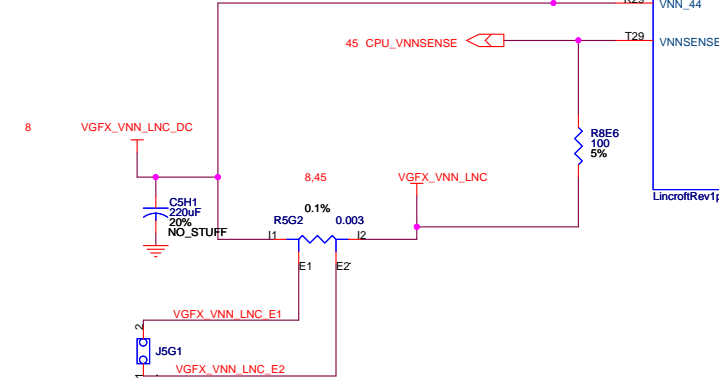
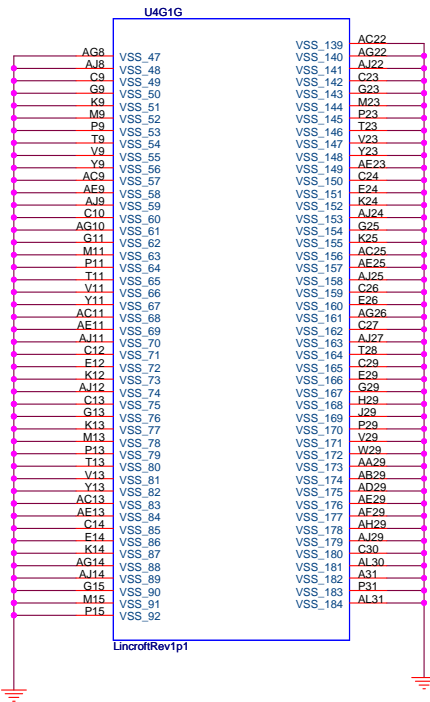
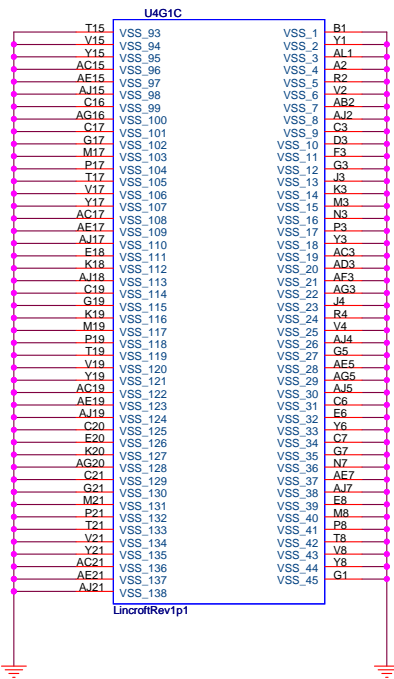
D
C
B
A



A



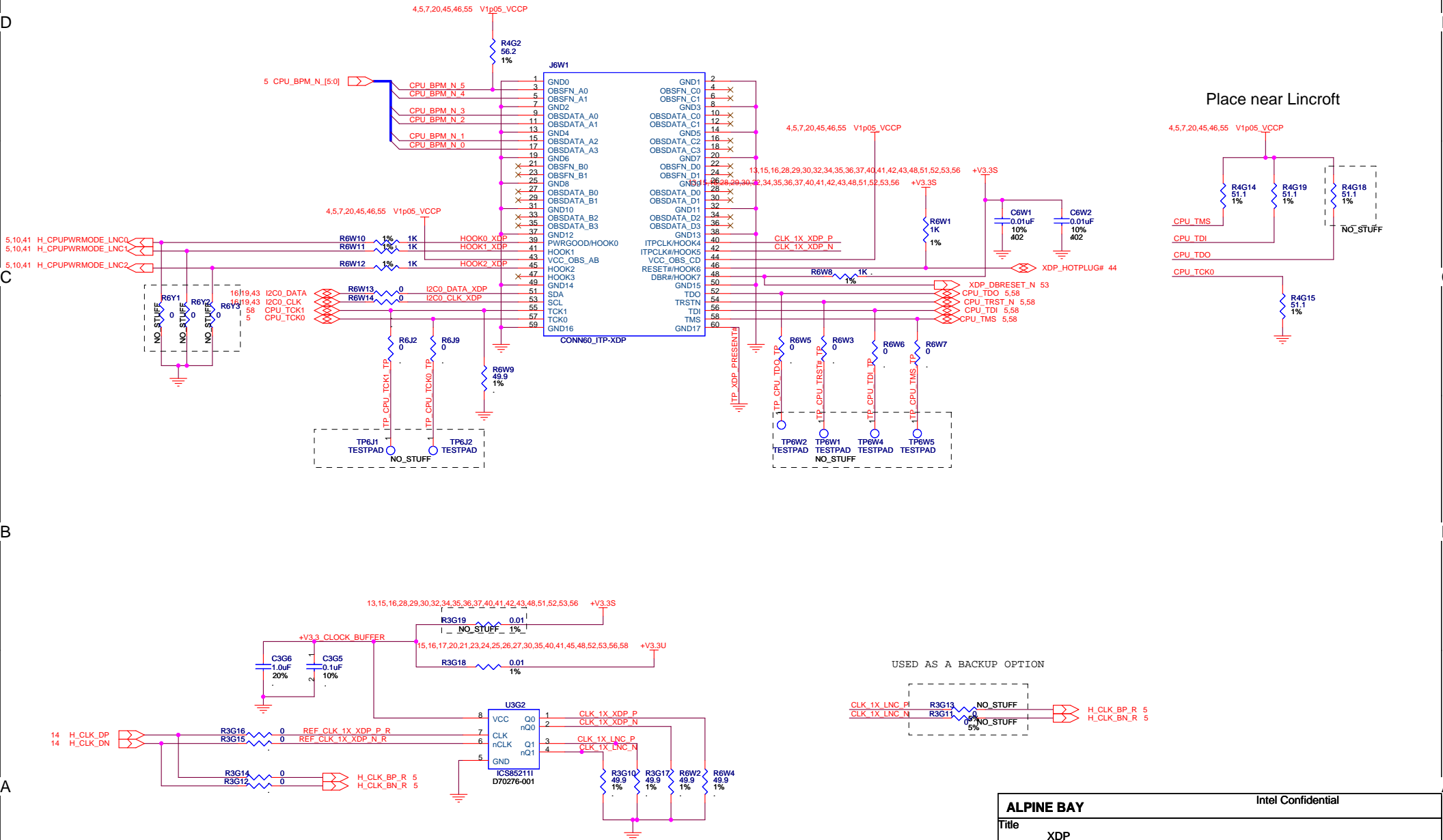
Lincroft North Complex (5 of 6)



Refer to Document ID: 460206 , [Oak Trail]
Platform, Lincroft CPU Sighting Alert
5-Nov-2010 for details on the VCCP
implementation

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Title					
LINCROFT (5 OF 6)					
Size	Document Number				Rev
A4	448204				1.5
Date:	Monday, December 06, 2010		Sheet	7	of 58

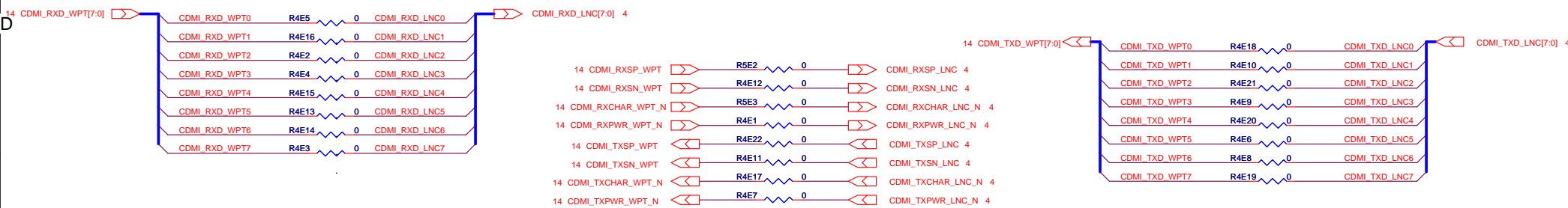
XDP CONNECTOR



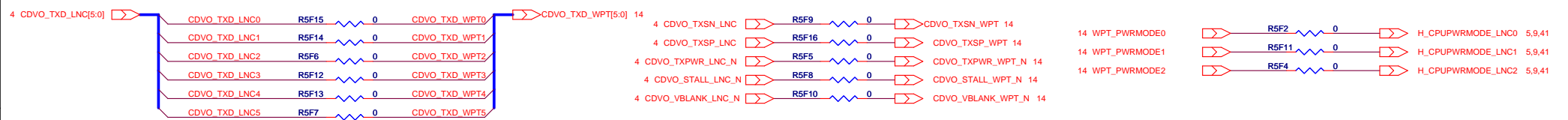
Use clock buffer only if clock needs to be connected to XDP.

ALPINE BAY			Intel Confidential
Title			XDP
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	9 of 58

cDMI STUFFING OPTIONS



cDVO STUFFING OPTIONS

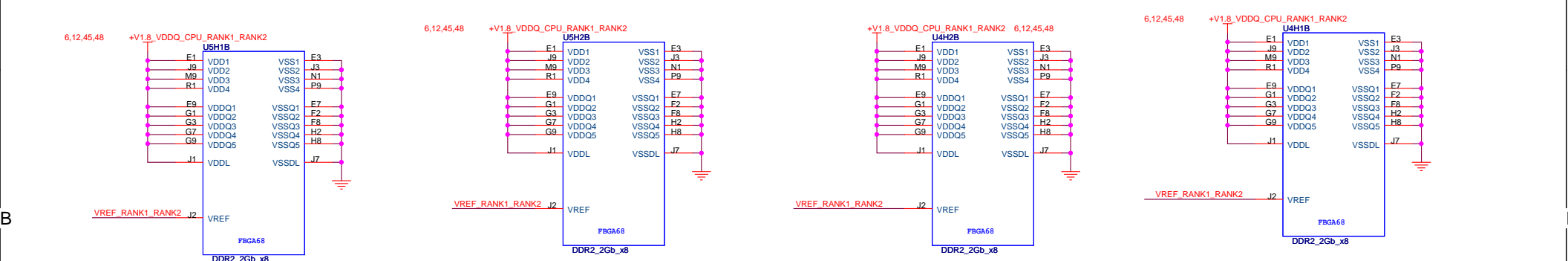
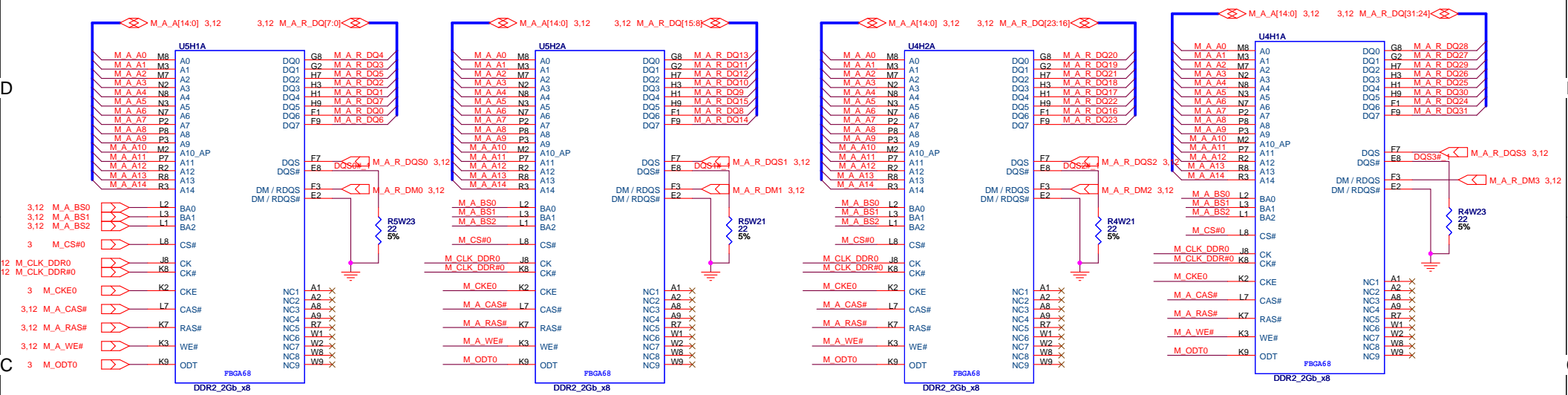


NOTE: RESISTOR STUFFING OPTIONS PROVIDED FOR VALIDATION PURPOSES

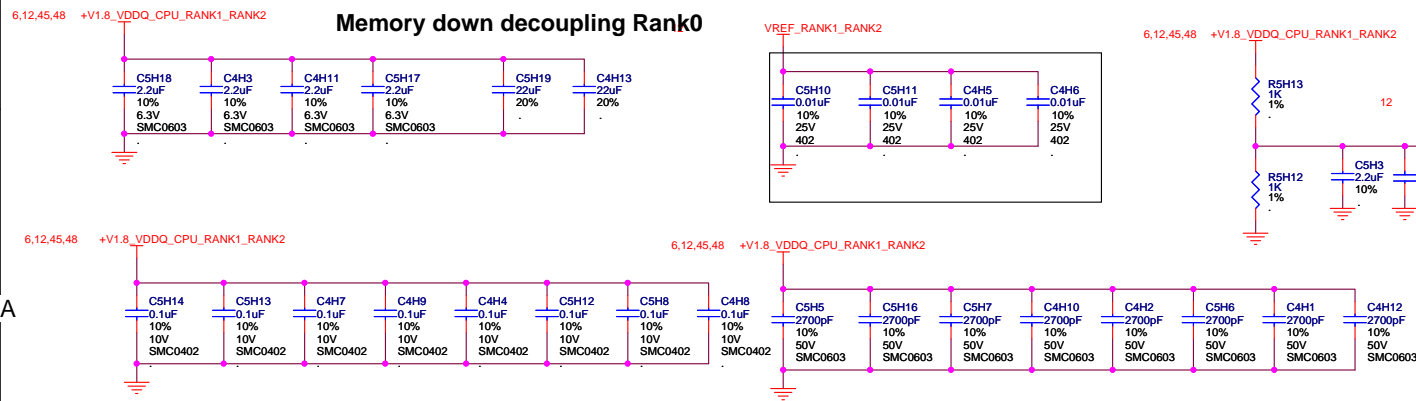


ALPINE BAY		Intel Confidential	
Title		CDMI & CDVO STUFFING	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	10 of 58

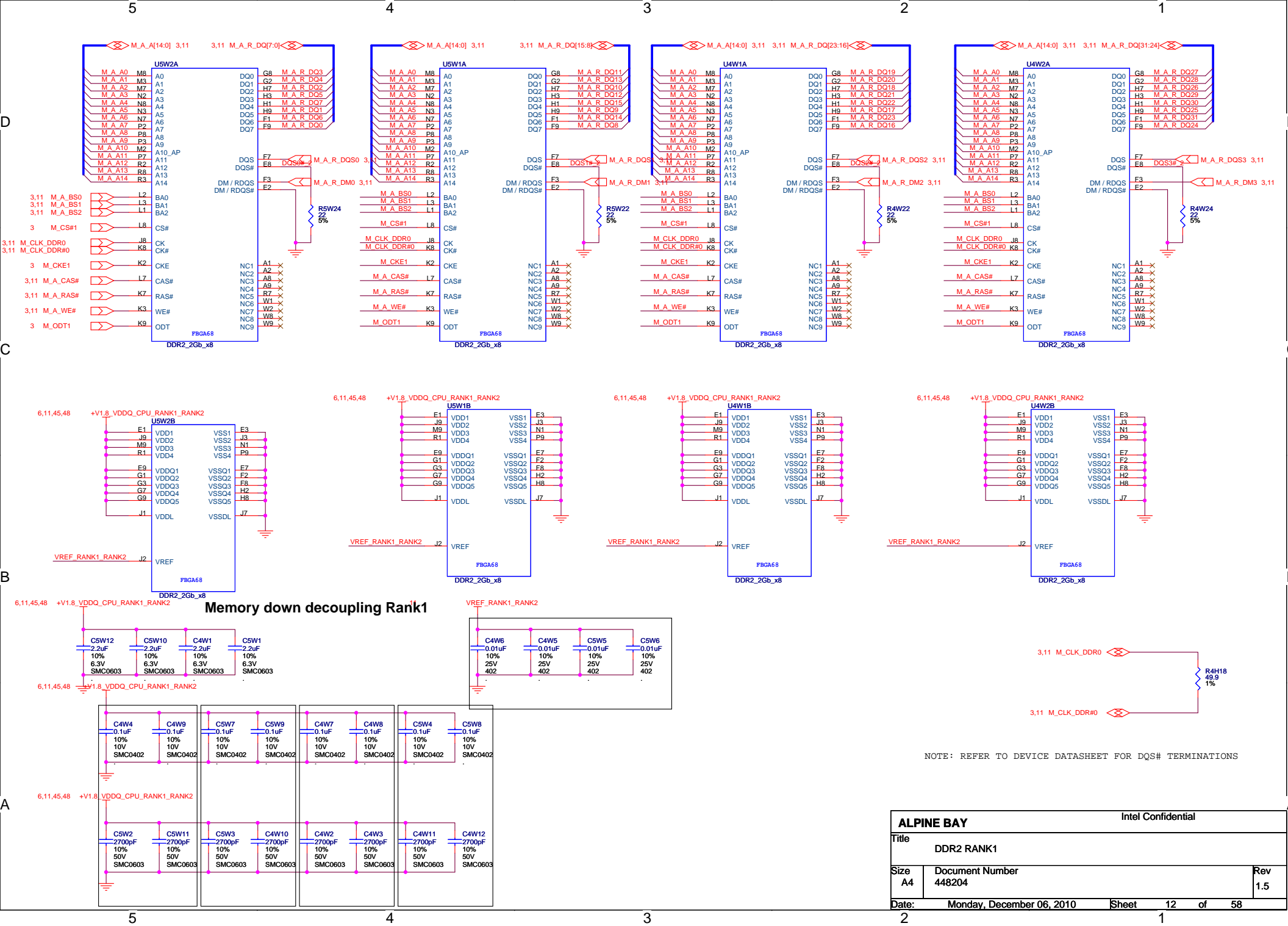
DDR2 Memory Down Rank 0 (TOP)



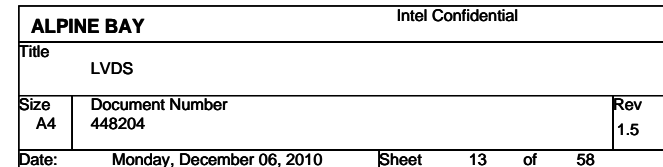
Memory down decoupling Rank0

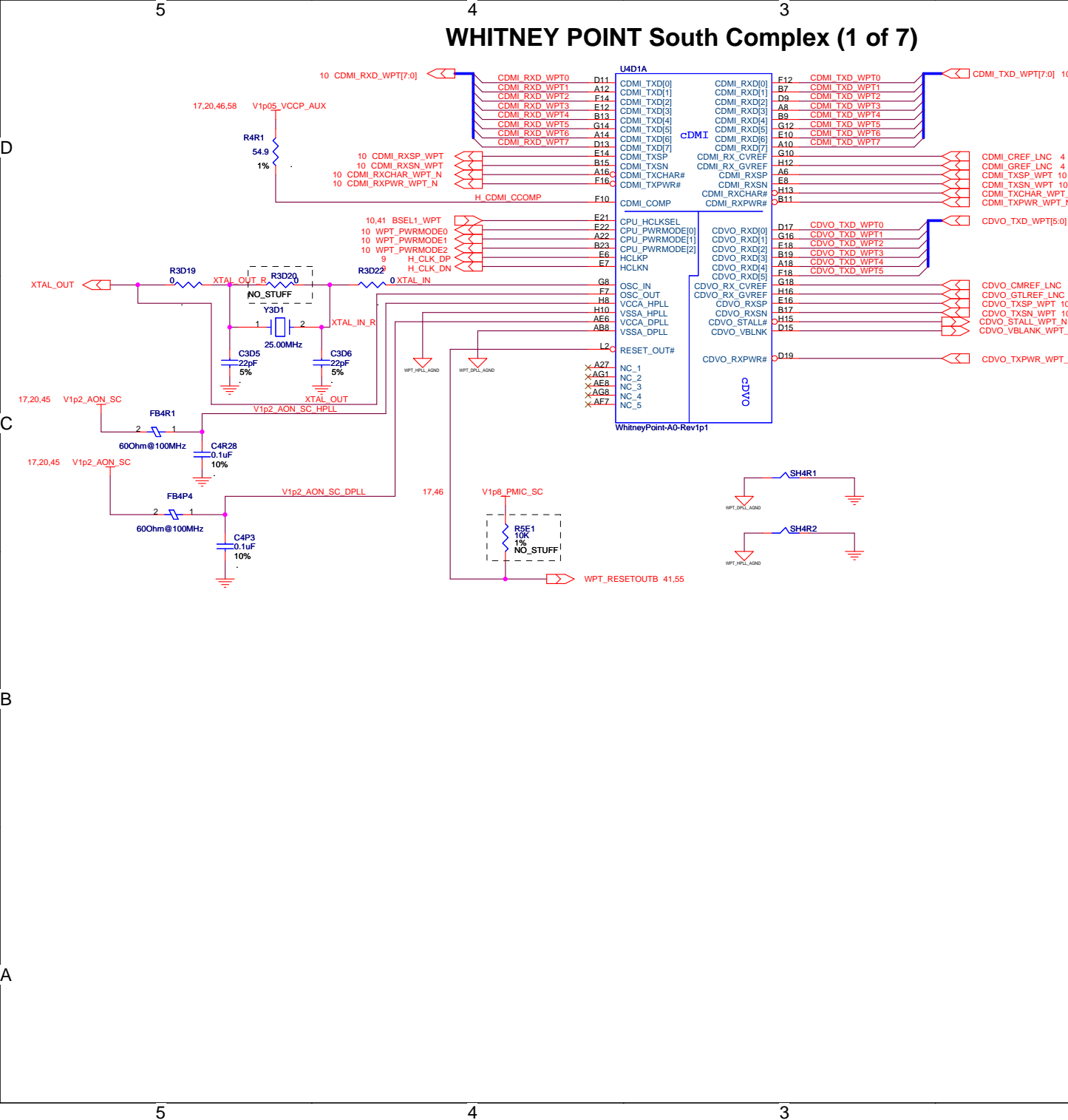


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Title			
DDR2 RANK0			
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010		Sheet 11 of 58

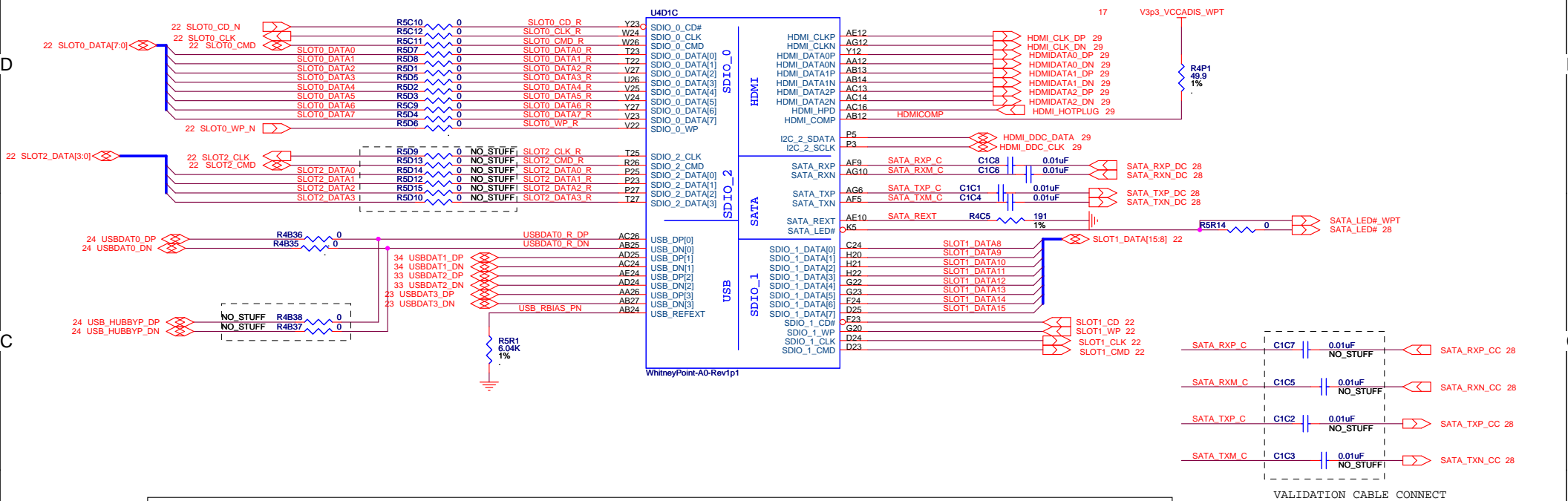


BOM NOTE:
Stuff R3V5 and NO_STUFF
R3V19 to override VDDEN option
on board



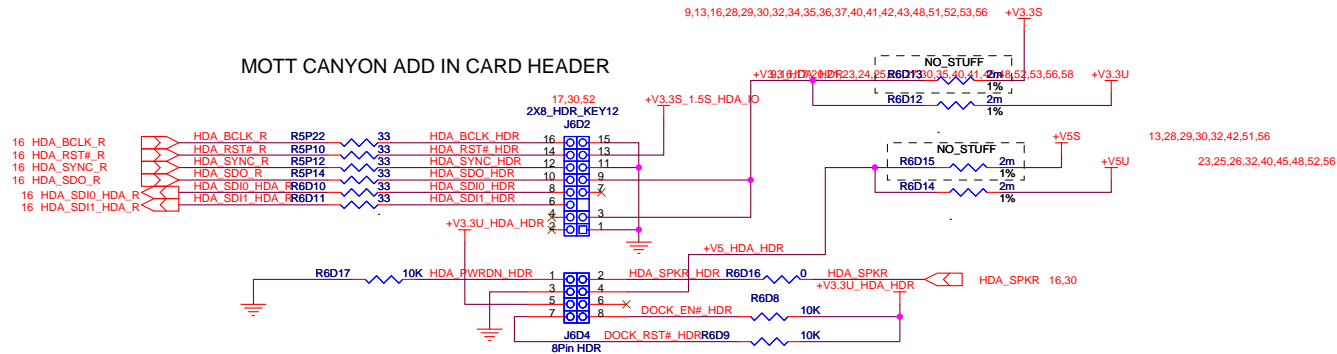
[illegible]

WHITNEY POINT South Complex (2 of 7)



HD AUDIO HEADER

MOTT CANYON ADD IN CARD HEADER



ALPINE BAY			Intel Confidential
Title			
WHITNEY POINT (2 OF 7)			
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	15 of 58

D



CODEC DEVICE DOWN IMPLEMENTATION

MOTT CANYON ADD IN CARD SUPPORT

If HDMI is implemented HDA_SDIO is internally used for HDMI audio. In that case HDA_SDIO must be connected to the external CODEC.



ALPINE BAY		Intel Confidential	
Title WHITNEY POINT (3 OF 7)			
Size A4	Document Number 448204	Rev 1.5	
Date:	Monday, December 06, 2010	Sheet	16 of 58

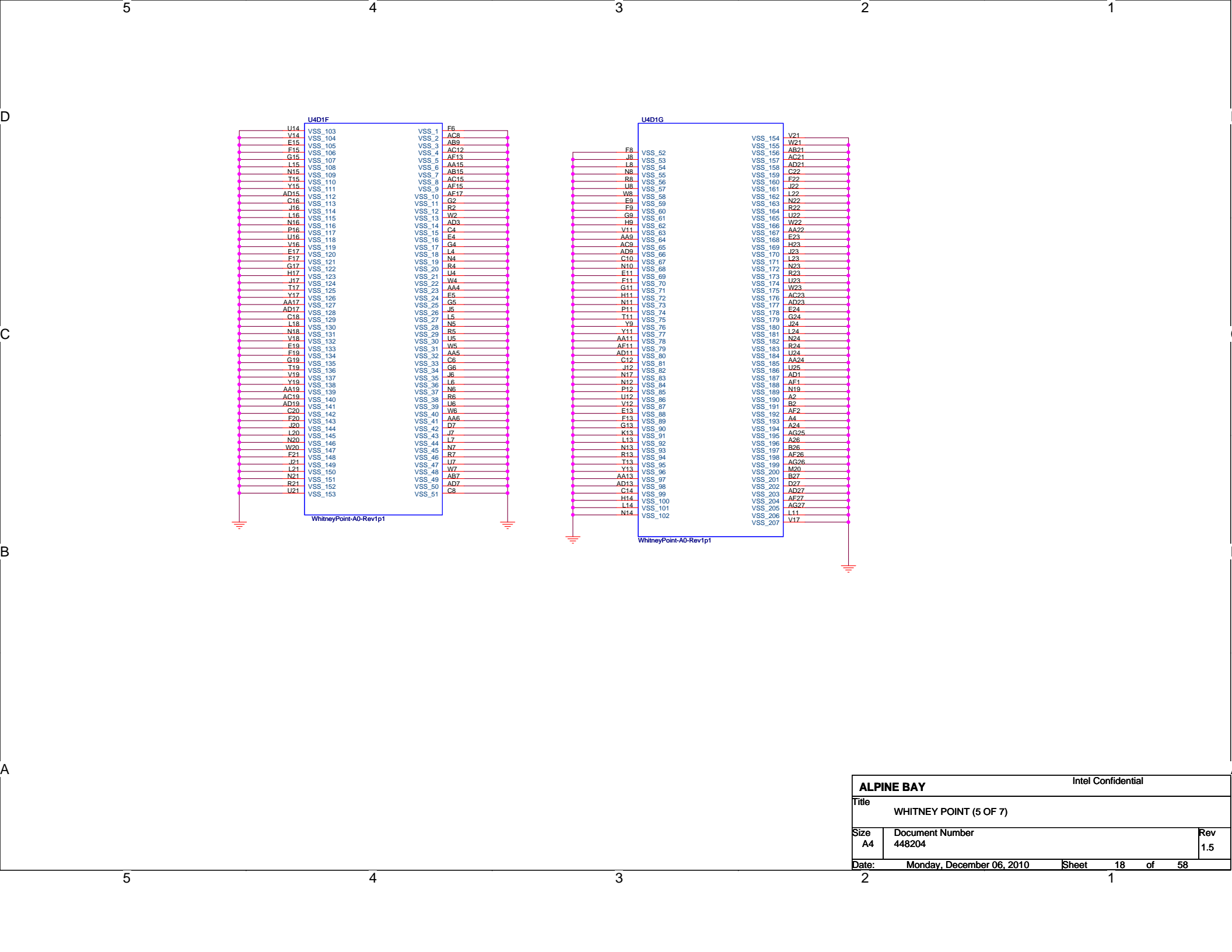
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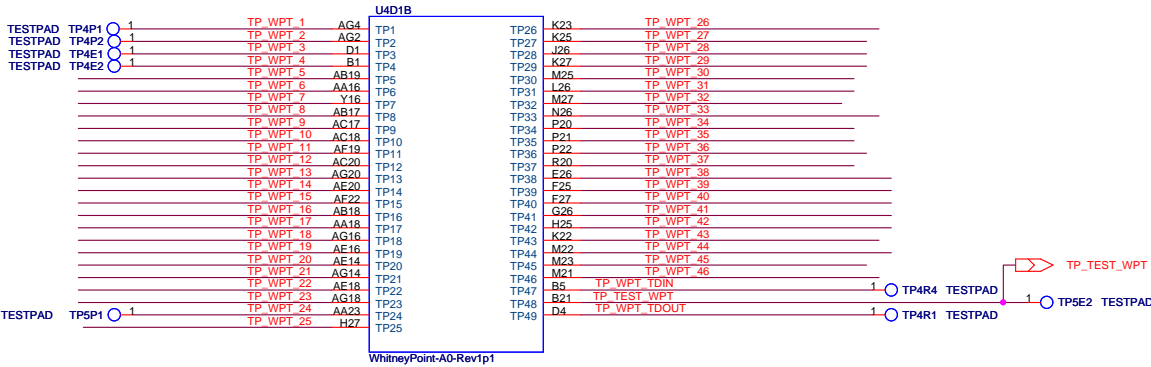
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Rev
1.5

Rev
1.5

Date: Monday, December 06, 2010 Sheet 17 of 58



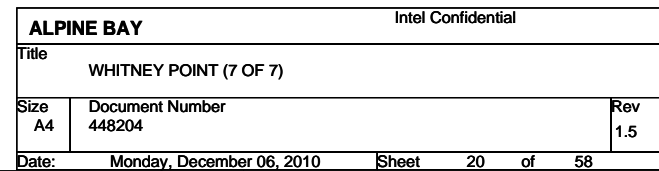


3-PIN HEADER FOR I2C0



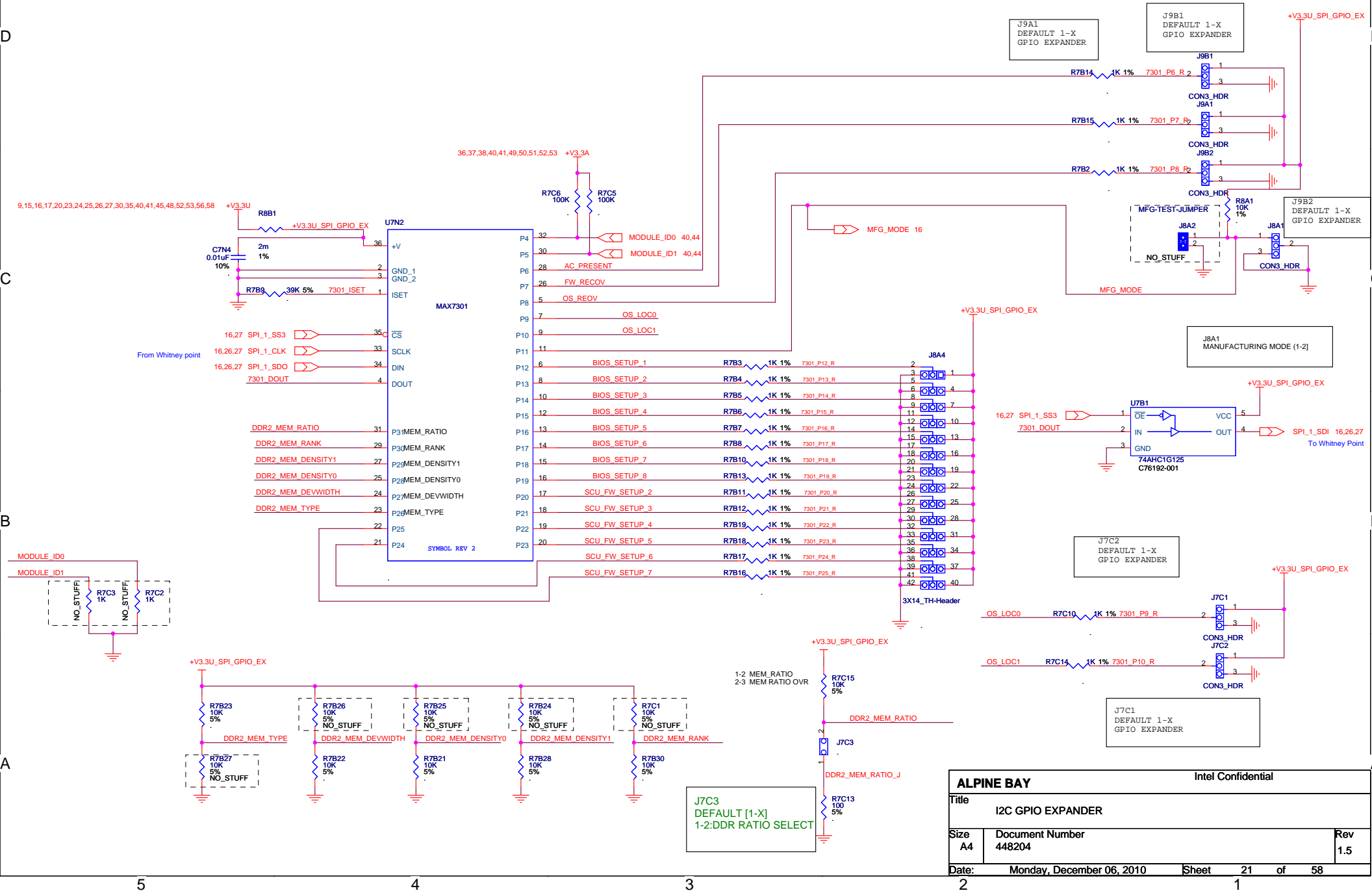
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Title			
WHITNEY POINT (6 OF 7)			
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet 19 of 58	

(REFER TO DESIGN GUIDE FOR OPTIMIZED PDBOM)



I2C GPIO EXPANDER

(GPIO EXPANDER CIRCUIT FOR VALIDATION PURPOSE ON CRB)

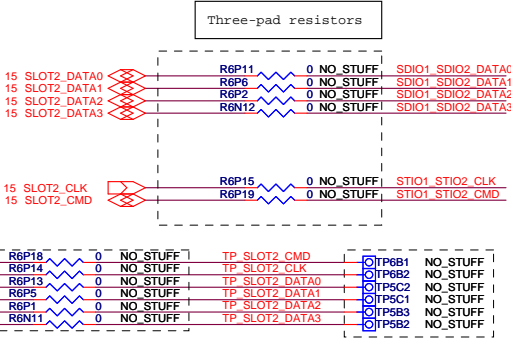
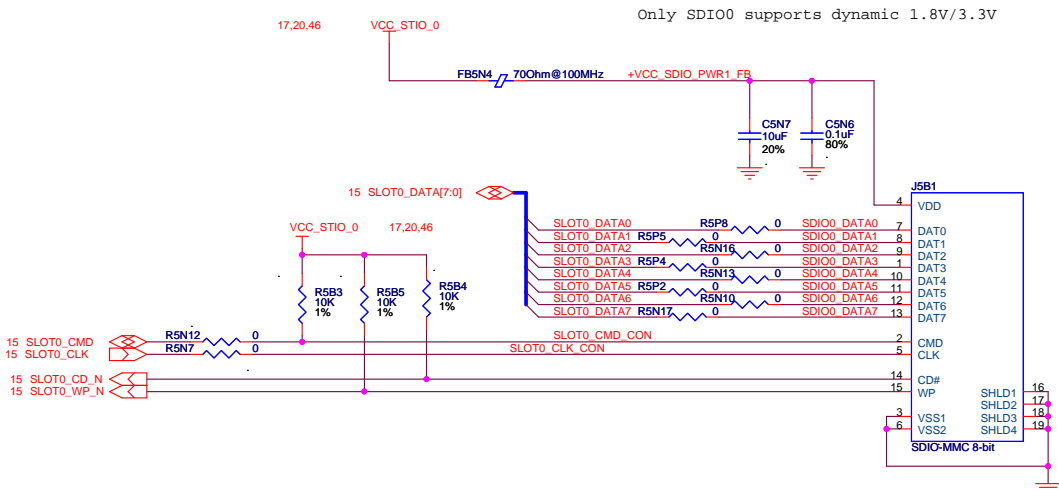


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Title			
I2C GPIO EXPANDER			
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	21 of 58

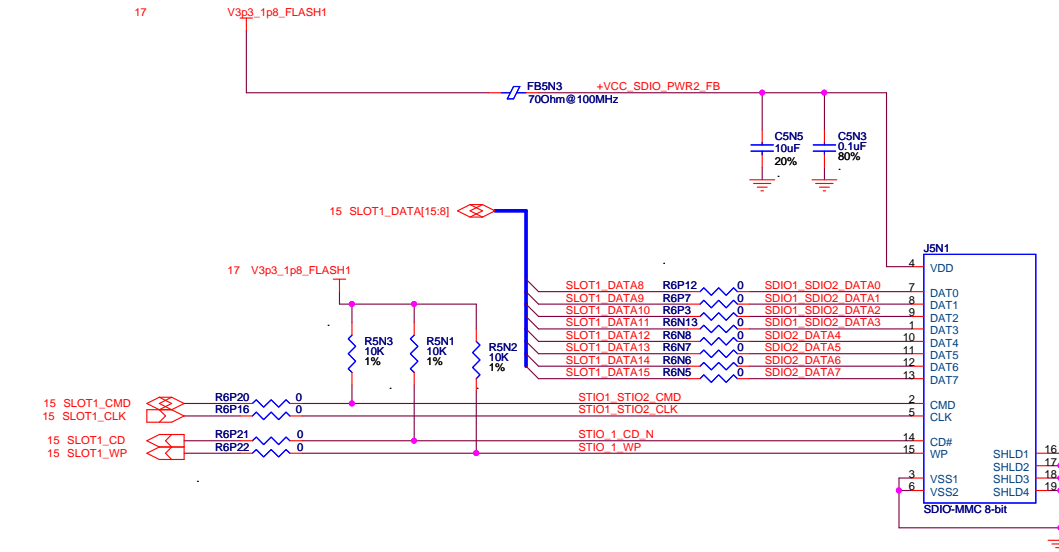
SDIO/MMC

SDIO0

Note: Refer to the Technical Advisory [Whitney Point] Chipset, Sighting Update (#3462612).
The doc # on CDI is 458825.

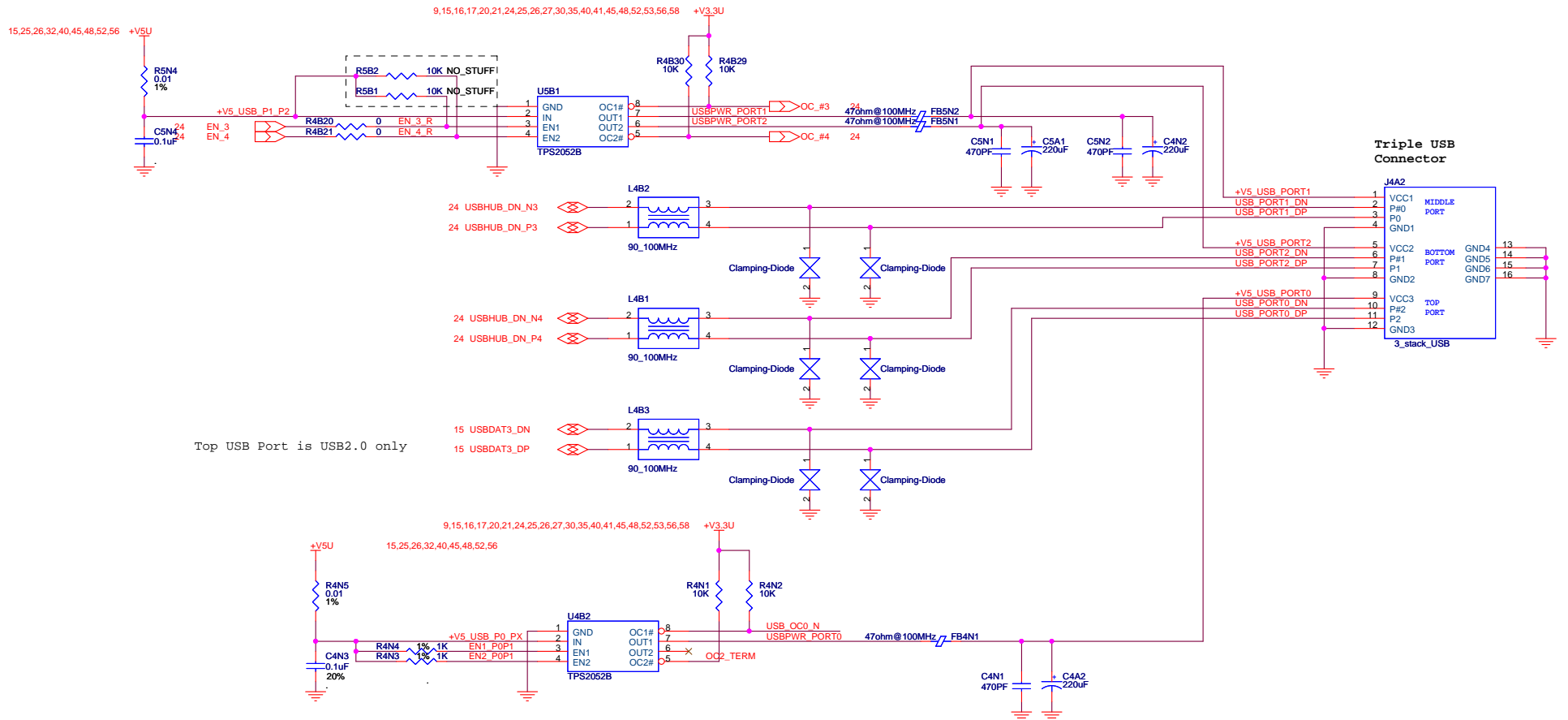


SDIO1



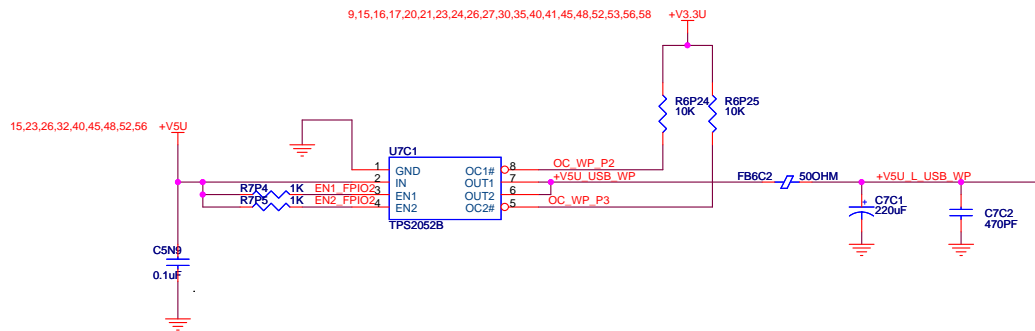
ALPINE BAY		Intel Confidential	
Title		SDIO/MMC	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	22 of 58

USB 2.0 (Back Panel)

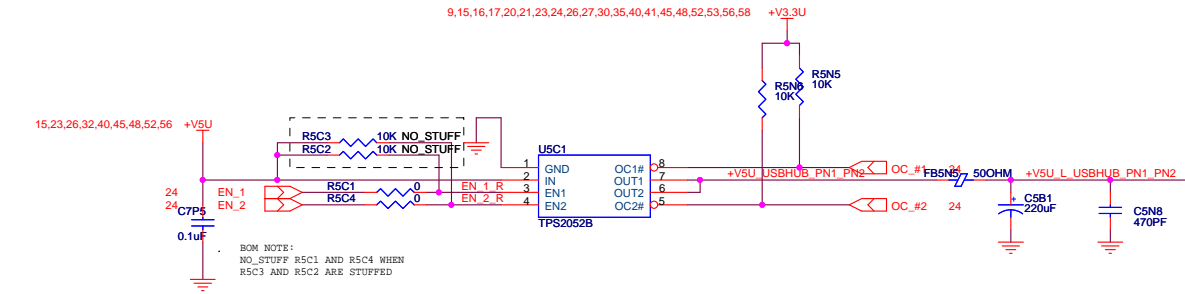
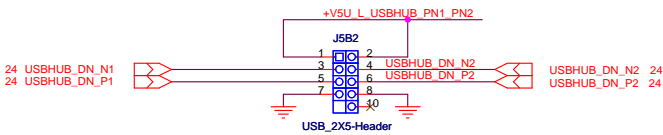


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Title		USB (1 OF 3)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	23 of 58

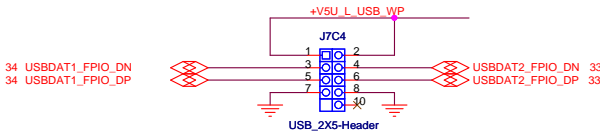
USB(FRONT PANEL)
(FOR UPHAM ADD IN CARD)



FRONT PANEL HEADER 1
Port 1, 2 from HUB



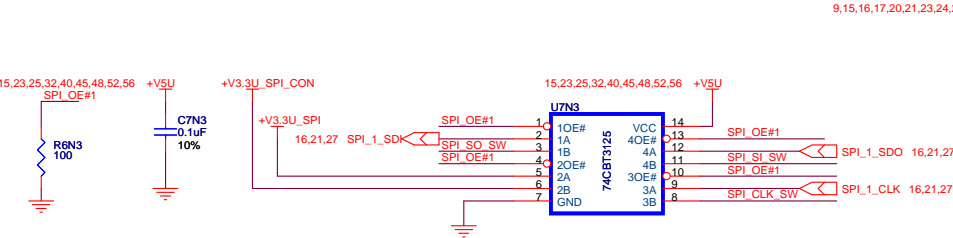
FRONT PANEL HEADER 2
From WPT



ALPINE BAY		Intel Confidential	
Title		USB (3 OF 3)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	25 of 58

SPI DEVICE FOR WHITNEY POINT

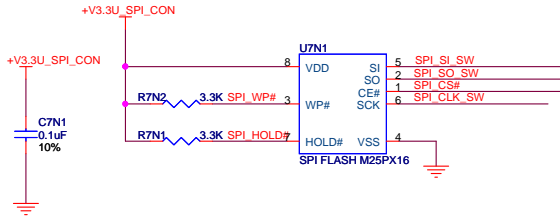
FET SWITCH FOR ISOLATION



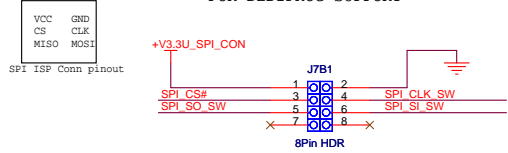
Provided for on board SPI programming

J7A1 (SPI PROGRAMMING HEADER)
1-X -- DEFAULT
1-2 -- TO PROGRAM SPI THROUGH DEDIPROG

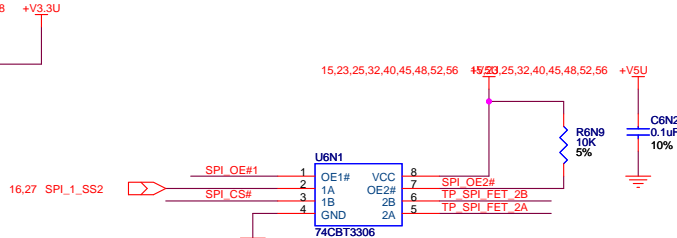
8 PIN SPI DEVICE



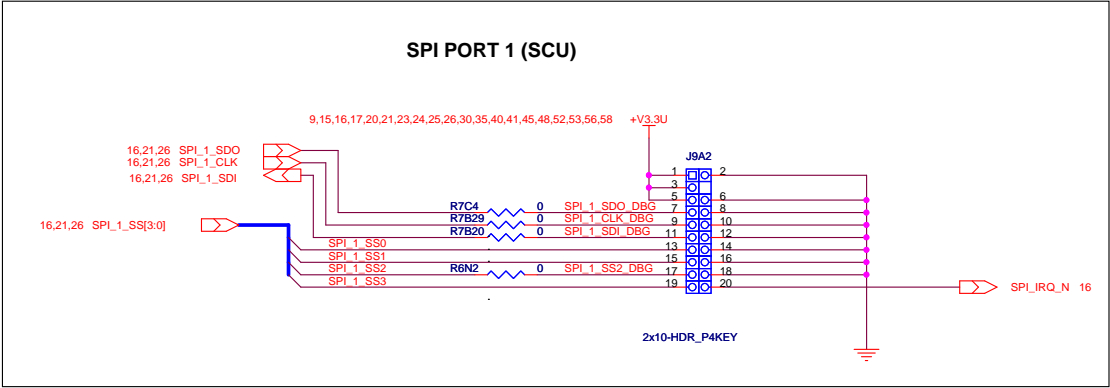
SPI PROGRAMMING HEADER
FOR DEDIPROG SUPPORT



FET SWITCH FOR ISOLATION



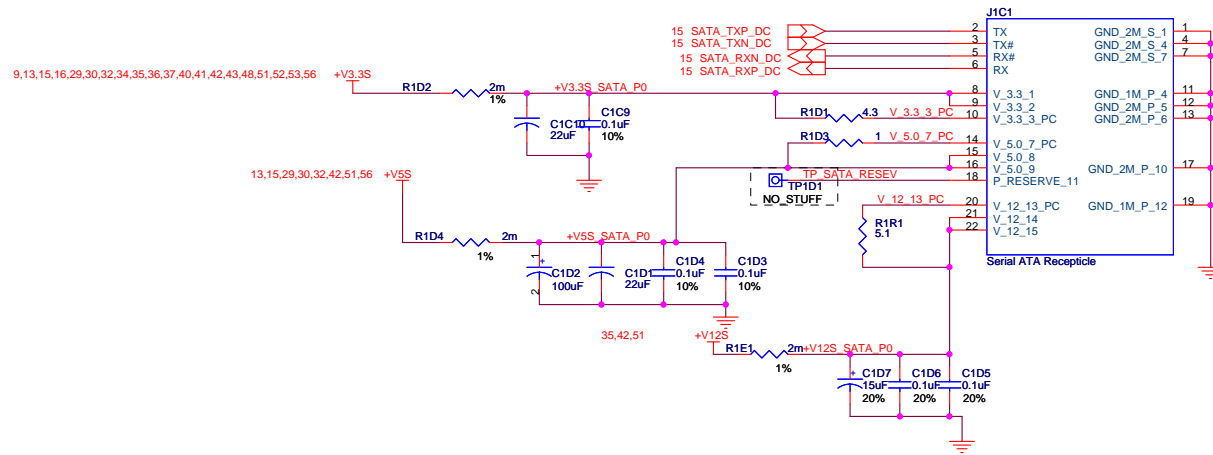
SPI PORTS
(FOR VALIDATION PURPOSES ON CRB)



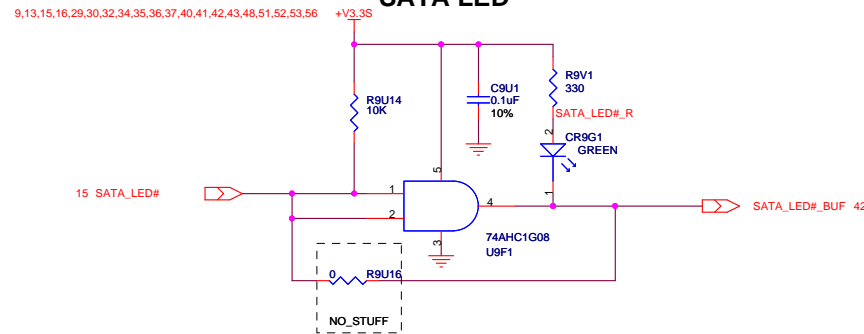
ALPINE BAY		Intel Confidential	
Title		SPI (2 OF 2)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	27 of 58

SATA PORT

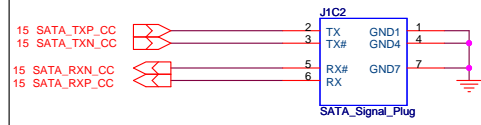
SATA DIRECT CONNECT



SATA LED



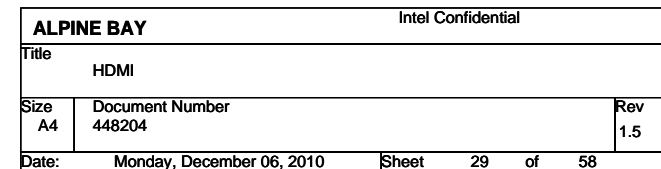
SATA CABLE CONNECT (OPTIONAL)



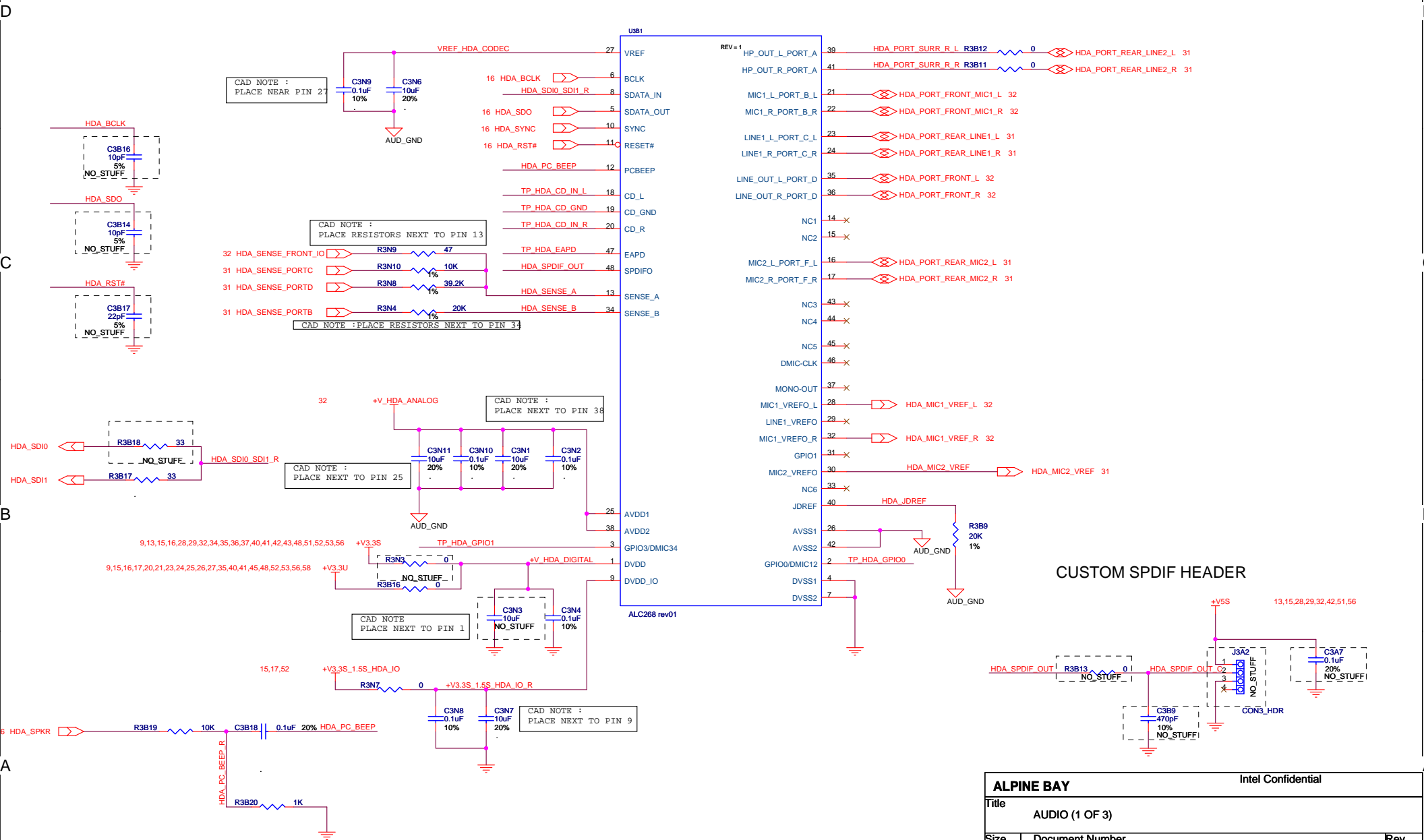
VALIDATION CABLE CONNECT

ALPINE BAY			Intel Confidential
Title			SATA
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	28 of 58

D

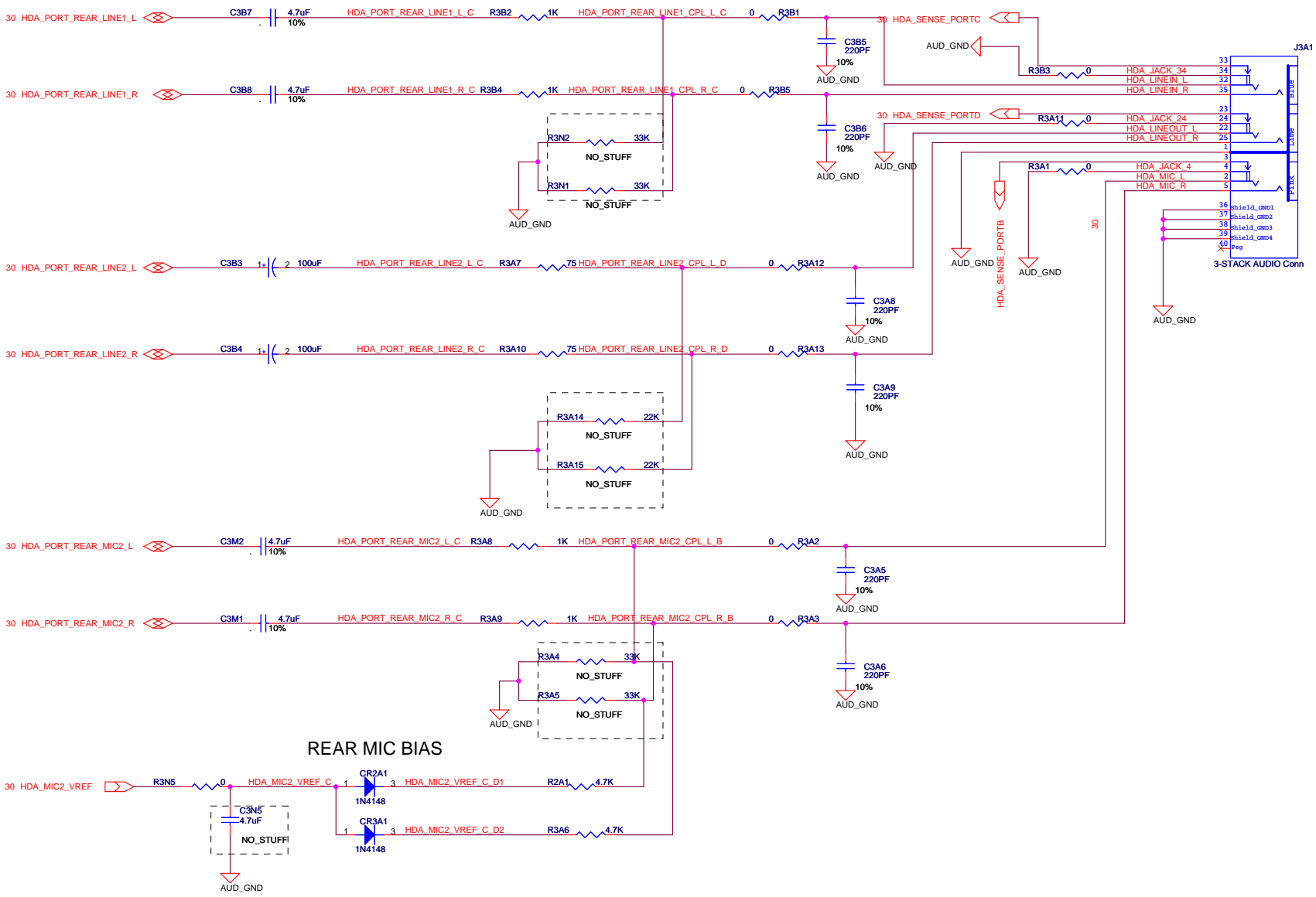


AUDIO CODEC



ALPINE BAY		Intel Confidential	
Title		AUDIO (1 OF 3)	
Size	A4	Document Number	448204
Date:	Monday, December 06, 2010		Rev 1.5
Sheet	30	of	58

BACK PANEL AUDIO JACK



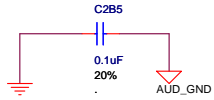
ALPINE BAY		Intel Confidential	
Title		AUDIO (2 OF 3)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	31 of 58

FRONT PANEL AUDIO HEADER

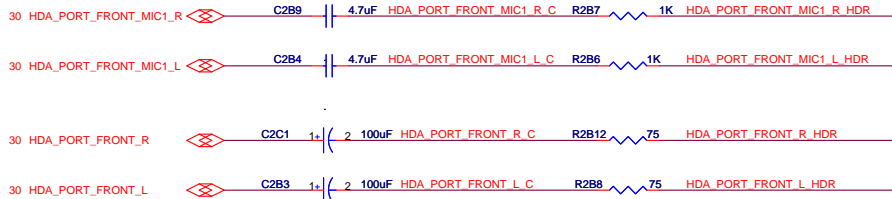
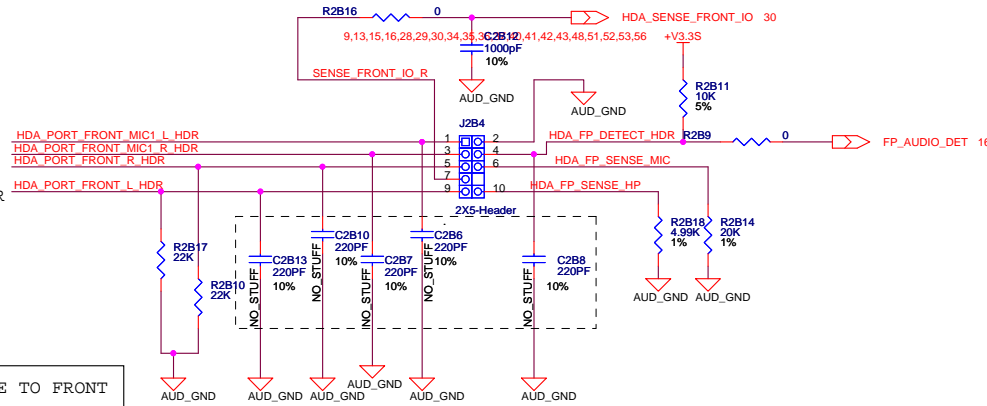
AUDIO FILTER

D

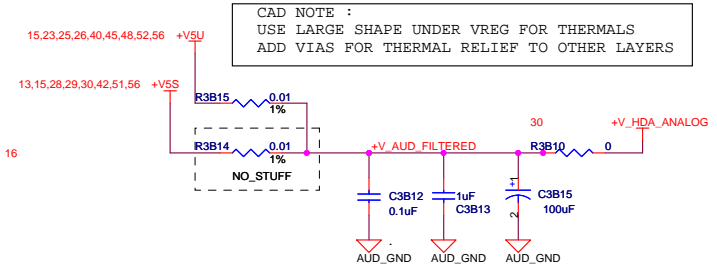
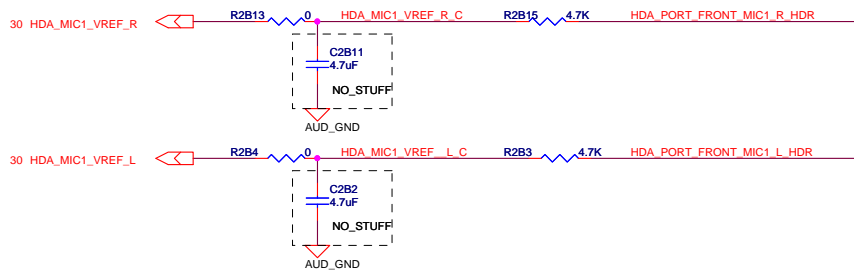
CAD NOTE:
PLACE CLOSE TO FRONT PANEL HEADER



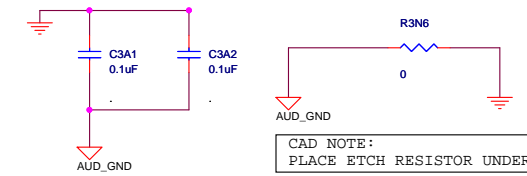
CAD NOTE :PLACE 220PF CAPS CLOSE TO FRONT PANEL CONNECTOR



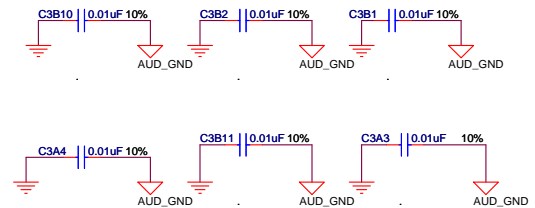
FRONT PORT BIAS



CAD NOTE:
ADD SEVERAL VIAS AFTER ETCH RESISTOR
TO V_HDA_ANALOG



CAD NOTE :
PLACE GROUND::AUD-GROUND DECOUPLING SITE AS
CLOSE AS POSSIBLE TO AUDIO TRIPLE-STACK CONNECTOR



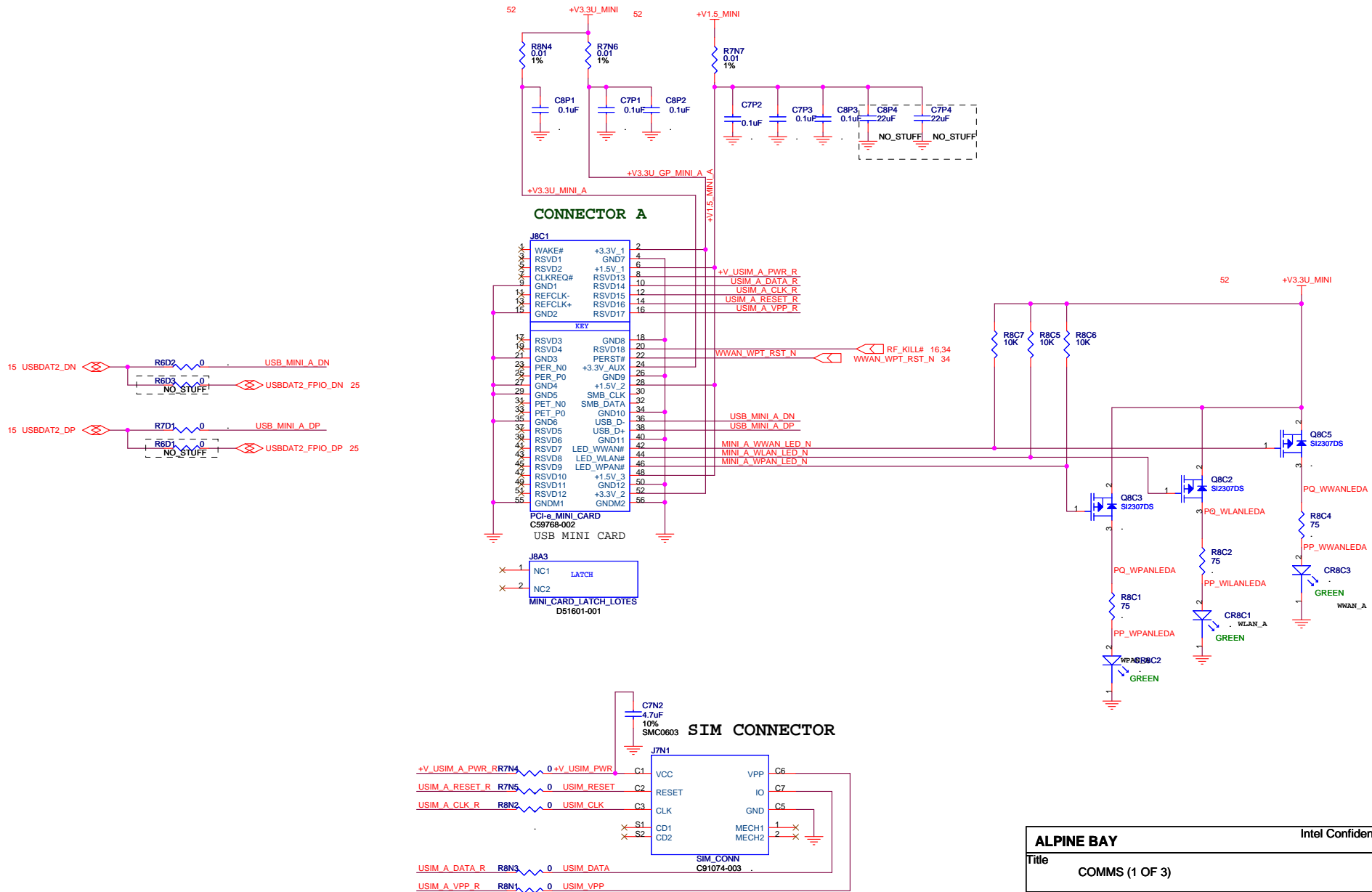
CAD NOTE:
DISTRIBUTE THREE NEAR THE REAR AUDIO JACK.
ONE NEAR THE FRONT PANEL AUDIO CONNECTOR.
REMAINING ALONG ANTI-ETCH BETWEEN ANALOG / DIGITAL GROUND

B

A

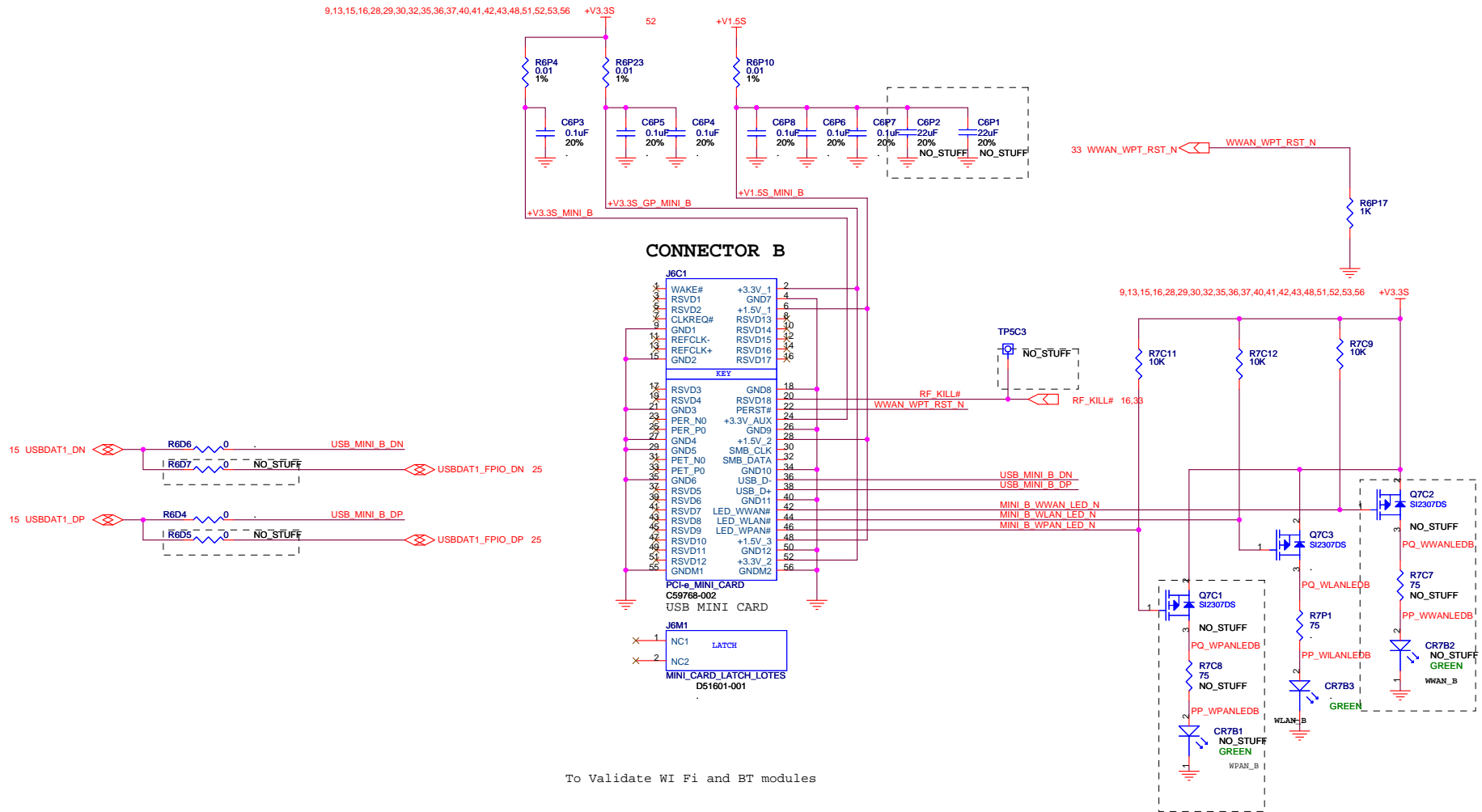
ALPINE BAY		Intel Confidential	
Title		AUDIO (3 OF 3)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	32 of 58

COMMS(1 OF 3)



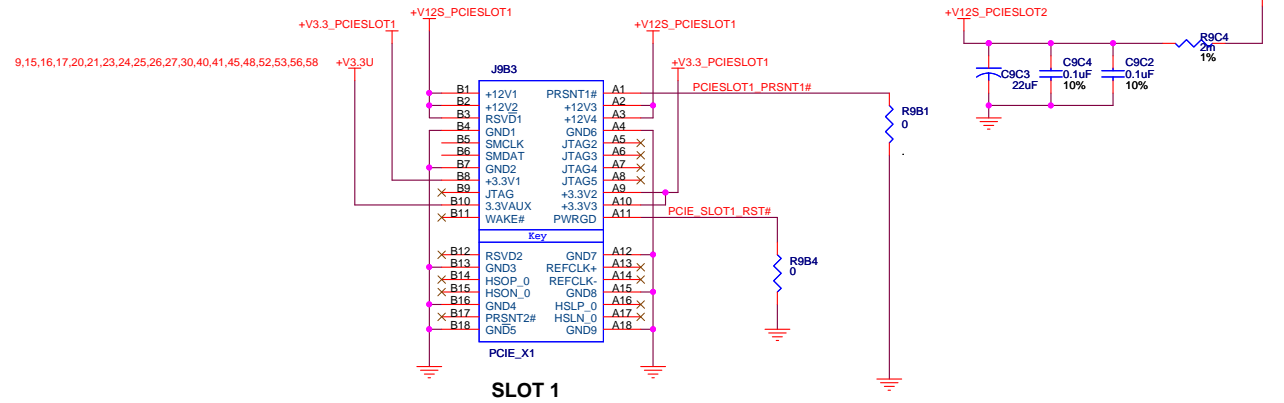
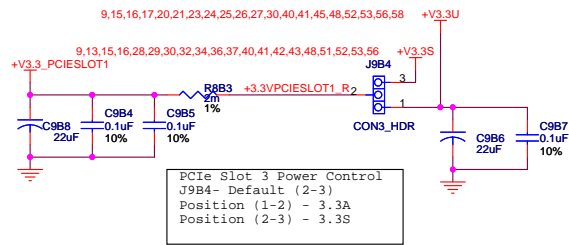
ALPINE BAY		Intel Confidential	
Title		COMMS(1 OF 3)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	33 of 58

COMMS (2 OF 3)

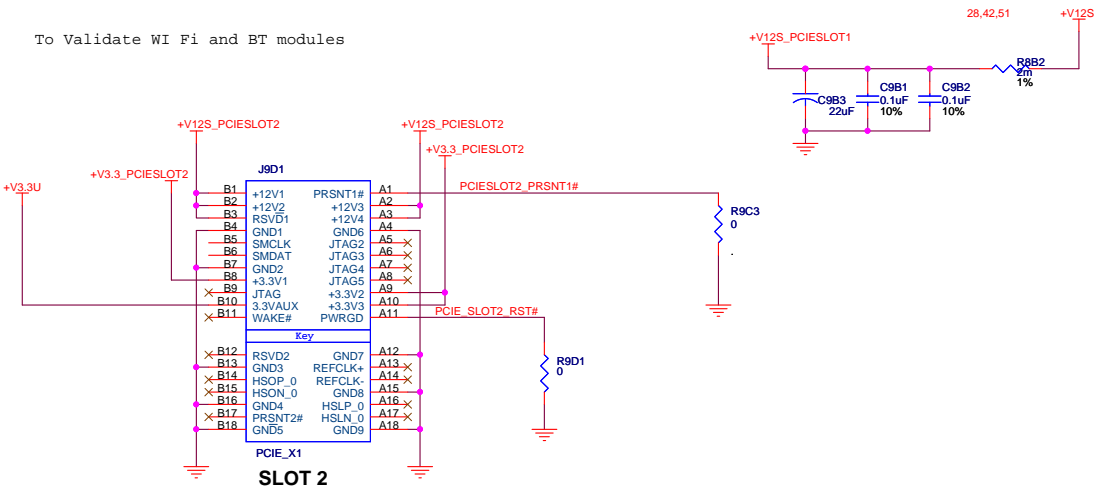
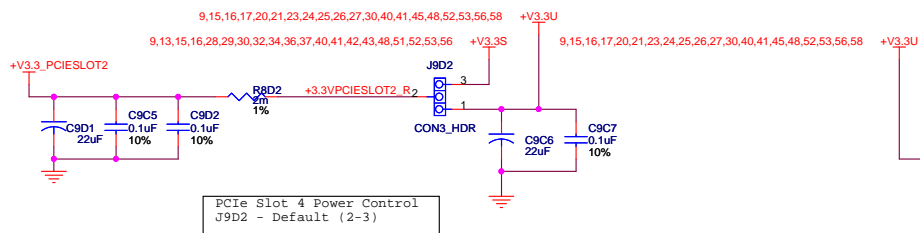


ALPINE BAY		Intel Confidential	
Title		COMMS (2 OF 3)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	34 of 58

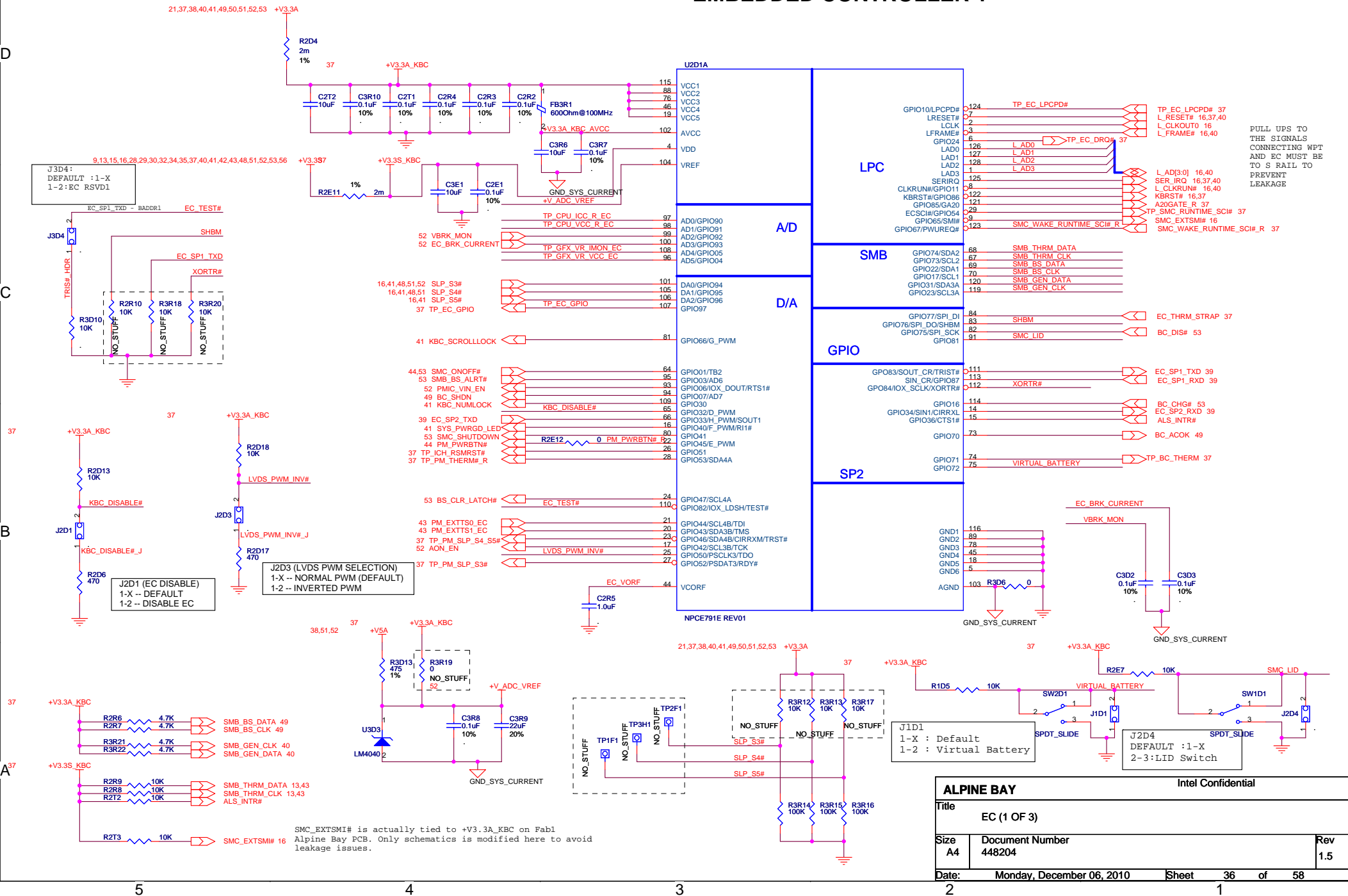
(FOR UPHAM AND MOTT CANYON ADD IN CARDS ON CRB)



To Validate WI Fi and BT modules

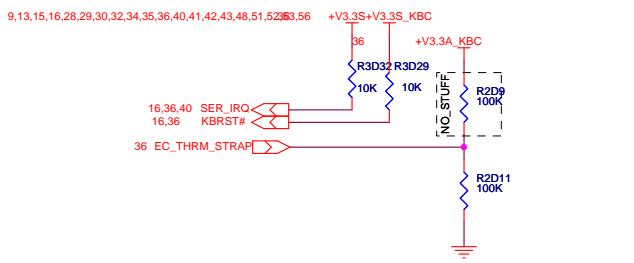
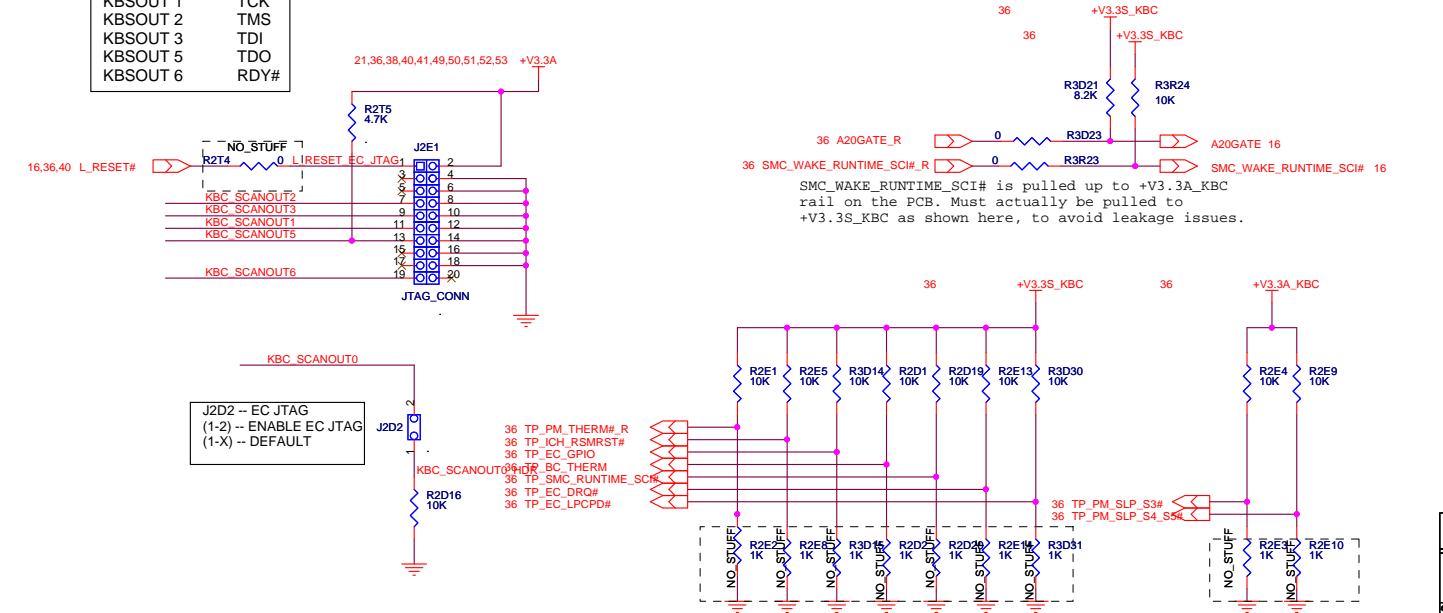
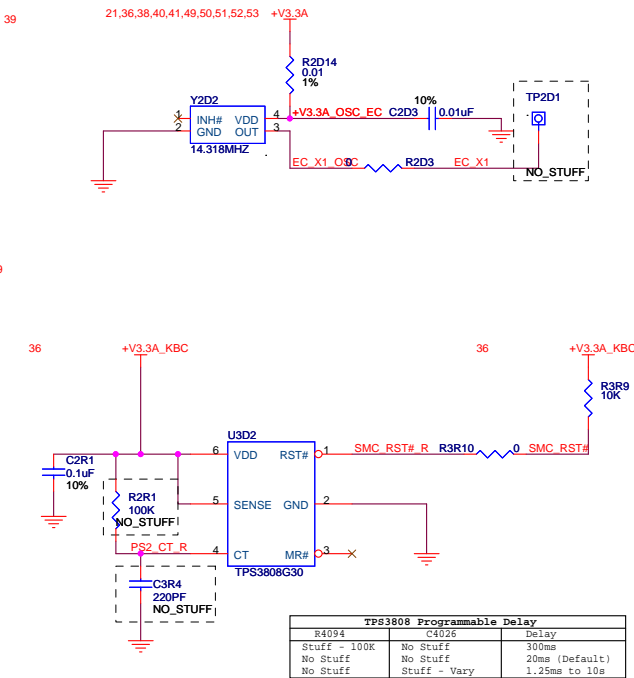
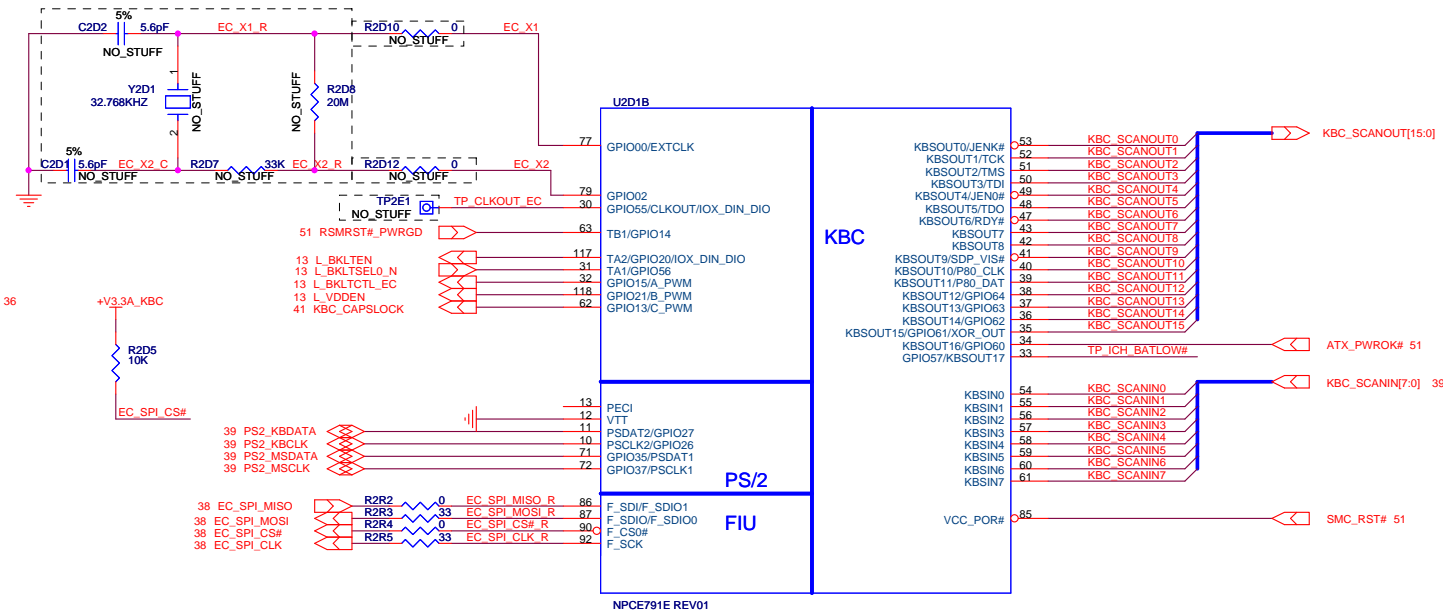


EMBEDDED CONTROLLER 1



ALPINE BAY				Intel Confidential	
Title					
EC (1 OF 3)					
Size A4	Document Number 448204				Rev 1.5
Date:	Monday, December 06, 2010		Sheet	36	of 58

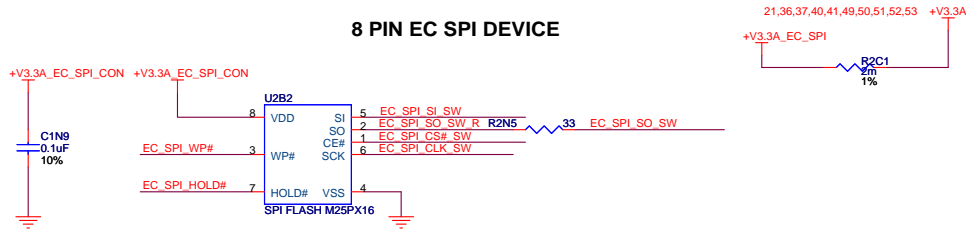
EMBEDDED CONTROLLER 2



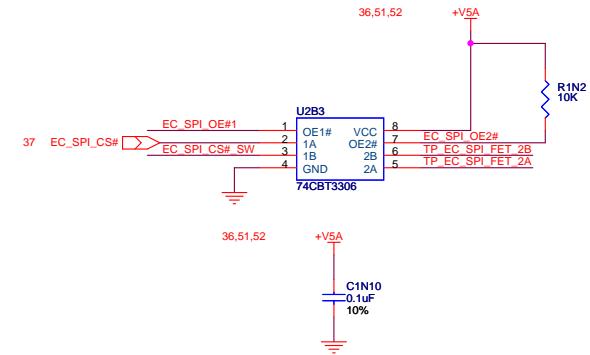
ALPINE BAY		Intel Confidential
Title		EC (2 OF 3)
Size	Document Number	Rev
A4	448204	1.5
Date:	Monday, December 06, 2010	Sheet 37 of 58

SPI DEVICE FOR EC

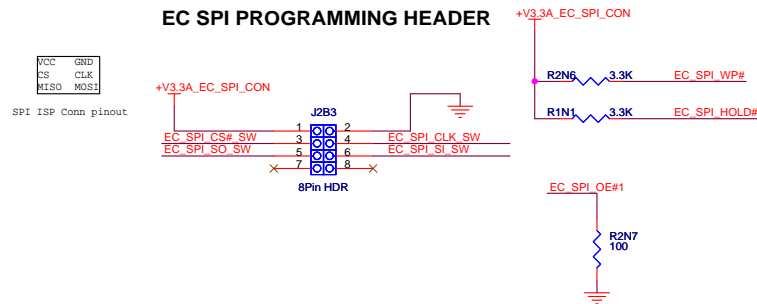
8 PIN EC SPI DEVICE



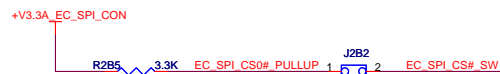
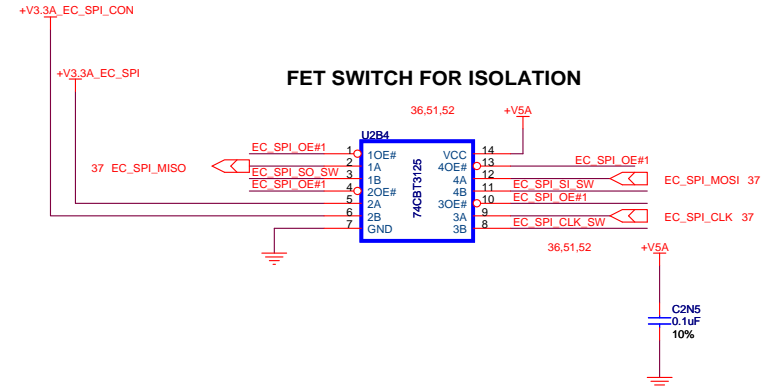
FET SWITCH FOR ISOLATION



EC SPI PROGRAMMING HEADER



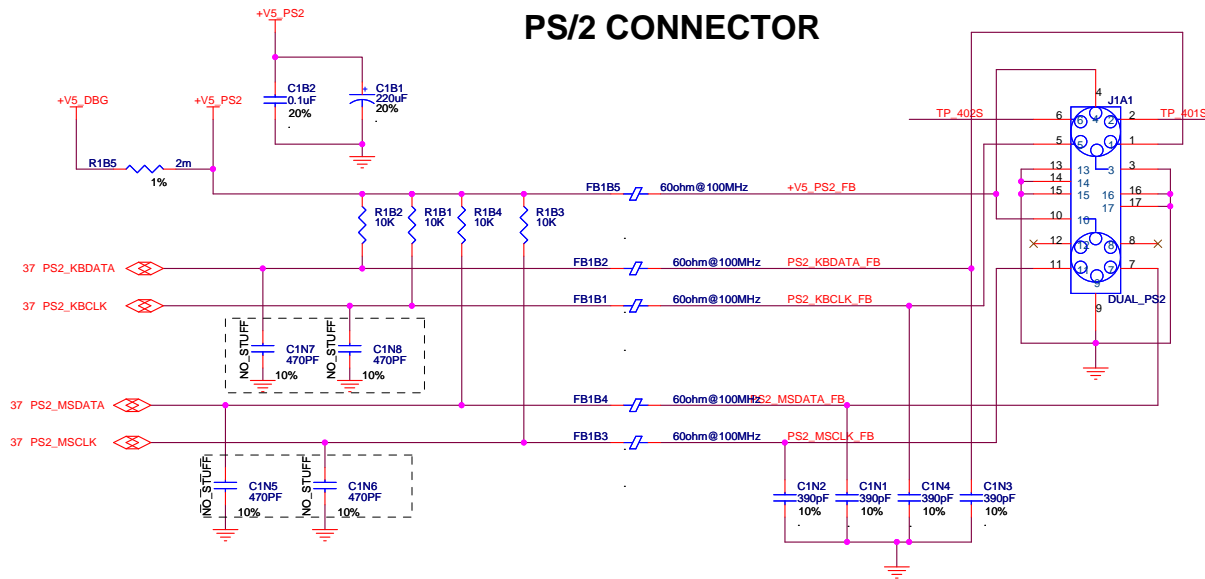
FET SWITCH FOR ISOLATION



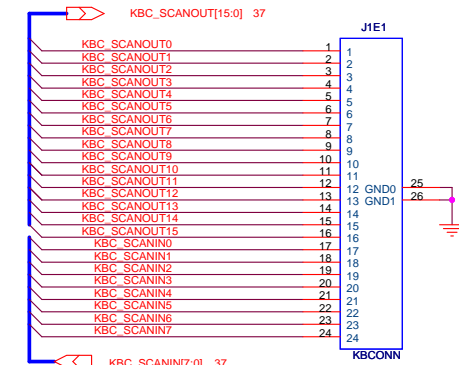
J1B2
DEFAULT :1-X
1-2:Programming EC SPI Flash

ALPINE BAY			Intel Confidential
Title			EC (3 OF 3)
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	38 of 58

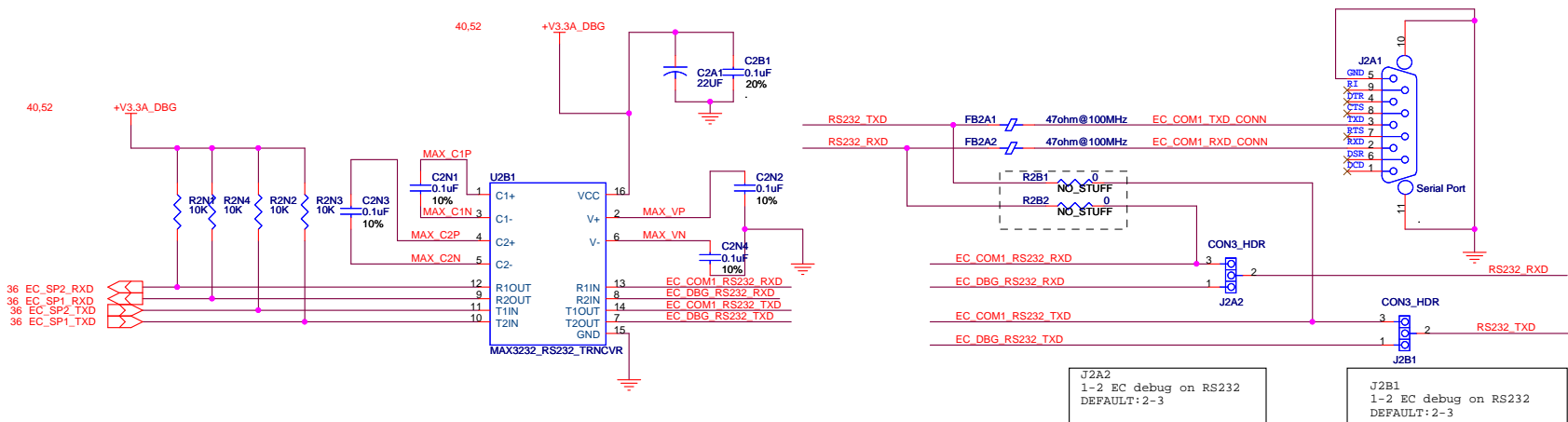
PS/2 CONNECTOR



SCAN MATRIX KEYBOARD



SERIAL PORT



J2A2
1-2 EC debug on RS232
DEFAULT: 2-3

J2B1
1-2 EC debug on RS232
DEFAULT: 2-3

ALPINE BAY			Intel Confidential
Title			LEGACY (1 OF 2)
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	39 of 58

5
4
3
2
1

8-bit I/O PORT EXPANDER

PCA9557PW Pin Connections:

- 15: PCA9557_RST#
- 16: VDD (+V3_3A)
- 8: VSS
- 1: SCL
- 2: SDA
- 3: A0
- 4: A1
- 5: A2
- 6: I/O0
- 7: I/O1
- 9: I/O2
- 10: I/O3
- 11: I/O4
- 12: I/O5
- 13: I/O6
- 14: I/O7

Board ID and Module ID Connections:

- REV_FAB_ID0
- REV_FAB_ID1
- BOARD_ID0
- BOARD_ID1
- MODULE_ID0
- MODULE_ID1

BOARD REVISION and FAB REVISION Connections:

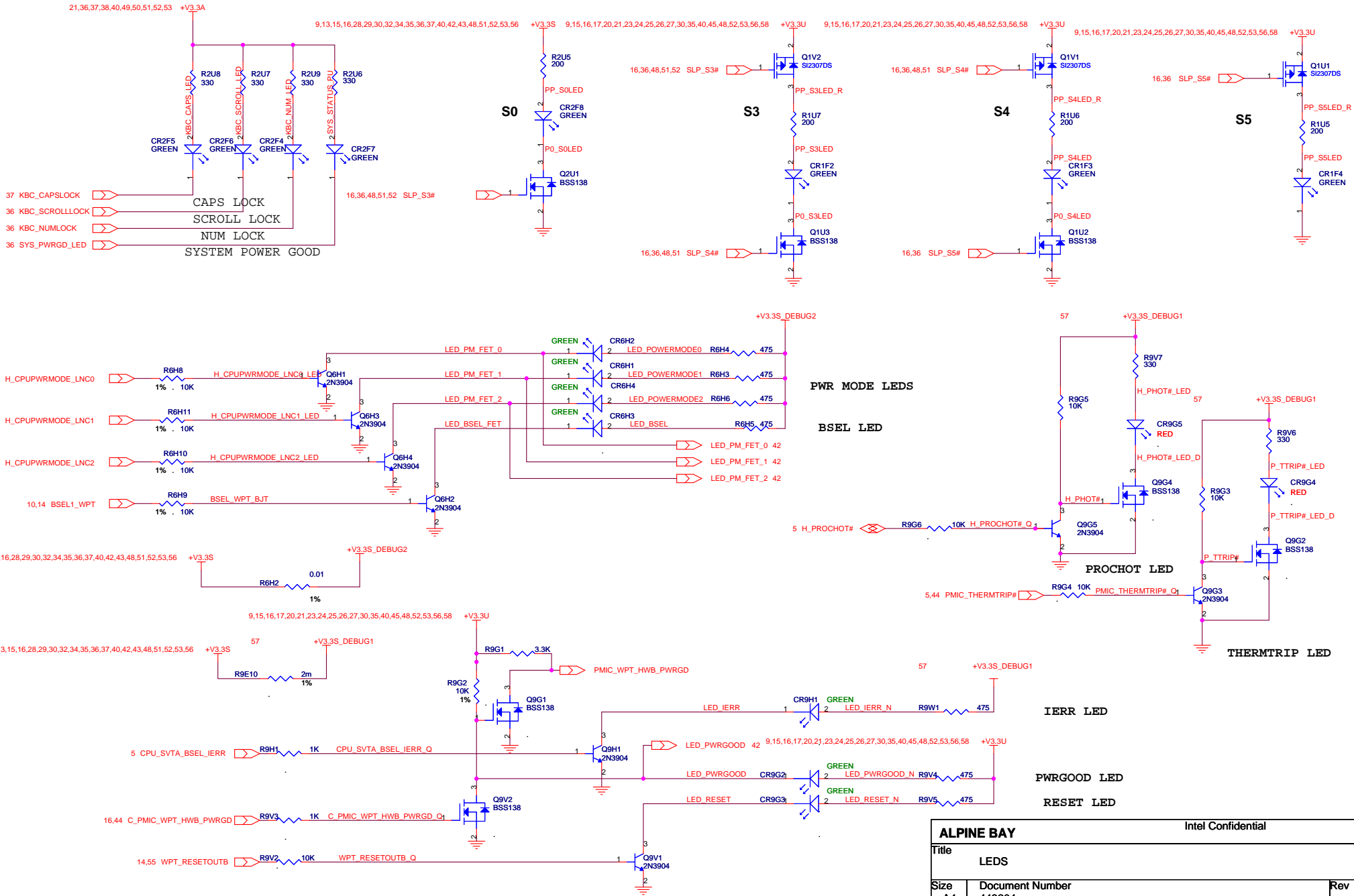
- R1G1, R1G2, R2G12, R2G9: NO_STUFF
- R1V2, R1V3, R2V6, R2V4: 10K
- +V3_3A
- GROUND

Board ID		Fab ID	
3	2	1	0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Board ID		Fab ID	
3	2	1	0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

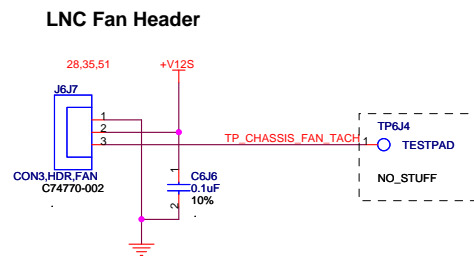
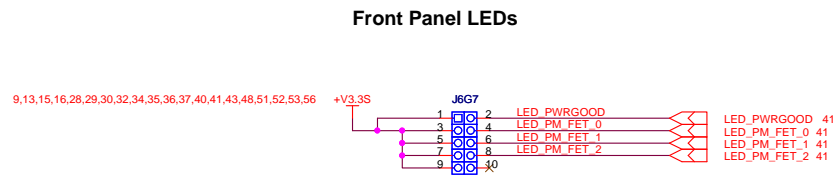
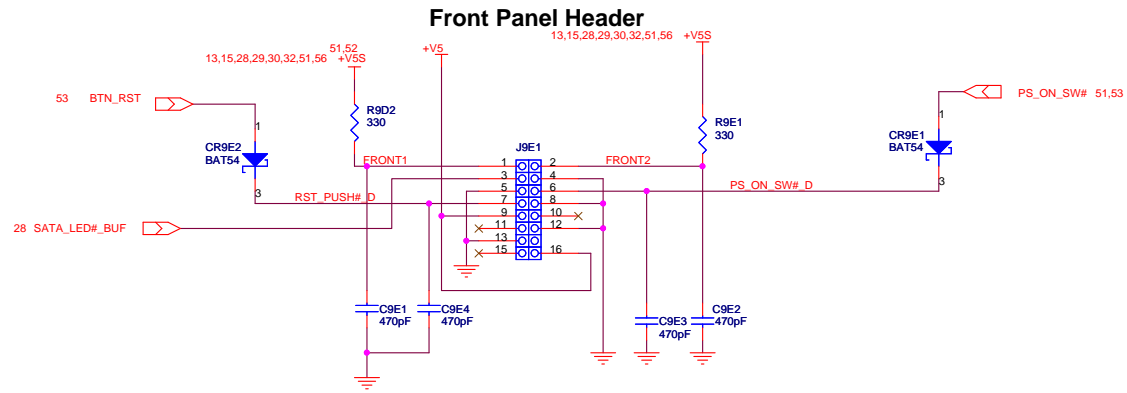
The schematic diagram illustrates the PORT 80 circuit. It features a MAX6958 driver (U1F1) connected to four 7-segment displays (CR2F1, CR2F2, CR2F3, CR1F1). The driver's inputs are connected to the SDA, SCL, and GND pins. The driver's outputs are connected to the DP, CT, COM, and SEG pins of the displays. The displays are connected to the PORT 80 pins. The circuit includes a 39.52 kHz oscillator (R1E2, C1F2, C1F3, C1F1) and a 3.3V supply (V3_3A_PORT80, V3_3S_DBG). The displays are labeled LED SEG0 through LED SEG9.

LEDs



ALPINE BAY			Intel Confidential
Title		LEDs	
Size	A4	Document Number	448204
Date:	Monday, December 06, 2010		Rev 1.5
Sheet	41	of	58

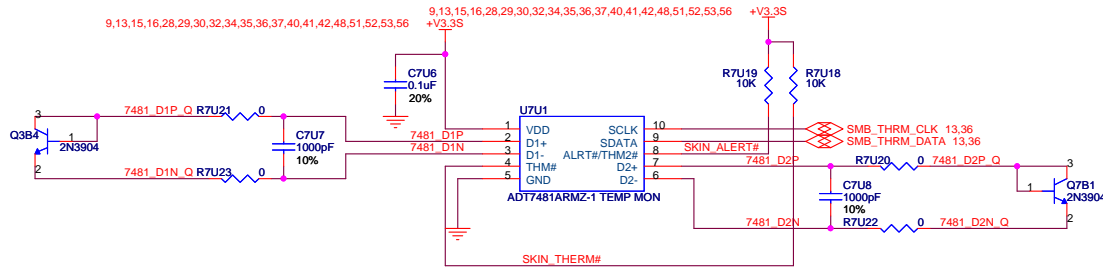
MISCELLANEOUS



ALPINE BAY			Intel Confidential
Title			MISC
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	42 of 58

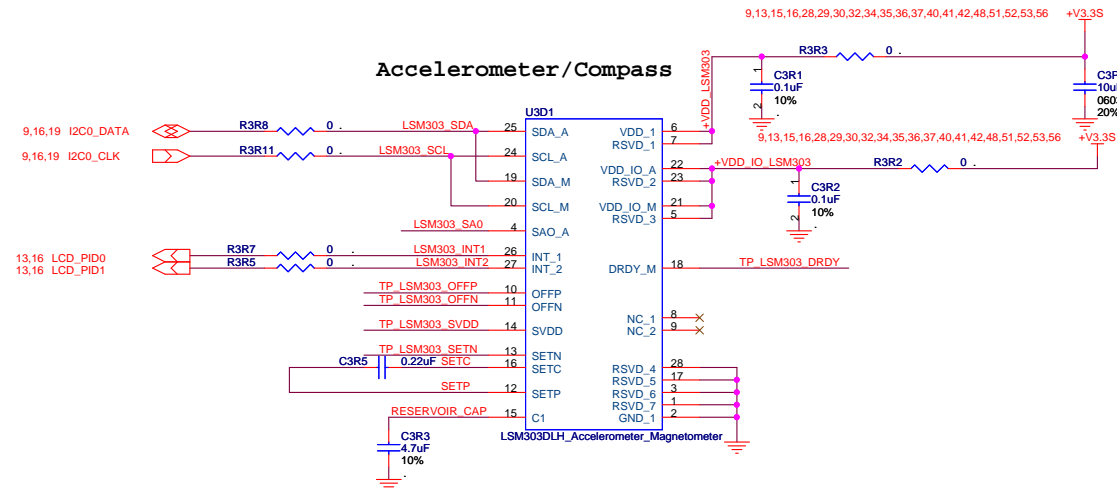
SENSORS

SKIN TEMPERATURE SENSOR



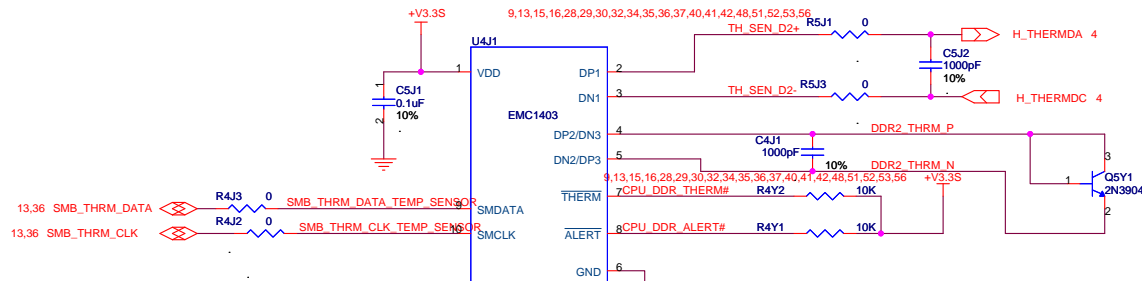
Address: 0x4B

Accelerometer/Compass



Address: 0x18

Lincroft Thermal Sensor



Address: 0x4C

CAD NOTE: PLACE THE DDR2 THERMAL SENSOR NEAR DDR2

ALPINE BAY			Intel Confidential
Title			SENSORS
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	43 of 58

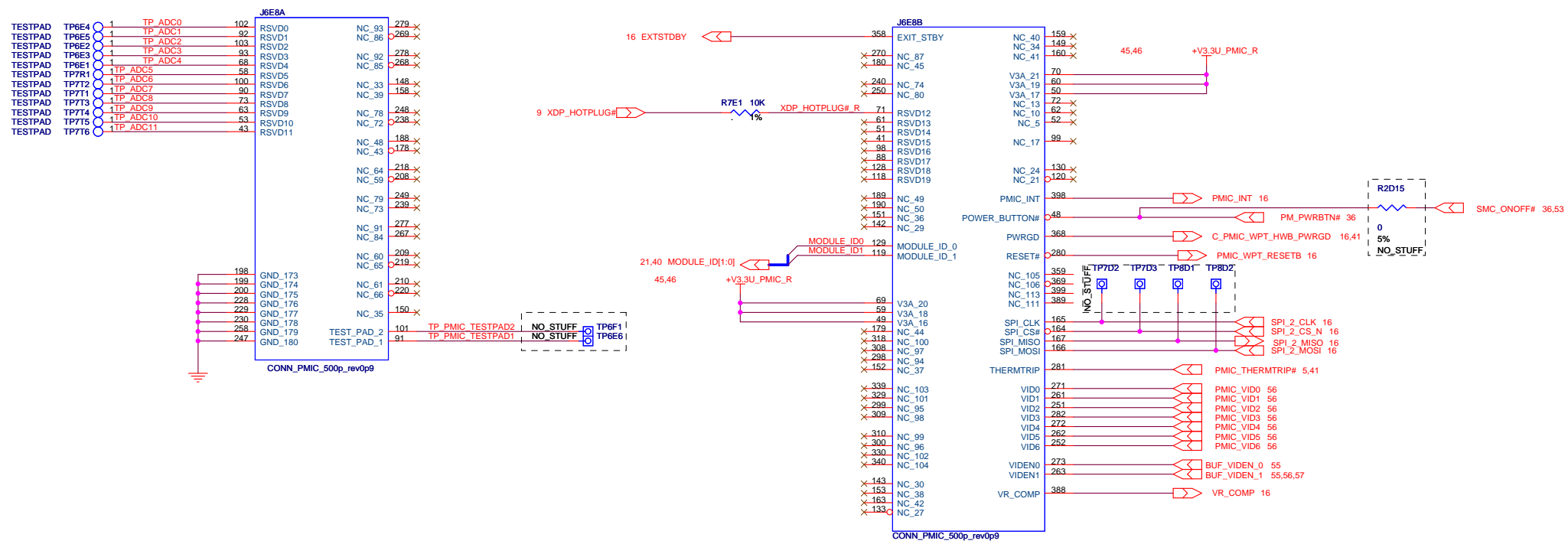
PMIC (1 OF 4)

D

C

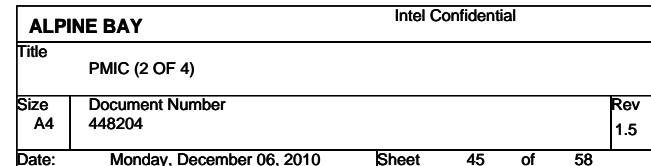
B

A

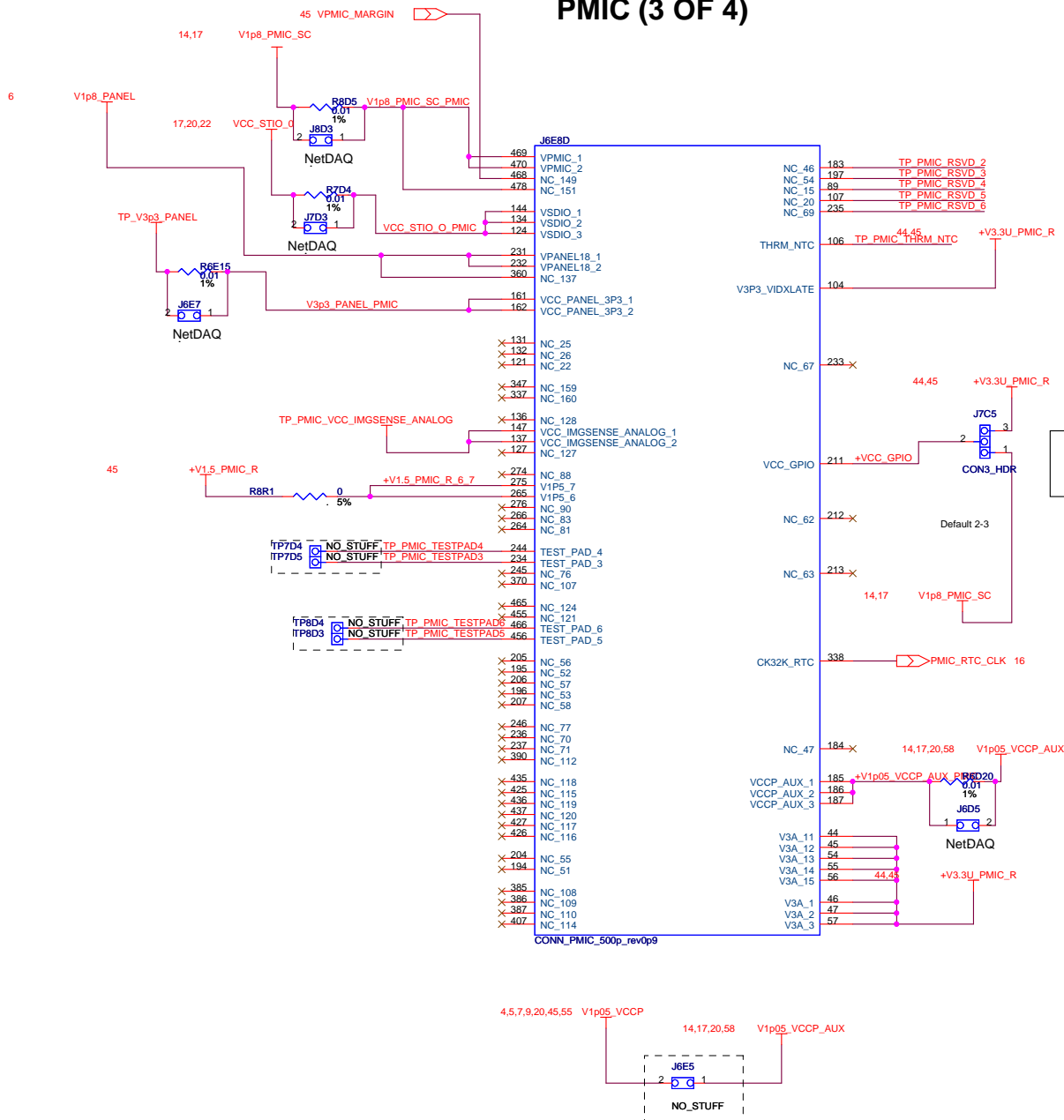


ALPINE BAY			Intel Confidential
Title			
PMIC (1 OF 4)			
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010	Sheet	44 of 58

5



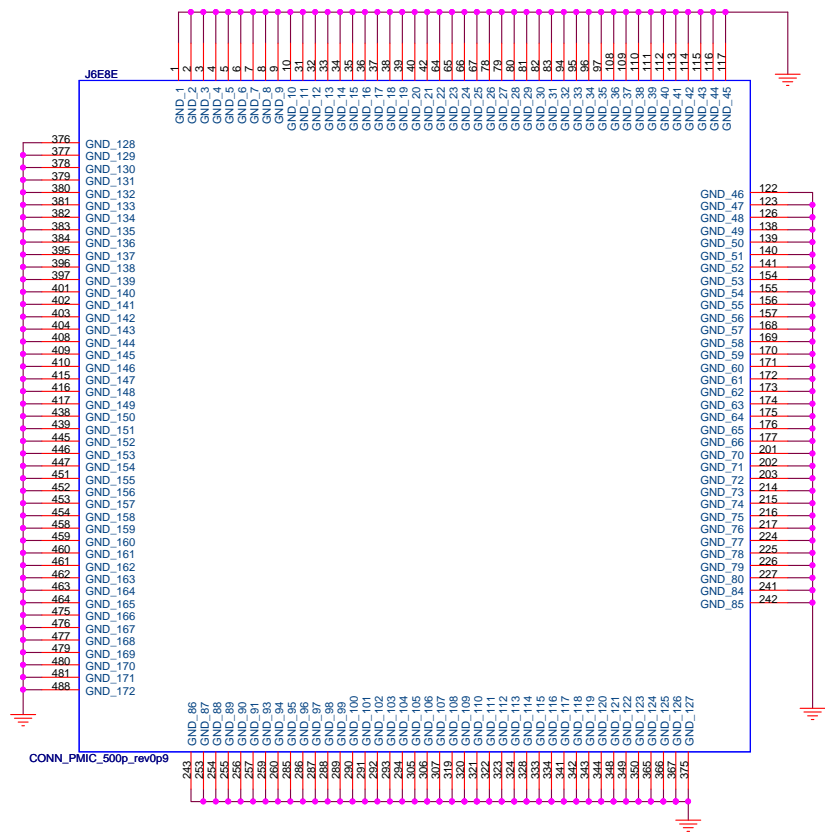
PMIC (3 OF 4)



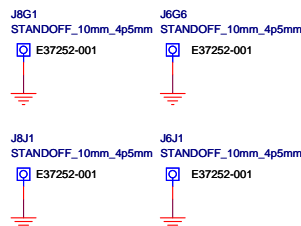
J7C5	2-3	3.3 V
DEFAULT	1-2	1.8 V

ALPINE BAY		Intel Confidential
Title		
PMIC (3 OF 4)		
Size	Document Number	Rev
A4	448204	1.5
Date:	Monday, December 06, 2010	Sheet 46 of 58

PMIC (4 OF 4)



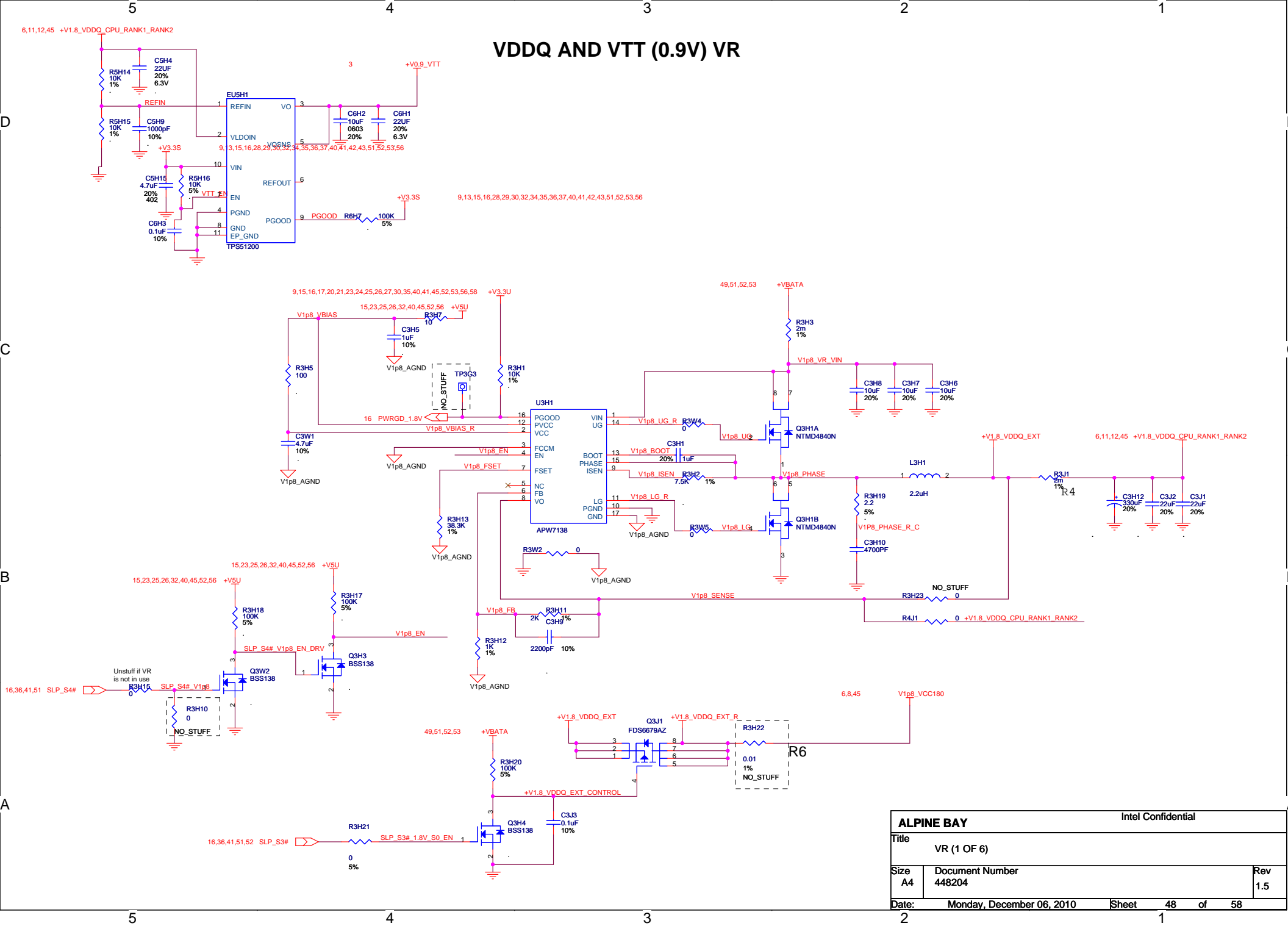
Mounting Holes for PMIC module



BOM Note: Manually add one screw for each standoff to BOM. E38917-001 (M2.5x0.45)

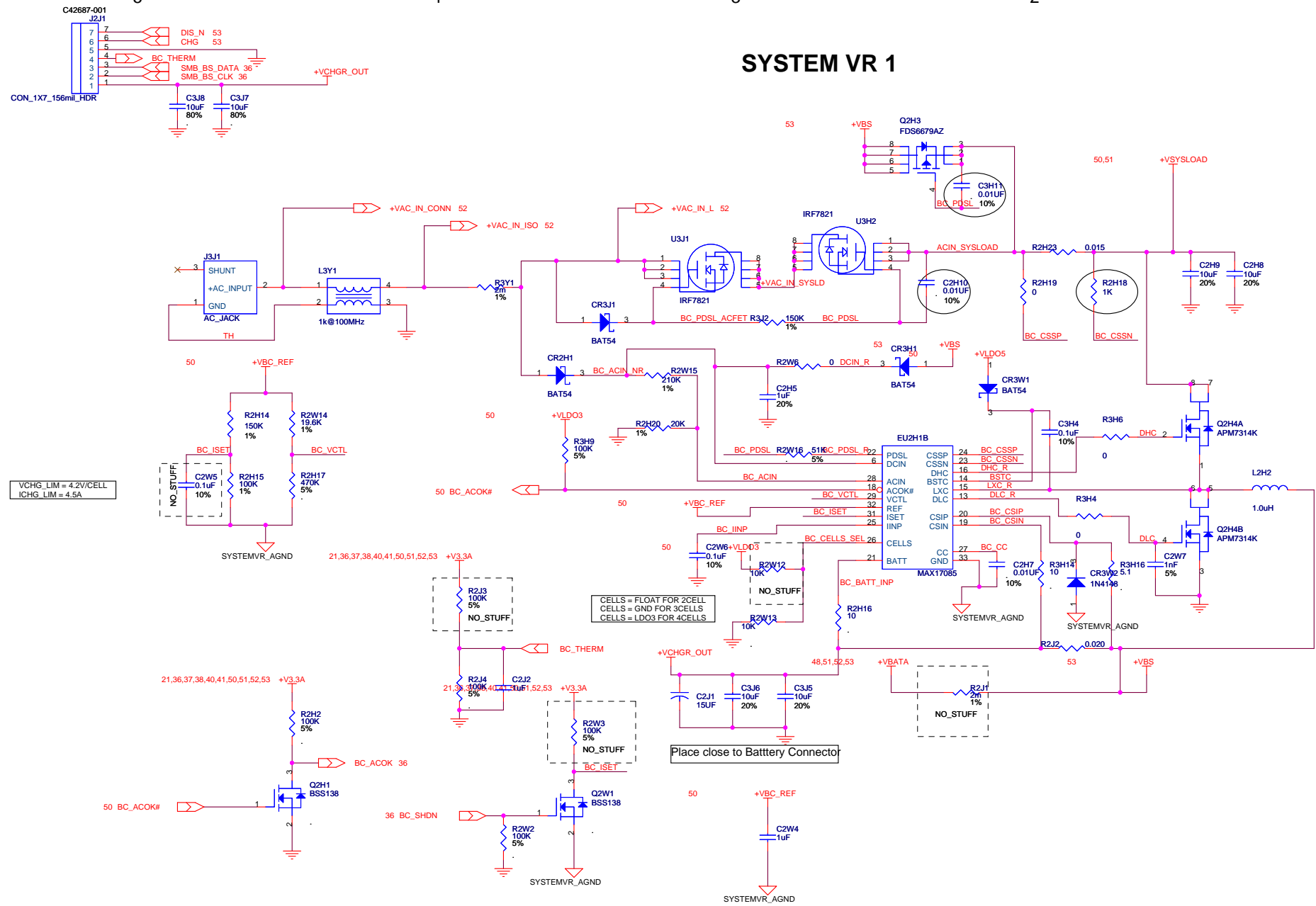
ALPINE BAY		Intel Confidential	
Title		PMIC (4 OF 4)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	47 of 58

VDDQ AND VTT (0.9V) VR



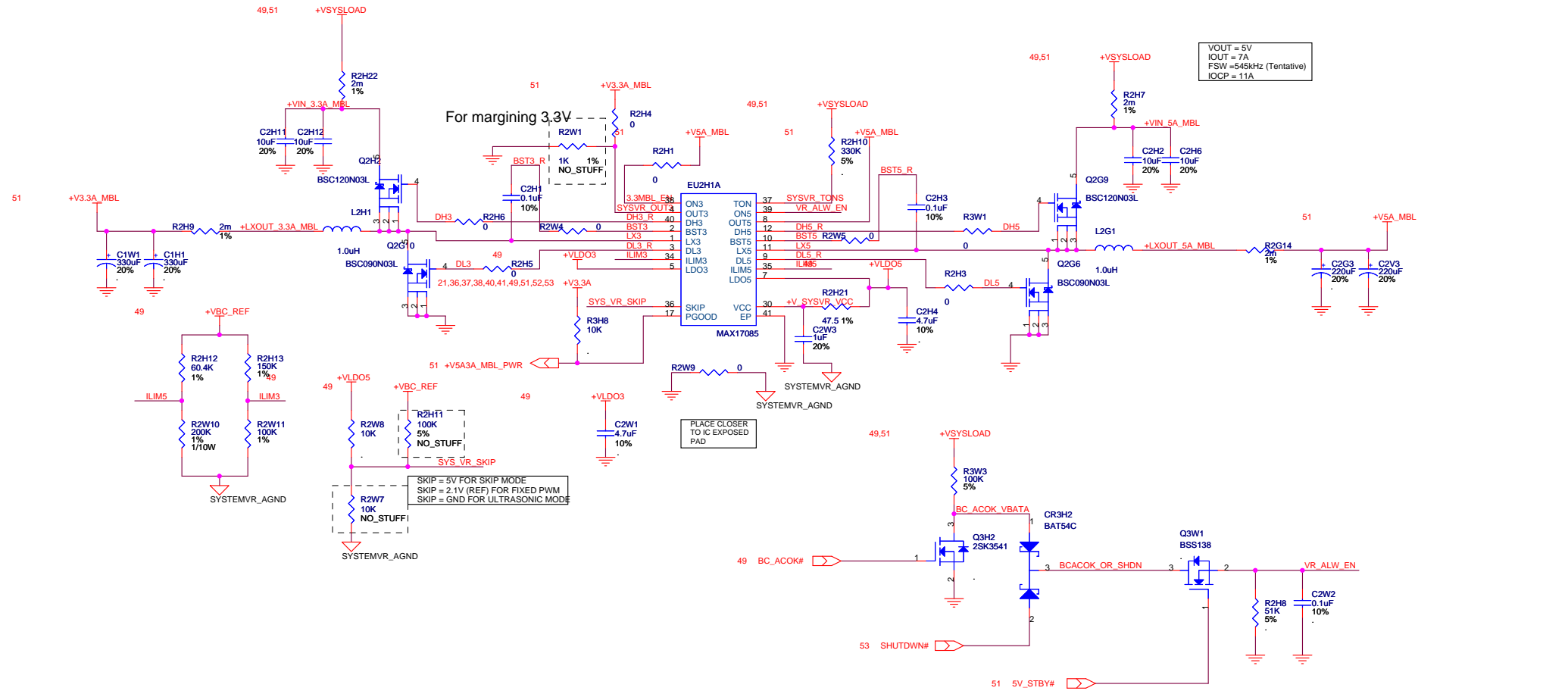
ALPINE BAY			Intel Confidential
Title		VR (1 OF 6)	
Size	A4	Document Number	448204
Date:	Monday, December 06, 2010	Sheet	48 of 58
		Rev	1.5

SYSTEM VR 1



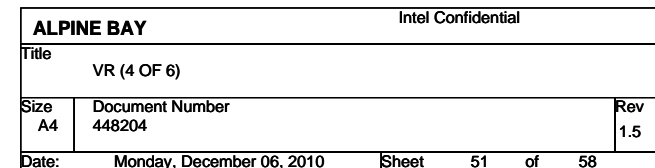
ALPINE BAY				Intel Confidential	
Title VR (2 OF 6)					
Size A4	Document Number 448204				Rev 1.5
Date:	Monday, December 06, 2010		Sheet	49	of 58

SYSTEM VR 2



ALPINE BAY			Intel Confidential
Title			VR (3 OF 6)
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010		Sheet 50 of 58

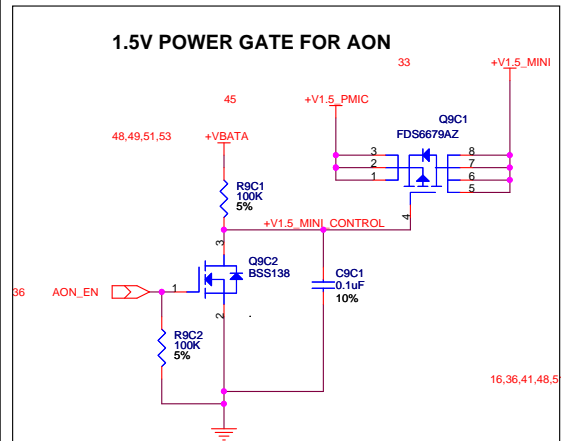
1



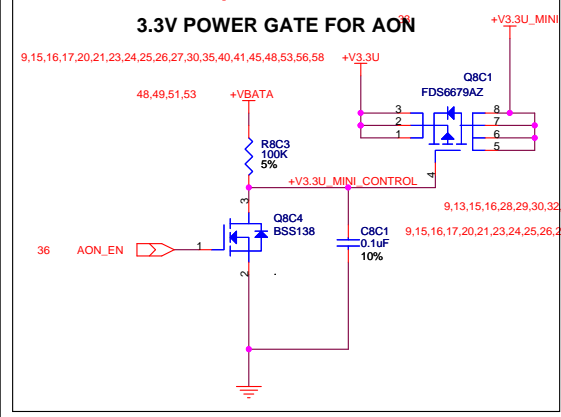
MISCELLANEOUS VR

VR FOR HD AUDIO 1.5V POWER GATE FOR HD AUDIO

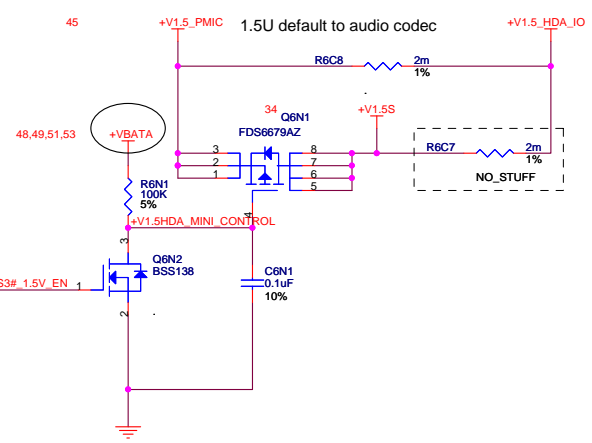
1.5V POWER GATE FOR AON



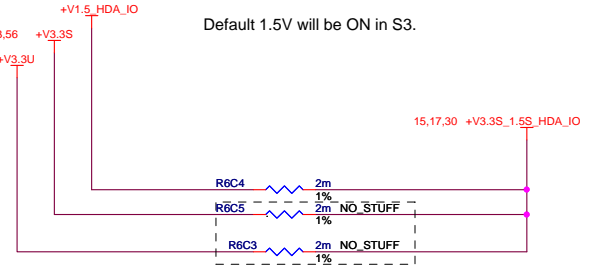
3.3V POWER GATE FOR AON



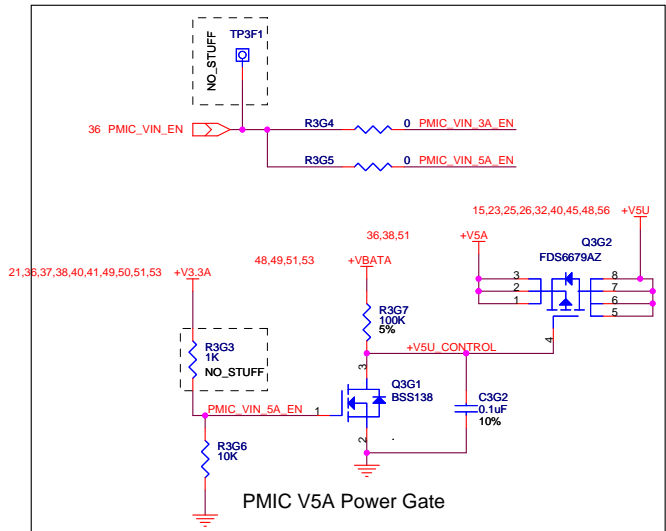
1.5U default to audio codec



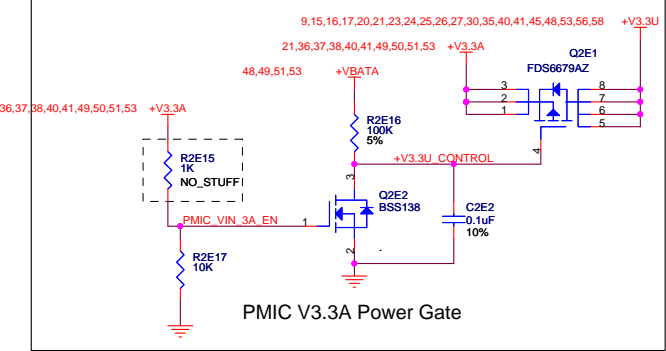
Default 1.5V will be ON in S3.



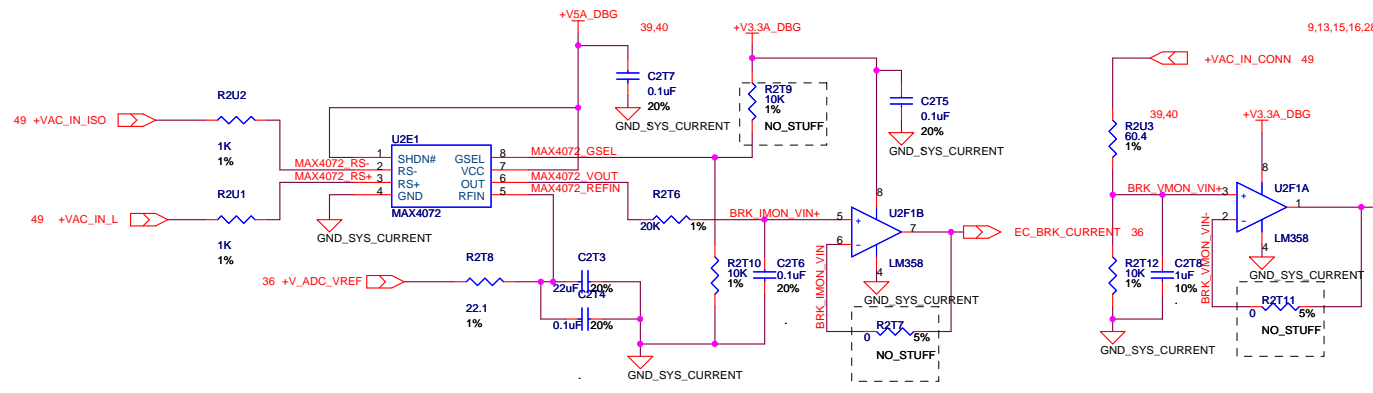
PMIC V5A Power Gate



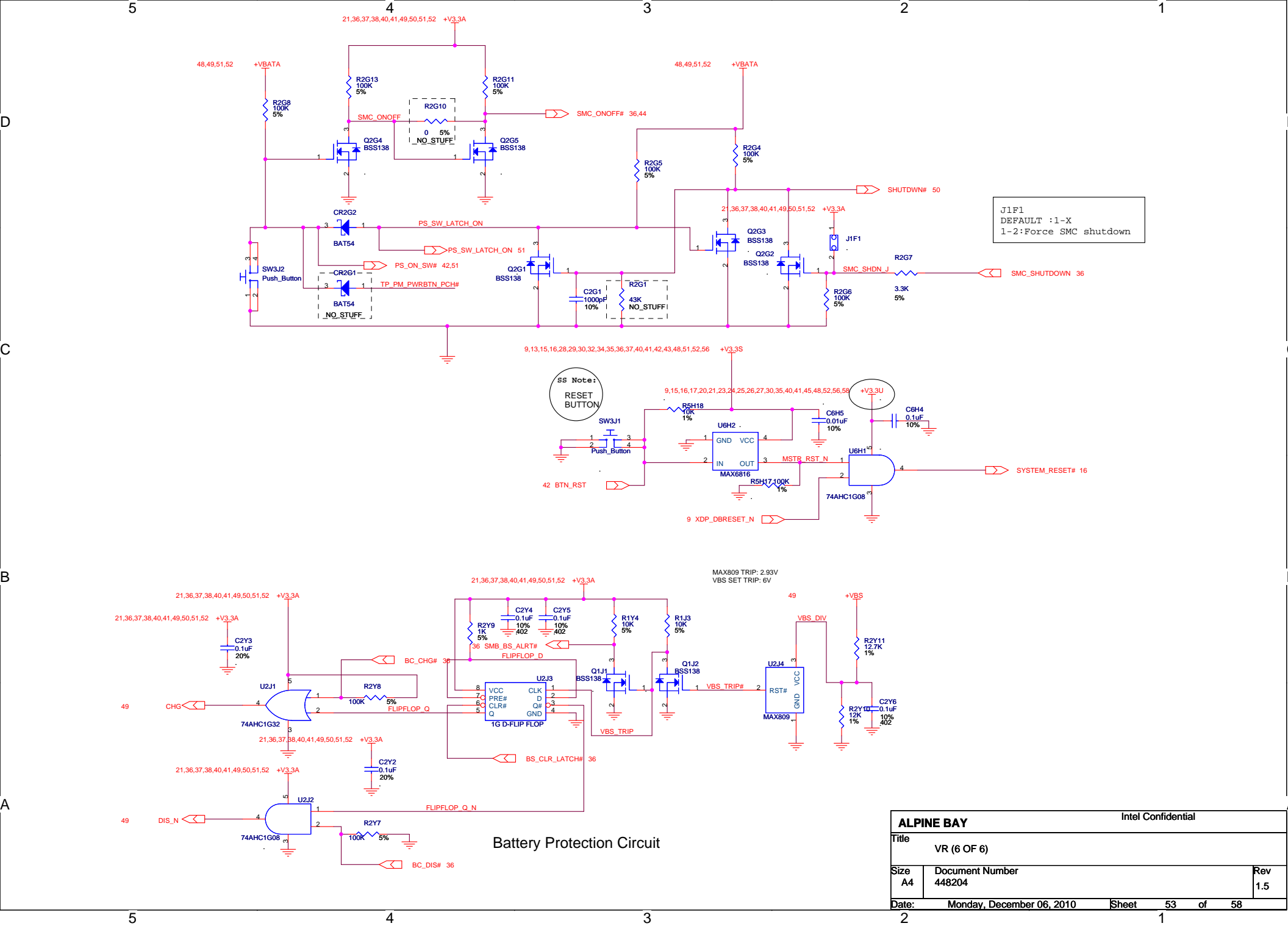
PMIC V3.3A Power Gate



Battery Charge Voltage & Current Monitor

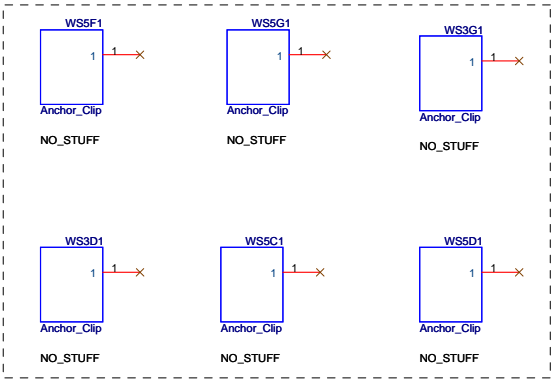
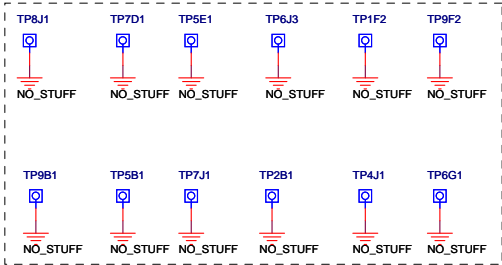


ALPINE BAY			Intel Confidential
Title			VR (5 OF 6)
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	52 of 58

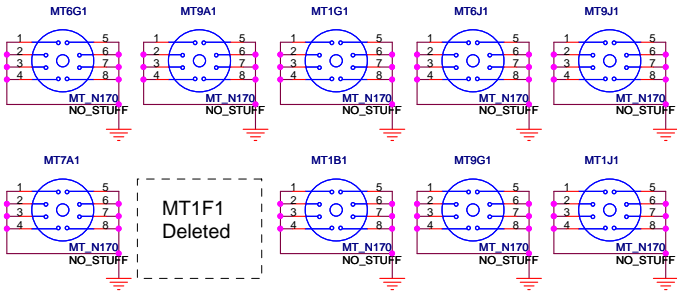


MOUNTING HOLES

Anchors for LNC/WPT (3ea / MPI skt)



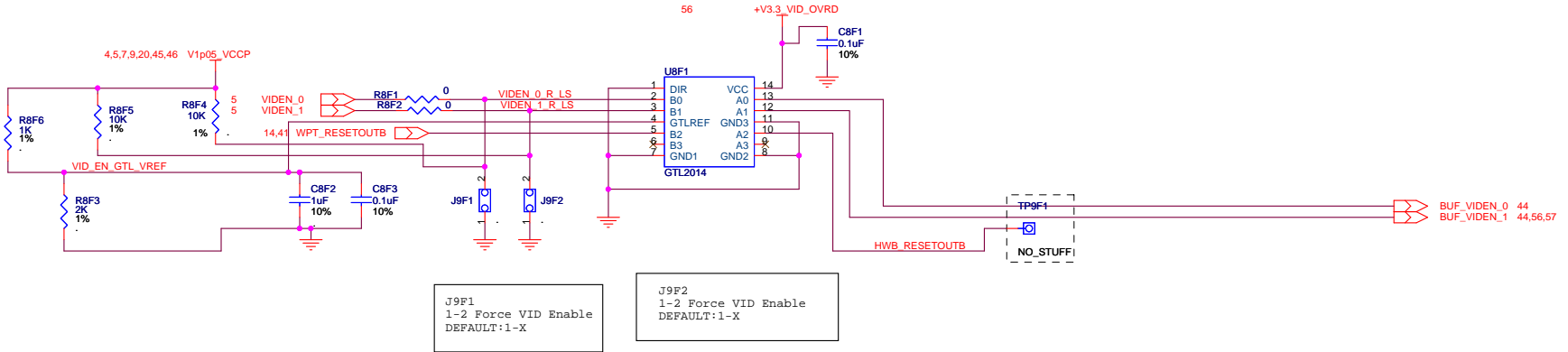
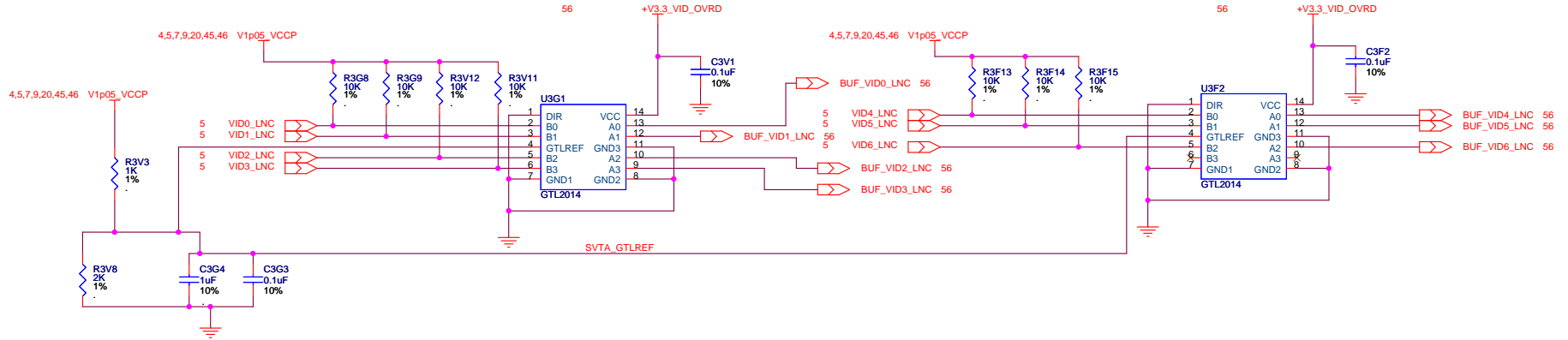
Mounting holes for the PCB to chassis



ALPINE BAY			Intel Confidential	
Title				
MOUNTING HOLES				
Size	Document Number			Rev
A4	448204			1.5
Date:	Monday, December 06, 2010		Sheet	54 of 58

VID LEVEL SHIFTER

USED FOR MANUAL VID IMPLEMENTATION. NOT REQUIRED FOR ONE-TO-ONE CONNECTION BETWEEN PMIC AND LINCROFT



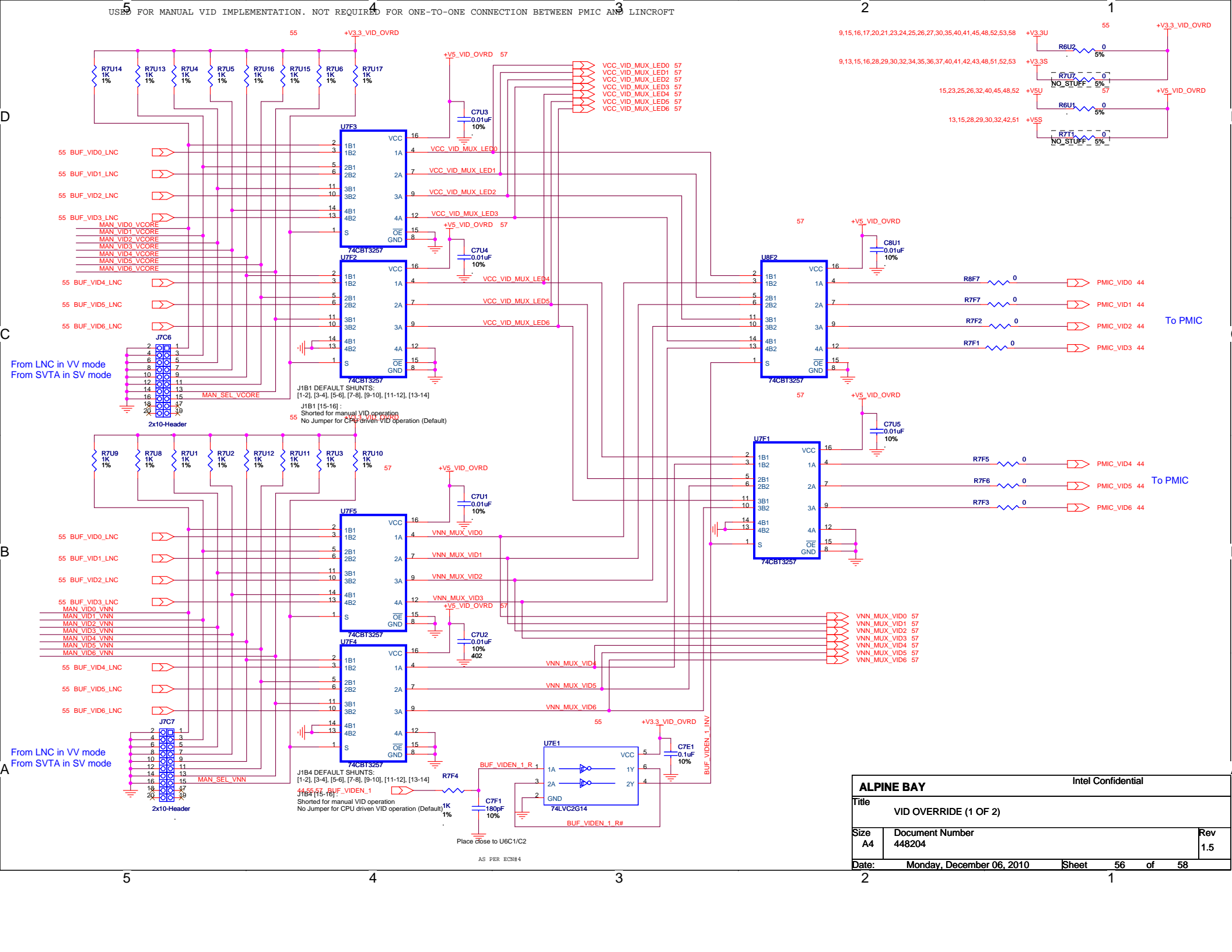
ALPINE BAY			Intel Confidential
Title			
VID LEVEL SHIFTER			
Size	Document Number		Rev
A4	448204		1.5
Date:	Monday, December 06, 2010		Sheet 55 of 58

D

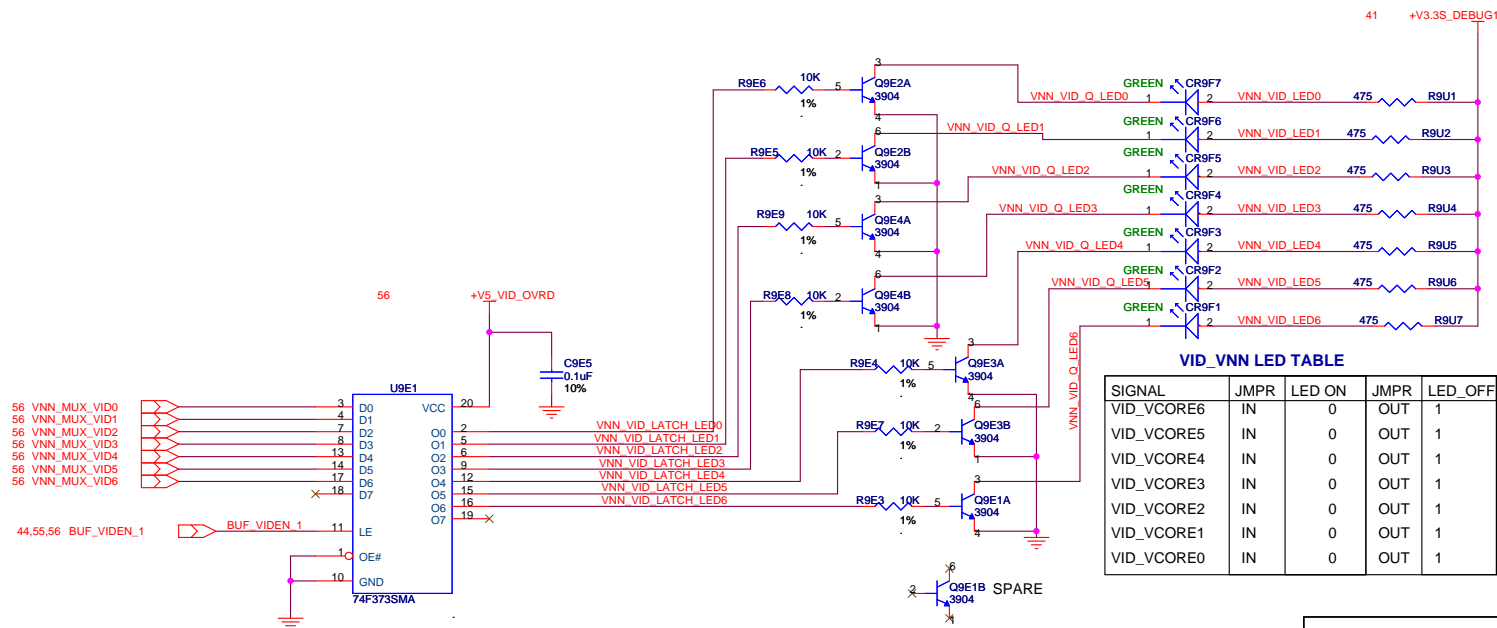
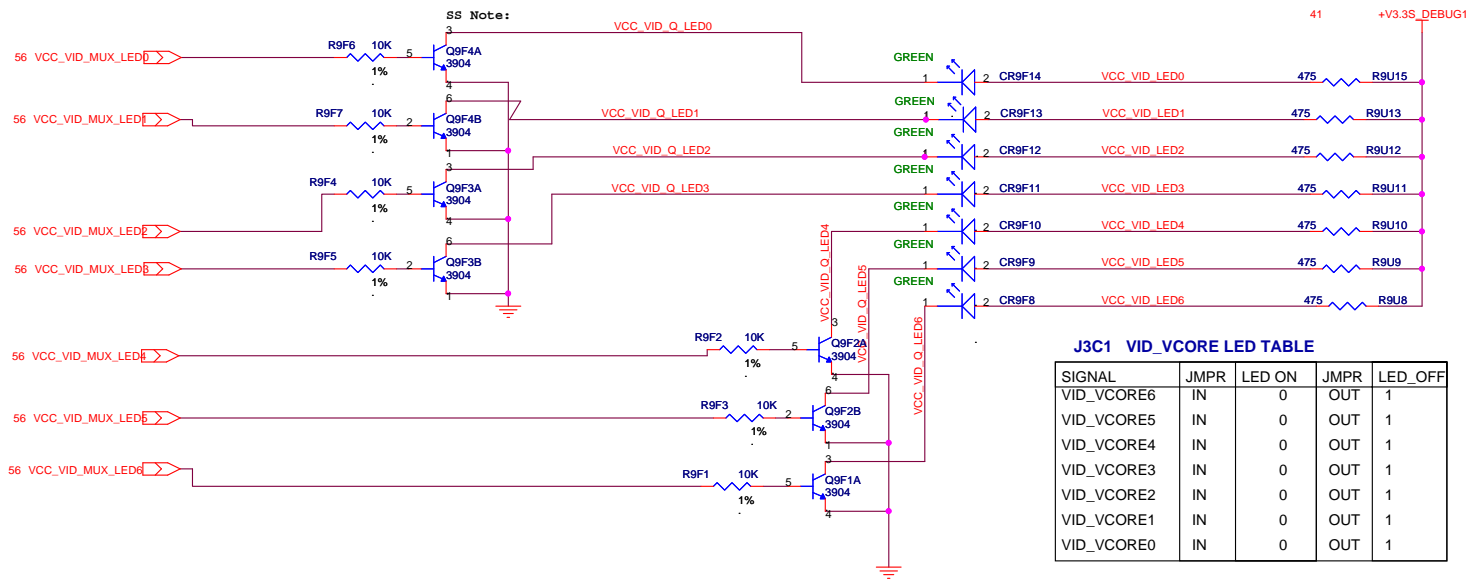
C

B

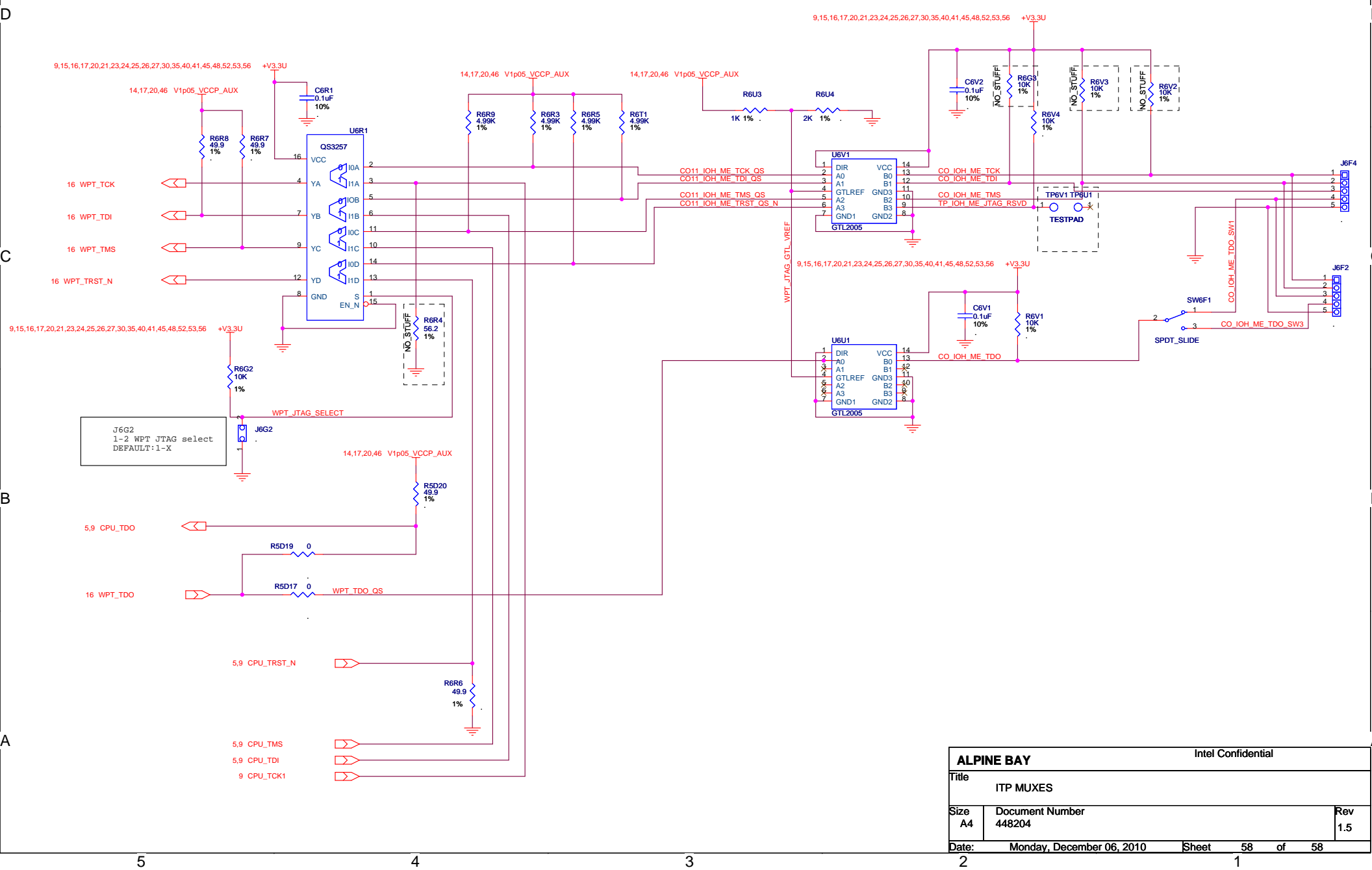
A



ALPINE BAY			Intel Confidential
Title		VID OVERRIDE (1 OF 2)	
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	56 of 58



ITP MUXES



ALPINE BAY			Intel Confidential
Title			ITP MUXES
Size	Document Number	Rev	
A4	448204	1.5	
Date:	Monday, December 06, 2010	Sheet	58 of 58