Design Of Sample and Hold Merged With 2.5 Bit Multiplying Digital-to-Analog Converter

Xiao-lei Wang, Chang Liang, Xian-zhong Guan, Hong-hui Deng
Institute of VLSI Design
Hefei University of Technology
Hefei, China
changliang87@hfut.edu.cn

***Abstract*—A design of a SHA merged with MDAC(SMDAC) which can be used in a 14 bit 80Msps pipelined analog-to-digital converter (ADC) is presented in this paper. A two-stage transconductance-controlled op-amp is used in the SMDAC to ensure the requirment of the resolution, speed and stability of the circuit when its feedback factor alternate between 1/2 and 1/4. Simulation by cadence based on Chartered 0.18μ 1P5M CMOS process under 1.8V supply voltage shows 116dB loop gain, 1.05GHz unity gain bandwidth and 61° phase margin in two different feedback factors of the op-amp. The output signal of the S/H phase and MDAC phase can be settled to 14bit and 12bit accuracy in 5ns, respectively.**

Keywords-SMDAC; op-sharing; transconductance-controlled

I. INTRODUCTION

With the recent development of portable devices especially in video and wireless devices, low power high resolution analog-to-digital converter (ADC) is exigent. Moreover, pipelined ADC can achieve good compromise between speed, power and resolution, it has become the mainstream of the research. Recently further power saving has been achieved by sharing op-amp between S/H and the first MDAC [1]. While the SMDAC merging the S/H with the first MDAC successfully reduces power consumption, it has two drawbacks. First, because the op-amp has to work continuously in S/H phase and MDAC phase, the input node never reset and every working phase of the op-amp will be affected by the error voltage stored on the capacitor to the previous phase. We call it memory effect [2]. The problem can be partly solved by adding an extra input differential pair [3]. However, this augment will increase the chip area and complexity of the clock circuit. The second drawback is caused by feedback factor. The factor of the S/H will no more than 1/2 to achieve unity gain and the first stage generally greater than 1/4 as multi-bit MDAC is usually used in the first stage of the pipelined ADC to reduce resolution requirement of the following stages [4]. Under this circumstance the op-amp which is shared in the SMDAC can hardly work under appropriate unity-gain or phase margin when it is alternated between two different feedback factors.

This work solves these problems by using a transconductance-controlled op-amp with a short discharge phase in the SMDAC. The proposed op-amp provides a constant overdrive voltage of the input pair which can make further improvement on the performance. Thus, the SMDAC achieves low-power operation without sacrificing speed and stability, which can be used in 14 bit 80MS/s pipelined ADC.

II. 2.5BIT SMDAC

The function of a sample-and-hold (S/H), a multiplying digital-to-analog converter (MDAC) for first stage and a discharge for eliminating memory effect [2] should be merged in the proposed SMDAC. Figure 1 show the SMDAC architecture including working clocking phase.

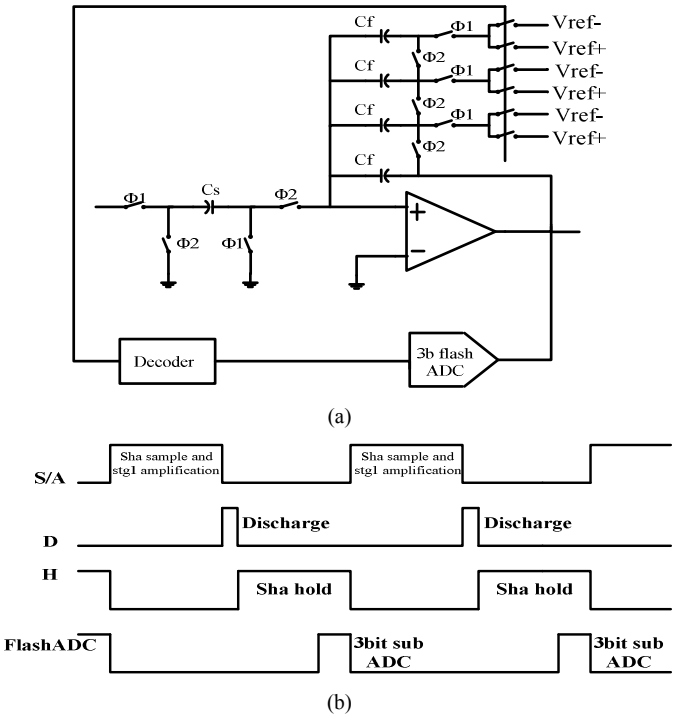

Figure 1. (a) The architecture of SMDAC (b) The clock phase of SMDAC

Two main working phases and a discharge phase are shown in Figure1 (b). During the sample and amplifier(S/A) phase, the switch Φ1 is closed and the input is sampled on the sampling capacitor Cs, the op-amp is working for the first MDAC. While the input sample is held on Cs, the input nodes

of op-amp and feedback capacitor C_f are reset to AC ground in discharge phase. Then, in the holding phase, the switch Φ2 is closed and the op-amp is working for holding the input signal which was sampled on Cs in S/A phase. The closed loop character is settled to unity gain by making $Cs=4C_f$.

The resolution of the first MDAC should be carefully selected to fit the power, speed and resolution of the ADC. High resolution of the first stage can decrease resolution requirement of the following stages in which size of circuits and power consumption can be scaled down [4]. However, higher resolution MDAC has a large feedback factor which needs higher open-loop gain and unity-gain bandwidth of the op-amp. It can also increase the design complex of the shared op-amp. A 2.5bit MDAC is used in this SMDAC overall evaluating these factors, and the rest of the pipeline stages consist of five 1.5 bit op-sharing stages.

Figure 2 shows the residue curve of 2.5-bit MDAC in which no overflow detection is used and the input range will be reduced from ±Vref to ±7/8Vref.

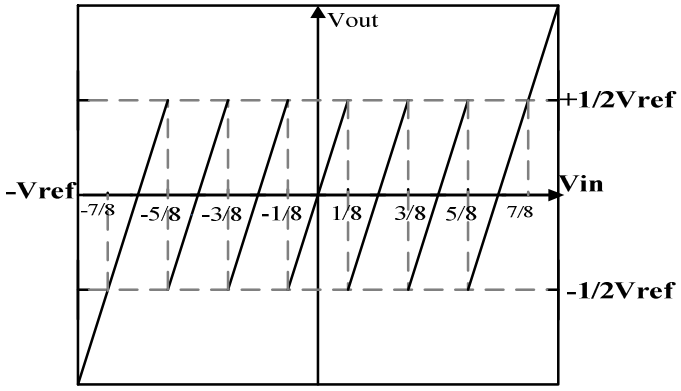

Figure 2. Residue curve of 2.5bit MDAC

When input signal amplitude is higher than +7/8Vref or lower than -7/8Vref, the digital code of ADC will overflow and the circuit can't give any respond to reflect it. Thus, the input signal of ADC should be avoided to exceed ±7/8Vref. While input signal in the range between ±7/8Vref, transfer function of the 2.5-bit MDAC is expressed as

$$Vout=\begin{cases} 4Vin-3Vref & 5/8Vref \le Vin \le 7/8Vref \\ 4Vin-2Vref & 3/8Vref \le Vin < 5/8Vref \\ 4Vin-Vref & 1/8Vref \le Vin < 3/8Vref \\ 4Vin & -1/8Vref \le Vin < 1/8Vref \\ 4Vin+Vref & -3/8Vref \le Vin < -1/8Vref \\ 4Vin+2Vref & -5/8Vref \le Vin < -3/8Vref \\ 4Vin+3Vref & -7/8Vref \le Vin < -5/8Vref \end{cases}$$

In this case, the entire residue distributes between ±1/2Vref which can be connected with following stages directly.

III. CIRCUIT IMPLEMENTATIONS

A. Circuit of 2.5bit SMDAC

Figure 3 shows the equivalent circuit of SMDAC at each working phase.

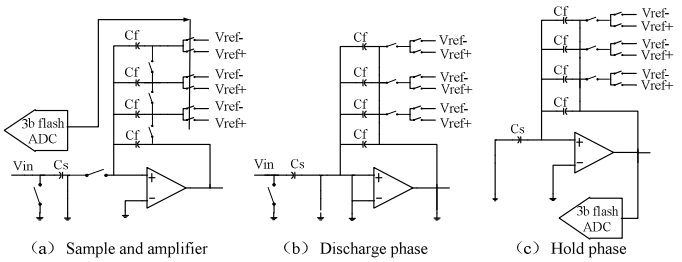

Figure 3. SMDAC configurations at each phase

During S/A phase, the sample capacitor Cs and feedback capacitor C_f is disconnected by switch between them. As a result, the sample process and amplification process can work independently, as shown in (a). At the end of this phase, the input and output node of the op-amp and C_f is connected to Vcm (which can be recognized as AC ground) to discharge. At this time, the total charge is shown as (1)

$$Q_{total}=(Vin-Vcm)\times Cs \tag{1}$$

After the discharge phase, the input voltage stored on Cs is transferred to four C_f's, the output of the op-amp is holding the input signal and the 3b flash ADC make a decision after the op-amp is settled in$1/2LSB_{14}$. Since the input node of the op-amp can be seen as AC ground approximately, and the total charge conserved at both phase is invariable, as in (2) to (4)

$$Q_{total}{}'=(Vout-Vcm)\times 4C_f \tag{2}$$

$$Q_{total}=Q_{total}{}' \tag{3}$$

$$Cs=4Cf \tag{4}$$

The transfer function is shown in (5) based on (1) to (4)

$$V_{out}=V_{in} \tag{5}$$

When the circuit transferred from hold phase to S/A phase, $Q_{total}{}'$ on $4C_f$ transferred to only one C_f and the output voltage is shown like (6)

$$Vout'=4Vin-D\times Vref \quad (D=0,\pm1,\pm2,\pm3) \tag{6}$$

The number of D is fixed by the digital code from flash ADC in holding phase. The sample and feedback capacitor is settled to 6pF and 1.5pF respectively to fit the requirement of noise, speed and power consumption.

Two important facts need to be noted in the SMDAC operation. First, the discharge phase should be more than 30% of the holding phase, as the result, the holding phase of S/H is about 30% shorter than that of the traditional S/H [5].

However, since the op-amp does not have to drive sampling capacitors of the following stage in the hold phase, the total op-amp load in the holding phase is decreased about 50% compared to the conventional S/H, which allows the SMDAC to settle faster to the required accuracy without increasing power. The second important fact is the phase margin and unity-gain-bandwidth of the op-amp when the feedback factor alternate between 1/2 and 1/4. It can be solved by the method below.

B. Circuit of transconductance-controlled op-amp

The proposed op-amp is used for the S/H and 2.5 bit first MDAC in a 14 bit 80MS/s pipelined ADC, thus the output signal must be settled in the resolution of residual level within 5ns. Total error brought by finite DC gain and finite bandwidth of the op-amp should be less than both $1/2LSB_{14}$ in the holding phase and $1/2LSB_{12}$ in the S/A phase. So the loop gain of the op-amp must be more than 100dB and unity-gain-bandwidth must be more than 800MHz. 60° phase margin is required to ensure a quick and stable settling. Figure 4 shows the input transconductance-controlled op-amp for the SMDAC.

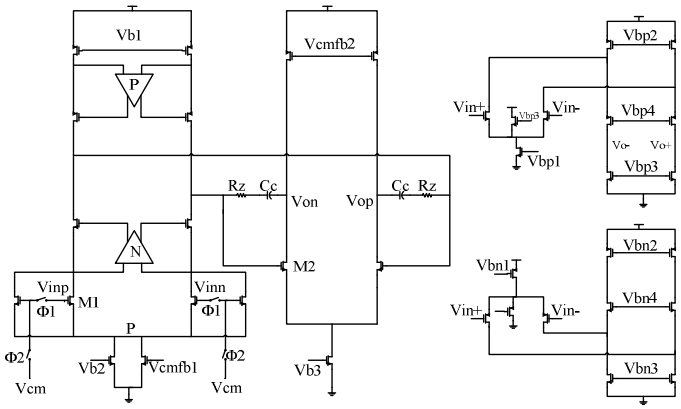

Figure 4. Two-stage op-amp with g_{m1}-controlled technique

A telescope op-amp with gain-boost technique is designed to achieve high DC gain and followed by a common-source differential circuit to reach high output swing. Input transconductance-controlled technique is used in the input differential pair to achieve stable settling. The open loop gain A_0 of the op-amp in figure 4 is shown in (7)

$$A_0 = g_{m1} g_{m2} R_{o1} R_{o2} \tag{7}$$

In which g_{m1}, R_{O1}, g_{m2}, R_{o2} represent the transconductance and output resistance of the first stage and the second stage of the op-amp, respectively. When the op-amp has a feedback factor β, the loop unity-gain-bandwidth and phase margin is shown in (8) and (9), where the dominant and non-dominant poles f_{p1} and f_{p2} are shown in (10) and (11)

$$GBW \approx f_{p1} \times A_0 \times \beta = \frac{g_{m1}}{2\pi C_C} \times \beta \tag{8}$$

$$PM = 90° - \arctan\frac{GBW}{f_{p2}} = \arctan\frac{f_{p2}}{GBW} \tag{9}$$

$$f_{p1} \approx \frac{1}{g_{m2} R_{o2} C_C \times R_{o1} \times 2\pi} \tag{10}$$

$$f_{p2} \approx \frac{g_{m2}}{C_L \times 2\pi} \tag{11}$$

As described in (9) and (10), the GBW in 1/2 feedback factor will be twice as much as the one of 1/4. Since f_{p2} is not changed, the PM will become too small in 1/2 feedback factor, which may decrease the stability of the circuit. G_{m1}-controlled technique is used to solve the problem. The equivalent circuit of the op-amp in both phases is shown in figure 5.

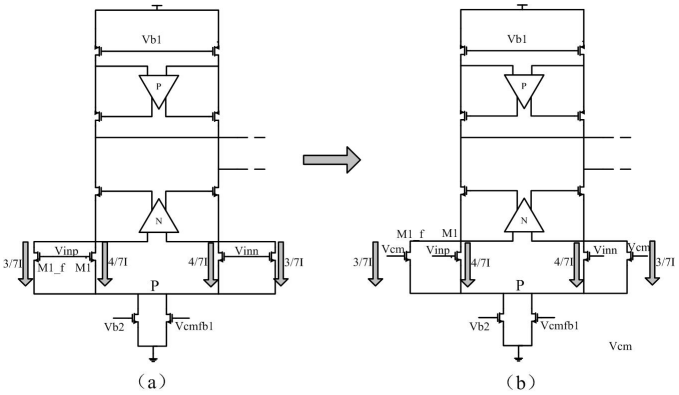

Figure 5. Equivalent circuit of the op-amp in both phases
(a) working in 1/4 feedback factor (b) working in 1/2 feedback factor

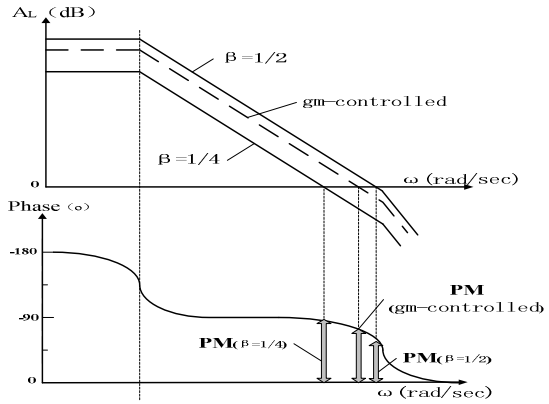

Figure 6. Bandwidth and phase margin of the shared op-amp with g_{m1}-control and without g_{m1}-control in the SMDAC

When the op-amp is working in 1/4 feedback factor, the switch Φ1 is closed, the gate of M1 and M1_f tied together to generate a large g_{m1} and GBW, as shown in figure 5(a). During the holding phase, the op-amp is working in 1/2 feedback factor, the switch Φ2 is closed and the gate of M1_f is tied to V_{CM} to generate a small g_{m1} and GBW, as shown in figure 5(b). The phase profile will not change too much during two feedback factors as the dominate and non-dominate pole is not changed. The bandwidth and phase margin of the shared op-amp in the SMDAC are illustrated in figure 6.

The solid line represents the loop gain of the shared op-amp working in different feedback factor without g_{m1}-control.

The phase margin at the holding mode of the S/H is not sufficient due to the large β like (9). This can degrade the overall ADC performance. While the op-amp is working with g_{m1}-controlled technique, as the analysis above, the bandwidth and phase margin of the op-amp are not changed, while those of the S/H are improved due to the reduced g_{m1}. The performance of the g_{m1}-controlled op-amp is shown as the dotted line in figure 6. The phase margin of 60° can be reached based on this line.

The current in M1_f is chosen 75% of that in M1, so that the g_{m1} will reduce about 40% in S/H holding phase. Although the open loop gain and the loop gain bandwidth of op-amp are somewhat decreased, the op-amp of this work satisfies the stability at the holding mode of the S/H.

Compared to other g_m-controlled op-amps [5], the designed op-amp in this paper not only ensured the stability of the SMDAC, it can also make the node voltage of "P" in fugure5 invariable. A constant "P" keeps the overdrive voltage of the input pair invariable between two different feedback factors which can make further improvement on the performance of the SMDAC.

IV. SIMULATED RESULTS

The designed circuits are simulated by Cadence based on Chartered 0.18um 1P5M 1.8V CMOS process. The simulation results of gain and phase curve of the op-amp is indicated in figure 7.

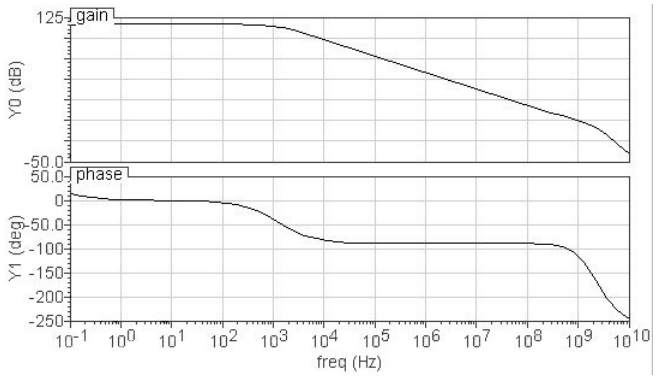

Figure 7. AC response of the op-amp

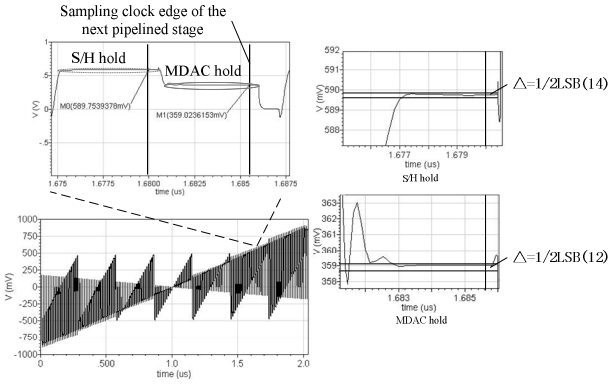

Figure 8. Transient response of the SMDAC output signal

The AC response of the op-amp in both 1/2 and 1/4 feedback factor are approximately the same according to the analysis above. Through the simulation, the loop gain of the op-amp A_{loop}=106dB, the loop unity-gain-bandwidth GBW_{loop}=1.05GHz. Both have enough margins compared to theoretical calculation. 61° phase margin ensures a quick and stable settling.

Transient response of the SMDAC output is shown in figure 8. The residue curve varies in the same modality shown in figure 2 as differential input slope signal varies from -7/8Vref to +7/8Vref (Vref=1V). The overshoot voltage and the under-damping behavior are due to the parasitic capacitance brought by switches and 61° phase margin, respectively.

According to the waveform of figure 8, the error of the first MDAC is only 0.1mV, which is far less than $1/2LSB_{12}$. The output signal in both holding and S/A phase can be settled in the required precision in 5ns. Total power consumption of the SMDAC is 75mW, about 50% reduced compared to the traditional S/H and first MDAC. It can also save considerable chip area.

V. CONCLUSION

An S/H merged with first MDAC used in 14bit 80Msps pipelined ADC is presented in this paper. Transconductance-controlled op-amp is shared in the proposed SMDAC to achieve high speed and stability. Simulation by cadence based on Chartered 0.18um 1P5M 1.8V CMOS process shows the S/H and first MDAC can both settled in required accuracy in 5ns. The power and chip area of the SMDAC is greatly reduced compared with the traditional ADC which can be used in low power, high resolution applications.

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REFERENCES

[1]. B. M. Min, P. Kim, D. Boisvert and A. Aude, "A 69mW 10b 80MS/s Pipelined CMOS ADC," ISSCC Dig. Tech.Papers, pp. 324-325, Feb 2003.

[2]. B. G. Lee, B. M. Min, G. Manganaro and J. W. Valvano, "A 14bit 100MS/s Pipelined ADC with a Merged Active S/H and First MDAC," ISSCC. pp. 248-249, Feb 2008.

[3]. R. Yin, X. Wen, Y. Liao, W. Zhang and Z. Tang, "Switch-embedded opamp-sharing MDAC with dual-input OTA in pipelined ADC," ELECTRONICS LETTERS, vol. 46, pp. 831-832, 2010.

[4]. R. Zhang, Y. S. Yin, S. Q. Liang and M. L. Gao, "A Multi-bit Digital-to-Analog Converter with Bi-directional overflow detection," ICSICT, pp. 427-429, 2010.

[5]. K. H. Lee, K. S. Kim and S. H. Lee, "A 12b 50MS/s 21.6mW 0.18um CMOS ADC Maximally Sharing Capacitors and Op-Amps," Transactions on circuits and systems, vol. 58, pp. 2127-2135, Sep 2011.