
Current Sensing Circuit Concepts and Fundamentals

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INTRODUCTION

Current sensing is a fundamental requirement in a wide range of electronic applications.

Typical applications that benefit from current sensing include:

- Battery life indicators and chargers
- Overcurrent protection and supervising circuits
- Current and voltage regulators
- DC/DC converters
- Ground fault detectors
- Linear and switch-mode power supplies
- Proportional solenoid control, linear or PWM
- Medical diagnostic equipment
- Handheld communications devices
- Automotive power electronics
- Motor speed controls and overload protection

This application note focuses on the concepts and fundamentals of current sensing circuits. It introduces current sensing resistors, current sensing techniques and describes three typical high-side current sensing implementations, with their advantages and disadvantages. The other current sensing implementations are beyond the scope of this application note and reserved for subsequent Microchip Technology Incorporated's application notes.

CURRENT SENSING RESISTOR

Description

A current sensor is a device that detects and converts current to an easily measured output voltage, which is proportional to the current through the measured path.

There are a wide variety of sensors, and each sensor is suitable for a specific current range and environmental condition. No one sensor is optimum for all applications.

Among these sensors, a current sensing resistor is the most commonly used. It can be considered a current-to-voltage converter, where inserting a resistor into the current path, the current is converted to voltage in a linear way of $V = I \times R$.

The main advantages and disadvantages of current sensing resistors include:

a) Advantages:

- Low cost
- High measurement accuracy
- Measurable current range from very low to medium
- Capability to measure DC or AC current

b) Disadvantages:

- Introduces additional resistance into the measured circuit path, which may increase source output resistance and result in undesirable loading effect
- Power loss since power dissipation $P = I^2 \times R$. Therefore, current sensing resistors are rarely used beyond the low and medium current sensing applications.

Selection Criteria

The disadvantages mentioned previously could be reduced by using low-value sensing resistors. However, the voltage drop across the sensing resistor may become low enough to be comparable to the input offset voltage of subsequent analog conditioning circuit, which would compromise the measurement accuracy.

In addition, the current sensing resistor's inherent inductance must be low, if the measured current has a large high-frequency component. Otherwise, the inductance can induce an Electromotive Force (EMF) which will degrade the measurement accuracy as well.

Furthermore, the resistance tolerance, temperature coefficient, thermal EMF, temperature rating and power rating are also important parameters of the current sensing resistors when measurement accuracy is required.

In brief, the selection of current sensing resistors is vital for designing any kind of current monitor. The following selection criteria can be used for guidance:

1. Low resistance with tight tolerance, to create a balance between accuracy and power dissipation
2. High current capability and high peak power rating to handle short duration and transient peak current
3. Low inductance to reduce the EMF due to high-frequency components
4. Low temperature coefficient, low thermal EMF and high temperature capability, if there is a wide temperature variation

CURRENT SENSING TECHNIQUES

This section introduces two basic techniques for current sensing applications, low-side current sensing and high-side current sensing. Each technique has its own advantages and disadvantages, discussed in more detail in the following topics.

Low-Side Current Sensing

As shown in [Figure 1](#), low-side current sensing connects the sensing resistor between the load and ground. Normally, the sensed voltage signal ($V_{SEN} = I_{SEN} \times R_{SEN}$) is so small that it needs to be amplified by subsequent op amp circuits (e.g., non-inverting amplifier) to get the measurable output voltage (V_{OUT}).

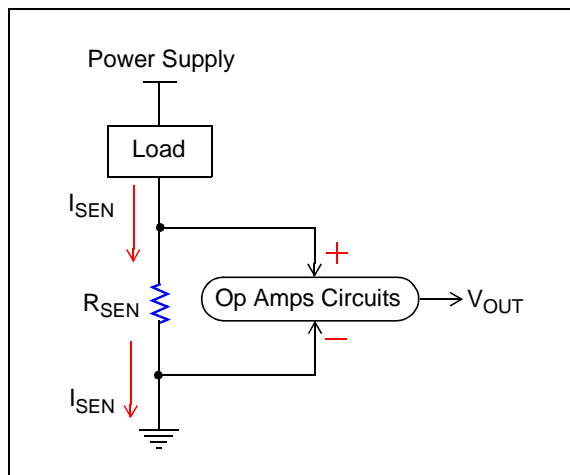


FIGURE 1: Low-Side Current Sensing.

- a) Advantages:
 - Low input Common mode voltage
 - Ground referenced input and output
 - Simplicity and low cost
- b) Disadvantages:
 - Ground path disturbance
 - Load is lifted from system ground since R_{SEN} adds undesirable resistance to the ground path
 - High load current caused by accidental short goes undetected
 - Low V_{DD} parts

In a single-supply configuration, the most important aspect of low-side current sensing is that the Common mode input voltage range (V_{CM}) of the op amp must include ground. The MCP6H0X op amp is a good choice since its V_{CM} is from $V_{SS} - 0.3V$ to $V_{DD} - 2.3V$.

Considering the advantages, choose low-side current sensing where short circuit detection is not required, and ground disturbances can be tolerated.

High-Side Current Sensing

As shown in Figure 2, high-side current sensing connects the sensing resistor between the power supply and load. The sensed voltage signal is amplified by subsequent op amp circuits to get the measurable V_{OUT} .

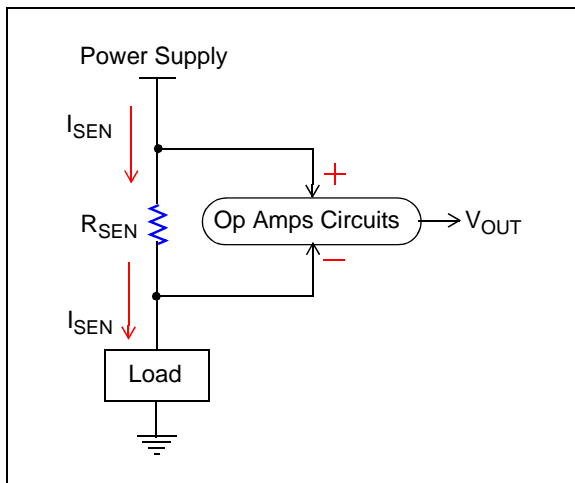


FIGURE 2: High-Side Current Sensing.

a) Advantages:

- Eliminates ground disturbance
- Load connects system ground directly
- Detects the high load current caused by accidental shorts

b) Disadvantages:

- Must be able to handle very high and dynamic Common mode input voltages
- Complexity and higher costs
- High V_{DD} parts

In a single-supply configuration, the most important aspects of high-side current sensing are:

- The V_{CM} range of the Difference amplifier must be wide enough to withstand high Common mode input voltages
- The Difference amplifier's ability to reject dynamic Common mode input voltages

The MCP6H0X op amp is a good fit for high-side current sensing, which will be discussed in more detail in the following section.

HIGH-SIDE CURRENT SENSING IMPLEMENTATION

High-side current sensing is typically selected in applications where ground disturbance cannot be tolerated, and short circuit detection is required, such as motor monitoring and control, overcurrent protection and supervising circuits, automotive safety systems, and battery current monitoring.

This section discusses three typical high-side current sensing implementations, with their advantages and disadvantages. Based on application requirements, one choice may be better than another.

Single Op Amp Difference Amplifier

Figure 3 shows a single op amp Difference amplifier that consists of the MCP6H01 op amp and four external resistors. It amplifies the small voltage drop across the sensing resistor by the gain R_2/R_1 , while rejecting the Common mode input voltage.

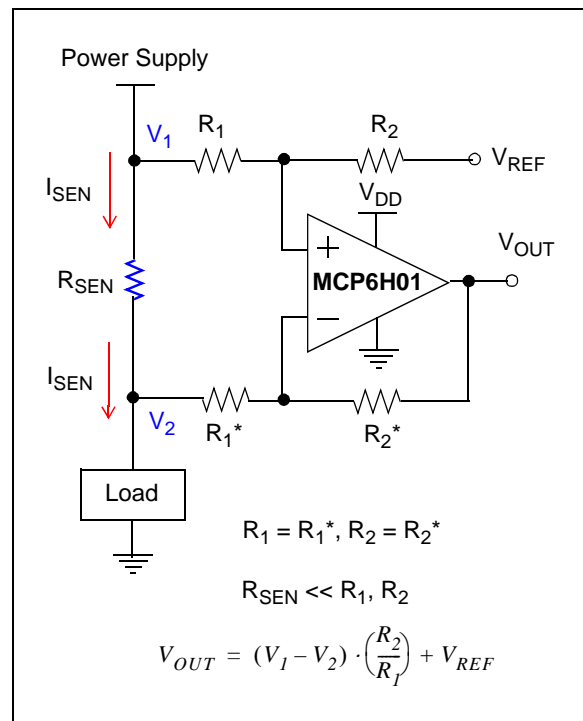


FIGURE 3: Single Op Amp Difference Amplifier.

The Difference amplifier's Common mode rejection ratio ($CMRR_{DIFF}$) is primarily determined by resistor mismatches (R_1, R_2, R_1^*, R_2^*), not by the MCP6H0X op amp's $CMRR$.

The resistor ratios of R_2/R_1 and R_2^*/R_1^* must be well matched to obtain an acceptable $CMRR_{DIFF}$. However, the tight tolerance resistors will add more cost to this circuit.

The DC $CMRR_{DIFF}$ is shown in Equation 1.

EQUATION 1:

$$CMRR_{DIFF} \approx 20 \log \left(\frac{1 + \frac{R_2}{R_1}}{K} \right)$$

$K = 4T_R$ in the worst case

Where:

T_R = Resistor Tolerance
 K = Net Matching Tolerance of R_2/R_1 to R_2^*/R_1^*
 $CMRR_{DIFF}$ (dB) = Common Mode Rejection Ratio of Difference Amplifier

Example 1

- If $R_2/R_1 = 1$ and $T_R = 0.1\%$, then the worst case DC $CMRR_{DIFF}$ will be 54 dB.
- If $R_2/R_1 = 1$ and $T_R = 1\%$, then the worst case DC $CMRR_{DIFF}$ will be only 34 dB.

Moreover, R_{SEN} should be much less than R_1 and R_2 in order to minimize resistive loading effect. The Difference amplifier's input impedances, seen from V_1 and V_2 , are unbalanced. Note that the resistive loading effect and the unbalanced input impedances will degrade the $CMRR_{DIFF}$.

The reference voltage (V_{REF}) allows the amplifier's output to be shifted to some higher voltage, with respect to ground. V_{REF} must be supplied by a low-impedance source, to avoid making $CMRR_{DIFF}$ worse.

In addition, as shown in Figure 3, the input voltages (V_1 , V_2) can be represented by Common mode input voltage (V_{CM}) and Difference mode input voltage (V_{DM}):

- $V_1 = V_{CM} + V_{DM}/2$ and $V_2 = V_{CM} - V_{DM}/2$
- $V_{OUT} = (V_1 - V_2) \times G + V_{REF} = V_{DM} \times G + V_{REF}$
 where $G = R_2/R_1$

In order to prevent V_{OUT} from saturating supply rails, it must be kept within the allowed V_{OUT} range between V_{OL} to V_{OH} .

The V_{CM} range of the Difference amplifier has been increased due to the resistor dividers made by R_1 , R_2 , R_1^* and R_2^* .

In brief, the V_{DM} and V_{CM} of the Difference amplifier must meet the requirements shown in Equation 2:

EQUATION 2:

$$\frac{V_{OL} - V_{REF}}{G} \leq V_{DM} \leq \frac{V_{OH} - V_{REF}}{G}$$

$$V_{CM} \geq (V_{CMRL} - V_{REF}) \cdot \left(1 + \frac{R_1}{R_2}\right) + \frac{V_{DM}}{2}$$

$$V_{CM} \leq (V_{CMRH} - V_{REF}) \cdot \left(1 + \frac{R_1}{R_2}\right) - \frac{V_{DM}}{2}$$

Where:

$G = R_2/R_1$; Gain of Difference Amplifier
 $V_{DM} = V_1 - V_2$; Difference Mode Input Voltage of Difference Amplifier
 $V_{CM} = (V_1 + V_2)/2$; Common Mode Input Voltage of Difference Amplifier
 $V_{OH} =$ Op Amp High-Level Output
 $V_{OL} =$ Op Amp Low-Level Output
 $V_{CMRH} =$ Op Amp Common Mode Input Voltage High Limit
 $V_{CMRL} =$ Op Amp Common Mode Input Voltage Low Limit

Example 2

Refer to Figure 3 and assume that $V_{DD} = 16V$, $V_{SS} = GND$, $V_{REF} = GND$, $R_2/R_1 = 1$, and the voltage drop across R_{SEN} is 200 mV.

Thus, according to the MCP6H01 data sheet (DS22243), it is $V_{CMRH} = V_{DD} - 2.3V = 13.7V$, $V_{CMRL} = V_{SS} - 0.3V = -0.3V$.

Based on Equation 2, the acceptable V_{CM} of the Difference amplifier is from -0.5V to 27.3V.

The advantages and disadvantages of Difference amplifiers include:

- Advantages:
 - Reasonable Common mode rejection ratio ($CMRR_{DIFF}$)
 - Wide Common mode input voltage range
 - Low-power consumption, low cost and simplicity
- Disadvantages:
 - Resistive loading effect
 - Unbalanced input impedances
 - Adjust the Difference amplifier's gain by changing more than one resistor value

Three Op Amp Instrumentation Amplifier

The three op amp instrumentation amplifier (3 op amp INA) is illustrated in Figure 4. It amplifies small Differential voltages and rejects large Common mode voltages.

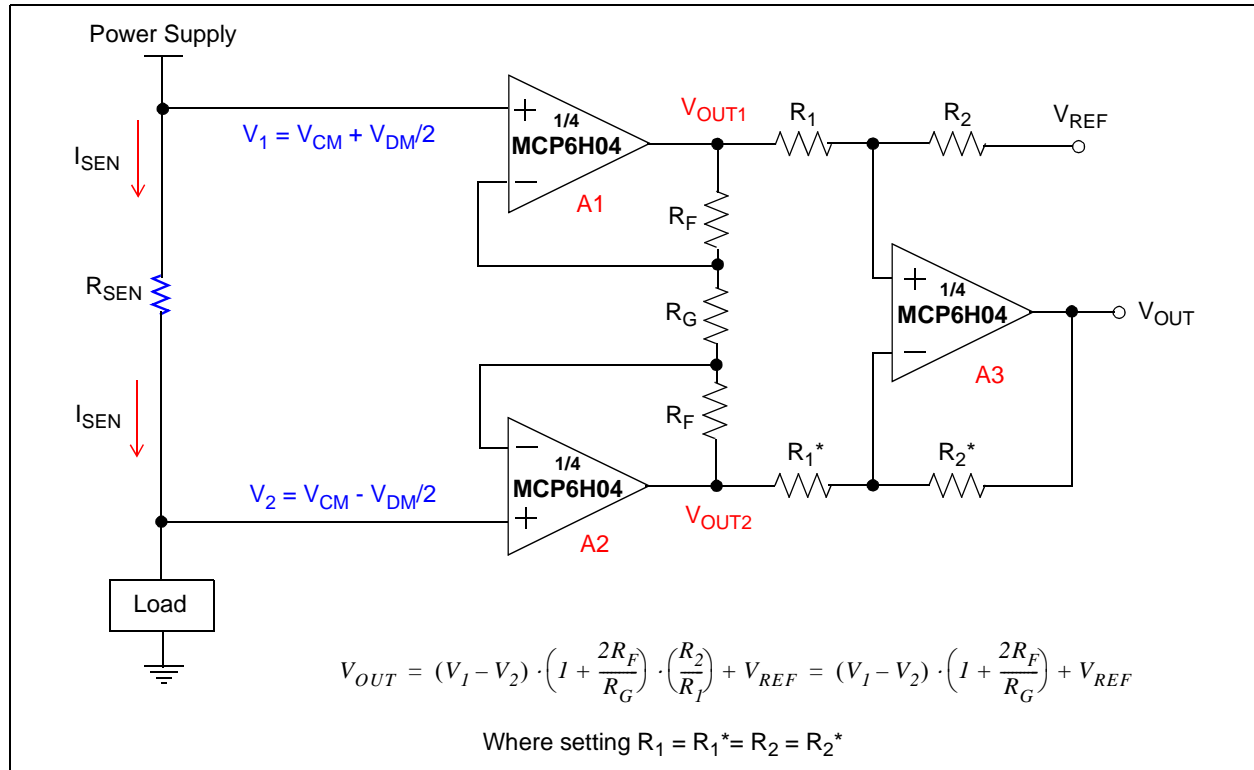


FIGURE 4: Three Op Amp Instrumentation Amplifier.

The 3 op amp INA's architecture includes the following:

1. First Stage

The first stage is implemented by a pair of high-input impedance buffers (A1, A2) and resistors (R_F and R_G). These buffers avoid both the input resistive loading effect and the unbalanced input impedances issue. In addition, the resistors R_F and R_G increase the buffer pairs' Difference mode voltage gains (G_{DM}) to $1 + 2R_F/R_G$ while keeping their Common mode voltage gains (G_{CM}) equal to 1.

One benefit of this method is that it significantly improves the 3 op amp INA's CMRR ($CMRR_{3INA}$), according to the equation $CMRR = 20 \log (G_{DM}/G_{CM})$. Thus, $CMRR_{3INA}$ will theoretically increase proportion to G_{DM} .

Another benefit is that the overall gain of the 3 op amp INA can be modified by adjusting only the resistance of R_G without having to adjust the resistors of R_1 , R_1^* , R_2 and R_2^* .

2. Second Stage

The second stage is implemented by a Difference amplifier (A3) which amplifies the Difference mode voltage and rejects the Common mode voltage. In a practical application, the R_2/R_1 ratio is usually set to 1.

The $CMRR_{3INA}$ is primarily determined by the Difference mode voltage gain of the first stage and net matching tolerance of R_2/R_1 and R_2^*/R_1^* . Note that the tolerance of resistors R_F and R_G do not affect $CMRR_{3INA}$.

The DC CMRR_{3INA} is shown in Equation 3.

EQUATION 3:

$$CMRR_{3INA} \approx 20 \log \left(\frac{\left(1 + \frac{2R_F}{R_G}\right) \cdot 2}{K} \right)$$

$K = 4T_R$ at the worst case

Where:

T_R = Resistor Tolerance

K = Net Matching Tolerance
of R_2/R_1 to R_2^*/R_1^*

CMRR_{3INA} (dB) = Common Mode Rejection
Ratio of 3 op amp INA

However, for the 3 op amp INA, there is a common issue that can be easily overlooked. This issue exists in the reduced Common mode input voltage range (V_{CM}) of the 3 op amp INA.

Referring to Figure 4, the input voltages (V_1 , V_2) can be represented by Common mode input voltage (V_{CM}) and Difference mode input voltage (V_{DM}). That is $V_1 = V_{CM} + V_{DM}/2$ and $V_2 = V_{CM} - V_{DM}/2$.

The amplifiers (A1, A2) provide a Difference mode voltage gain (G_{DM}), which is equal to the overall gain (G), and a Common mode gain (G_{CM}) equal to 1.

$$\begin{aligned} V_{OUT1} &= V_{CM} \times G_{CM} + (V_{DM}/2) \times G_{DM} \\ &= V_{CM} + (V_{DM}/2) \times G \end{aligned}$$

$$\begin{aligned} V_{OUT2} &= V_{CM} \times G_{CM} - (V_{DM}/2) \times G_{DM} \\ &= V_{CM} - (V_{DM}/2) \times G \end{aligned}$$

$$V_{OUT} = V_{DM} \times G + V_{REF}$$

In order to prevent V_{OUT1} , V_{OUT2} and V_{OUT} from saturating supply rails, they must be kept within the allowed output voltage range between V_{OL} and V_{OH} .

Or, stated in another way, the V_{DM} and V_{CM} of the 3 op amp INA must meet the requirements shown in Equation 4.

EQUATION 4:

$$\begin{aligned} \frac{V_{OL} - V_{REF}}{G} &\leq V_{DM} \leq \frac{V_{OH} - V_{REF}}{G} \\ V_{OL} + \frac{V_{DM}}{2} \cdot G &\leq V_{CM} \leq V_{OH} - \frac{V_{DM}}{2} \cdot G \end{aligned}$$

Where:

G = $1 + 2R_F/R_G$; Overall Gain

V_{DM} = $V_1 - V_2$; Difference Mode Input Voltage of
3 op amp INA

V_{CM} = $(V_1 + V_2)/2$; Common Mode Input Voltage
of 3 op amp INA

V_{OH} = Op Amp High-Level Output

V_{OL} = Op Amp Low-Level Output

Example 3

Refer to Figure 4 and assume $V_{REF} = 0V$, $V_{DD} = 15V$, $V_{SS} = 0V$, $V_{OH} = 14.47V$, $V_{OL} = 0.03V$, $R_F = R_1 = R_1^* = R_2 = R_2^* = 100 \text{ k}\Omega$, $R_G = 2 \text{ k}\Omega$, and the voltage drop across R_{SEN} is 100 mV.

Thus, the overall gain G is equal to 100 V/V, and the voltage range left for the 3 op amp INA's V_{CM} is only from 5.03V to 9.47V, based on Equation 4. This range is smaller than MCP6H01 op amp's V_{CM} range, which is from -0.3V to 12.7V at $V_{DD} = 15V$.

In conclusion, the V_{CM} range of the 3 op amp INA will be significantly reduced when it operates in a high gain configuration.

The advantages and disadvantages of the 3 op amp INA include:

a) Advantages:

- High Common mode rejection ratio (CMRR_{3INA})
- No resistive loading effect
- Balanced input impedances
- Adjust the overall gain without needing to change more than one resistor value

b) Disadvantages:

- V_{CM} range of the 3 op amp INA is reduced
- Increased power consumption and costs, due to more op amps

Two Op Amp Instrumentation Amplifier

Figure 5 shows a 2 op amp instrumentation amplifier (2 op amp INA). Compared to the 3 op amp INA, the 2 op amp INA provides savings in cost and power consumption. The input impedances of the 2 op amp INA are also very high, which avoids the resistive loading effect and the unbalanced input impedances issue.

The Common mode rejection ratio of the 2 op amp INA ($CMRR_{2INA}$) is primarily determined by the overall gain and the net matching tolerance of R_2/R_1 and R_2^*/R_1^* .

The DC $CMRR_{2INA}$ is shown in Equation 5.

EQUATION 5:

$$CMRR_{2INA} \approx 20 \log \left(\frac{1 + \frac{R_2}{R_1}}{K} \right)$$

$K = 4T_R$ at the worst case

Where:

K = Net Matching Tolerance of R_2/R_1 to R_2^*/R_1^*

T_R = Resistor Tolerance

$CMRR_{2INA}$ (dB) = Common Mode Rejection Ratio of 2 op amp INA

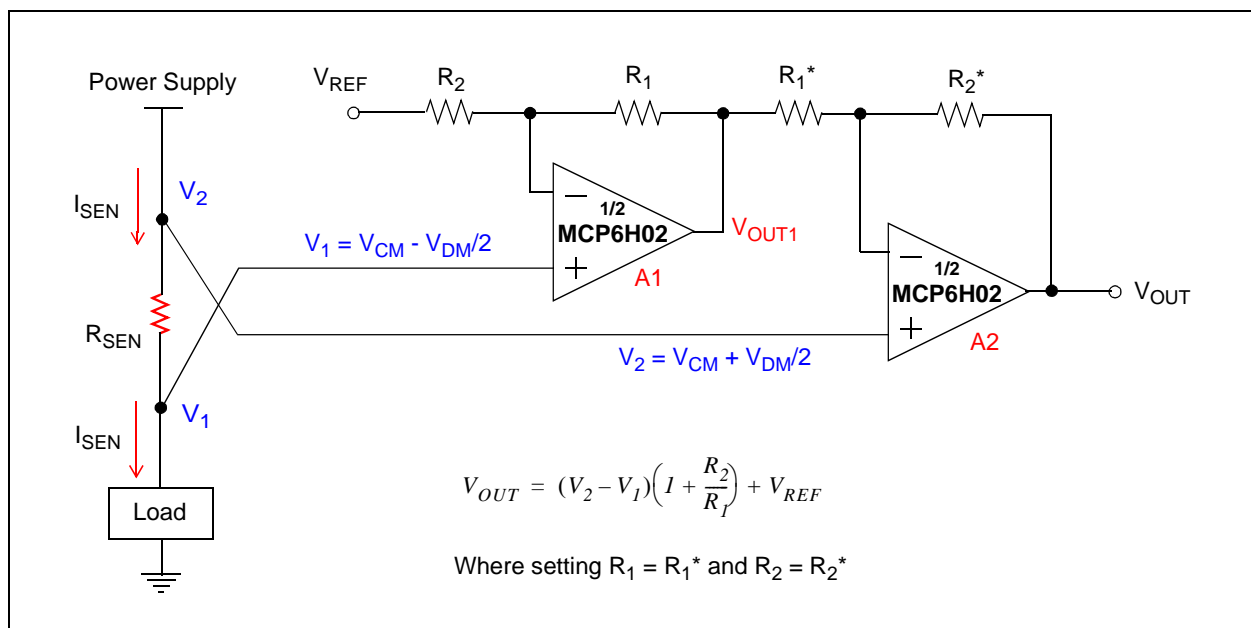


FIGURE 5: Two Op Amp Instrumentation Amplifier.

As shown in Figure 5, the input voltages (V_1 , V_2) can be represented by Common mode input voltage (V_{CM}) and Difference mode input voltage (V_{DM}). That is, $V_1 = V_{CM} - V_{DM}/2$, and $V_2 = V_{CM} + V_{DM}/2$.

$$\begin{aligned} V_{OUT} &= (1 + R_2/R_1) \times (V_2 - V_1) + V_{REF} \\ &= (1 + R_2/R_1) \times V_{DM} + V_{REF} \\ V_{OUT1} &= (1 + R_1/R_2) \times V_1 - (R_1/R_2) \times V_{REF} \\ &= (1 + R_1/R_2) \times (V_{CM} - V_{DM}/2) - (R_1/R_2) \times V_{REF} \\ V_{OUT} &= V_{DM} \times G + V_{REF} \end{aligned}$$

To prevent V_{OUT} and V_{OUT1} from saturating into supply rails, they must be kept within the allowed output voltage range between V_{OL} and V_{OH} .

The V_{DM} and V_{CM} of the 2 op amp INA must meet the requirements shown in Equation 6.

EQUATION 6:

$$\begin{aligned} \frac{V_{OL} - V_{REF}}{G} &\leq V_{DM} \leq \frac{V_{OH} - V_{REF}}{G} \\ V_{CM} &\geq \frac{V_{OL} + \frac{R_1}{R_2} \cdot V_{REF}}{G} + \frac{V_{DM}}{2} \\ V_{CM} &\leq \frac{V_{OH} + \frac{R_1}{R_2} \cdot V_{REF}}{G} + \frac{V_{DM}}{2} \end{aligned}$$

Where:

$$\begin{aligned} G &= 1 + R_2/R_1; \text{ Overall Gain} \\ V_{DM} &= V_2 - V_1; \text{ Difference Mode Input Voltage of 2 op amp INA} \\ V_{CM} &= (V_1 + V_2)/2; \text{ Common Mode Input Voltage of 2 op amp INA} \\ V_{OH} &= \text{Op Amp High-Level Output} \\ V_{OL} &= \text{Op Amp Low-Level Output} \end{aligned}$$

Example 4

Refer to Figure 5 and assume $R_1 = R_1^* = 5 \text{ k}\Omega$, $R_2 = R_2^* = 10 \text{ k}\Omega$, $V_{REF} = 0\text{V}$, $V_{DD} = 15\text{V}$, $V_{SS} = 0\text{V}$, $V_{OH} = 14.47\text{V}$, $V_{OL} = 0.03\text{V}$, and the voltage drop across R_{SEN} is 200 mV.

Thus, the overall gain G is equal to 3 V/V, and the voltage range left for the 2 op amp INA's V_{CM} is from 0.12 V to 9.75 V. This range is smaller than the MCP6H01 op amp's V_{CM} range, which is from -0.3V to 12.7V at $V_{DD} = 15\text{V}$.

Unlike the 3 op amp INA, the V_{CM} range of the 2 op amp INA will be significantly reduced when it operates in a low-gain configuration.

Moreover, the circuit's asymmetry in the Common mode signal path of the 2 op amp INA causes a phase delay between V_{OUT1} and V_1 , degrading the AC CMRR performance. Referring to Figure 5, the input signal V_1 must pass through amplifier A1 before it can be subtracted from V_2 by amplifier A2. Thus, the V_{OUT1} is slightly delayed and phase shifted with respect to V_2 . This is a big disadvantage of 2 op amp INA.

Referring to Figure 6, by adding the resistor R_G between two inverting inputs, the overall gain of the 2 op amp INA can be easily set by adjusting only R_G instead of several resistors. Moreover, the R_2/R_1 ratio is usually chosen for the desired minimum gain.

Another benefit of adding the resistor R_G is that the large resistor value usage of R_2 and R_2^* can be avoided in very high-gain configurations.

The V_{DM} and V_{CM} of 2 op amp INA with additional R_G must meet the requirements shown in Equation 7:

EQUATION 7:

$$\begin{aligned} \frac{V_{OL} - V_{REF}}{G} &\leq V_{DM} \leq \frac{V_{OH} - V_{REF}}{G} \\ V_{CM} &\geq \frac{V_{OL} + \frac{R_1}{R_2} \cdot V_{REF} + \frac{R_1}{R_G} \cdot V_{DM}}{1 + \frac{R_1}{R_2}} + \frac{V_{DM}}{2} \\ V_{CM} &\leq \frac{V_{OH} + \frac{R_1}{R_2} \cdot V_{REF} + \frac{R_1}{R_G} \cdot V_{DM}}{1 + \frac{R_1}{R_2}} + \frac{V_{DM}}{2} \end{aligned}$$

Where:

$$\begin{aligned} G &= 1 + R_2/R_1 + 2R_2/R_G; \text{ Overall Gain} \\ V_{DM} &= V_2 - V_1; \text{ Difference Mode Input Voltage of 2 op amp INA} \\ V_{CM} &= (V_1 + V_2)/2; \text{ Common Mode Input Voltage of 2 op amp INA} \\ V_{OH} &= \text{Op Amp High-Level Output} \\ V_{OL} &= \text{Op Amp Low-Level Output} \end{aligned}$$

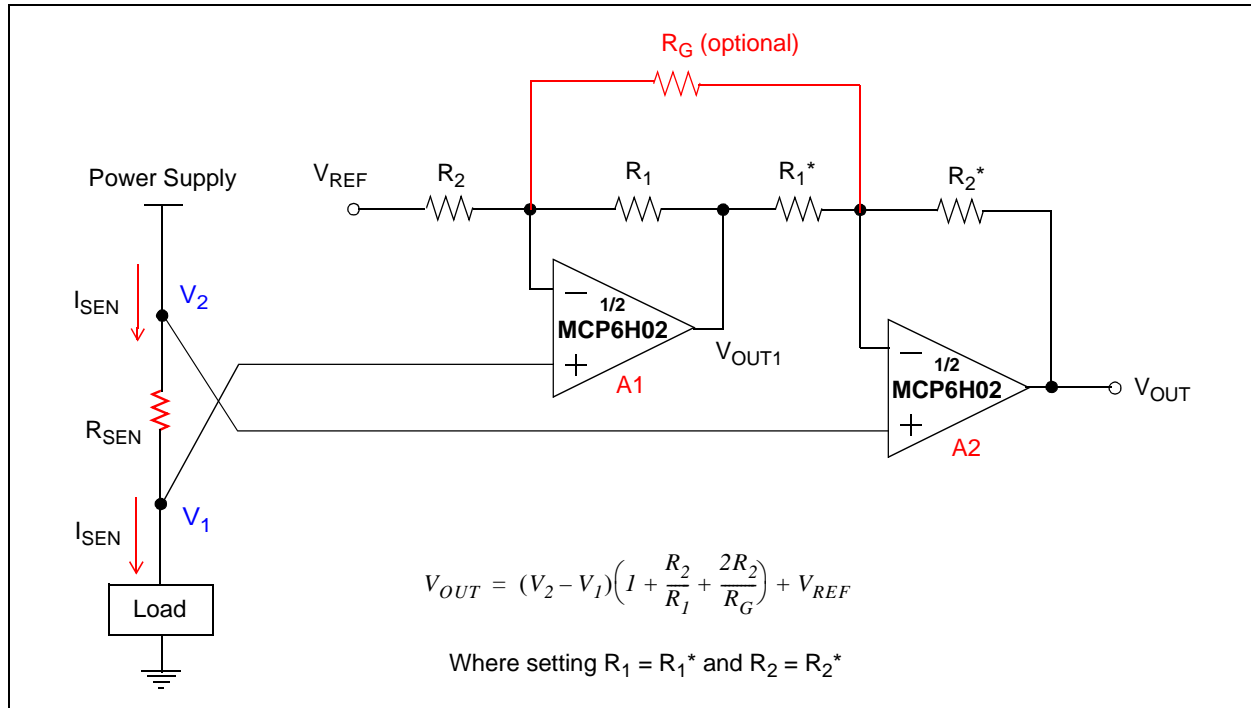


FIGURE 6: Two Op Amp Instrumentation Amplifier with Additional R_G

The advantages and disadvantages of the 2 op amp INA include:

- a) Advantages:
 - High DC Common mode rejection ($CMRR_{2INA}$)
 - No resistive loading effect
 - Balanced input impedances
 - Savings in cost and power consumption, compared to the 3 op amp INA
- b) Disadvantages:
 - Reduced V_{CM} range
 - Poor AC $CMRR_{2INA}$, due to the circuit's asymmetry
 - Unable to operate at unity gain

SUMMARY

This application note provides an overview of current sensing circuit concepts and fundamentals. It introduces current sensing techniques and focuses on three typical high-side current sensing implementations, with their specific advantages and disadvantages.

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REVISION HISTORY

Revision A (07/2010)

Original release.

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