Ultra High-Compliance CMOS Current Mirrors for Low Voltage Charge Pumps and References

O. Charlon[1] and W. Redman-White[1,2]

1. Philips Semiconductors, 1109, McKay Drive, San Jose, CA 95131, USA
2. Also with School of Electronics and Computer Science, University of Southampton, UK

Abstract:

We present a study of current mirror topologies for reference sources and PLL charge pumps, where the objective is to achieve excellent input to output DC matching over almost the whole available power supply range, while maintaining a very high output resistance. From the ideal requirements, we contrast existing designs and develop new topologies which come close to the ideal in terms of available range and resistance, by using regulation at the input as well as output. We consider noise, systematic and random and matching penalties in each circuit. It is shown that mirrors operating in triode region exhibit lower random mismatch compared with the equivalent conventional mirrors. Measured results are presented from a 0.25μm 2.5V CMOS test-chip.

1. Introduction

Current mirrors are one of the most common circuit primitives in the discipline of analogue IC design, and encapsulate many of the key issues of design in their operation. In particular, since the basic mirror relies critically on the concept of device matching, we see the performance limitations arising from the systematic and random device variations which affect all circuits on a larger scale. We also see the issue of circuit operation in a restricted power supply, which arises more frequently as CMOS technology scaling moves onwards.

In this paper we consider the key attributes of an ideal mirror and then examine some established circuit techniques to assess their performance and set benchmarks. We then propose two new circuits which we consider interesting for future low voltage designs.

2. Requirements in the Ideal Case

The characteristics of an ideal current mirror can be easily visualised as a rectangular function when plotting Iout versus Vout, as in Figure 1. In addition to the output possessing infinite output resistance, it is assumed that the output current is an exact copy for all possible values of voltage present at the output node, i.e., behave as an ideal current source notwithstanding the bias condition of any output device. In addition to these obvious points, the ideal mirror should have very large bandwidth and add no circuit noise.

3. Simple Mirror Limitations

We will review this case as a benchmark. For this study, all transistors that form the current mirrors have equal dimensions. The performance of the simple two-transistor mirror is limited by the characteristics of a single MOS transistor (Figure 5(a)). The output resistance is controlled directly by channel length modulation (and other short channel effects) as the output voltage varies, and is described in simple terms as

$$r_{OUT} \approx \frac{L}{\lambda I_D} \quad (1)$$

which is typically of the order of 10's-100's kΩ. Since the drain voltage of the output device and the input device only match at one output value, there is a systematic DC error in most applications. Random device mismatch has a direct impact on output current [1] without modification. Noise generated by the reference transistor is also copied to the output, such that

$$\overline{I_{NOUT}^2} = \frac{16}{3} k T g_m \quad (2)$$

For this reference design the RMS error in the output current is simulated as 3.3μA (Figure 5(c)). In most CMOS applications, the use of resistive source degeneration to reduce noise and improve matching is restricted due to headroom constraints.

4. Cascode Mirrors

The basic cascode offers an improvement in output resistance of the order of the intrinsic device gain, i.e.,

$$r_{OUT} \approx g_{m3} r_{DS3} r_{DS2} \quad (3)$$

but has a high minimum voltage for full performance. Many well known variants exist with a similar ideal output resistance and varying systematic offsets; the high compliance cascode in Figure 6a is generally the best with no systematic offset, and a random error as for the simple mirror. Note that the cascode does not add significant noise to the output current noise. There, the cascode mirrors noise can be approximated to equation (2). Simulated noise is shown in Figure 2. The minimum achievable output voltage is still no less than 2Vdsat (typically ~300-400mV). In low voltage applications, even this can be excessive. We therefore move on to consider circuits wherein additional gain is used to hold the output current constant down to very low output voltages.

5. Basic Regulated Cascode Mirror

The concept of the regulated cascode is to use feedback to ensure that the drain of the mirror transistor is held at some constant voltage in a feedback loop [3]. The circuit is often presented with a single MOS device M4 as the amplifier fed by a current source load. The reference voltage for the feedback loop is implicit in the operating point of M4; unless it has the same proportional size and current density as M1, there will be a difference between $V_{DS(M1)}$ and $V_{DS(M2)}$ and hence a systematic offset.

0-7803-8480-6/04/$20.00 ©2004 IEEE

An alternative implementation [1] uses a differential input servo amplifier, taking the input device as the reference (Figure 7(a)). This may seem a large overhead, but in reality a very simple low power amplifier design may be used especially for low frequency reference current applications (Figure 3).

In this form, the drain voltages of M1 and M2 match while

$$V_{OUT} \geq V_{GS(M1)} + V_{Dsat(M3)} \quad (4)$$

Under these conditions, the output resistance is given by

$$r_{OUT} \cong A\, r_{DS2}\, g_{m3}\, r_{DS3} \quad (5)$$

and there is no systematic current offset. The random offset is the same as in the simple mirror; the input offset of the servo amplifier A has only a second order impact via drain voltage, and this also relaxes the design requirements. The output noise is equivalent to the simple mirror case, since the amplifier noise is transferred to the output via M3, which is strongly degenerated by M2 in saturation. When the output voltage falls below that given in (4) M3 enters triode region (as shown in Figure 7(b)), and the output resistance will fall as g_{m3} and r_{ds3} are both falling, but if A is large, r_{OUT} will remain acceptable down to the point where $V_{DS(M3)}$ approaches zero. Further reduction in V_{OUT} means that $V_{DS(M2)}$ falls below $V_{DS(M1)}$, and so a systematic error appears in the output current; now the behaviour is directly comparable with a simple mirror, and the current source will collapse when $V_{OUT} < V_{Dsat(M2)}$.

6. High-Compliance Regulated Cascode Mirror

The output compliance range free of systematic offset may be extended (as in Figure 8(a)) by adding an additional device, M4, inside the drain-gate loop driving M1 [2]. This alters the reference of the servo amplifier A, such that the nominal operating point for M1 and M2 are with drain voltages close to V_{SS}, i.e., in triode region. The output resistance is still as given in (5), but since r_{ds2} is always at a low value, the gain A must be increased to compensate. An accurate current replication is achieved with $V_{OUT} > V_{DS(M1)}$, where the limit is typically of the order of 70mV, while the small-signal output resistance can be made acceptably high up to $V_{OUT} = V_{DD}$, making this an attractive option. When the output voltage falls below $V_{DS(M1)}$, the circuit rapidly fails and a large current error develops.

Monte-Carlo analysis shows that the RMS current error is 2.3μA, significantly less than the comparable simple mirror (Figure 8(c)); this might be counter intuitive, but it is mainly because a higher gate voltage is needed for M1 and M2 to pass the same DC current. The random mismatch between two MOS transistors is due to both differences in threshold voltage (Vt) and current factor (β) [4]. For low gate voltages, the threshold voltage mismatch dominates the overall random mismatch. Hence an increase in gate voltage results in a lower random mismatch. The output current noise is slightly higher at

$$\overline{I_{NOUT}^{\,2}} = \frac{8kT}{r_{Triode}} + \frac{\overline{V_{N(OpAmp)}^{\,2}}}{r_{Triode}^{\,2}} \quad (6)$$

since the amplifier noise is again converted into current noise at the output via M3, but now the degeneration provided by the output resistance of M2 is minimal as it is in triode region.

7. Regulated Input Current Mirror

As an alternative approach for high compliance, we propose investigation of the control the drain voltage of the input device, so as to force this to match that seen at the output. Figure 9(a) shows one possible scheme. With a simple output one can see that excellent matching is possible while the output voltage remains in the range

$$V_{OUT} \leq V_{GS(M1)} \quad (7)$$

with <1% systematic matching maintained down to ~5mV. M1 runs into triode region for part of this range, as does M3, but the output resistance in this range is maintained at greater than

$$r_{OUT} \cong A\, r_{DS2(Triode)} \quad (8)$$

Above the range in (7), the input servo loop is constrained by the gate terminal of M1, and a significant error develops; the output current rises with V_{OUT} in the same manner as in a simple mirror, and the random current error is essentially the same at 3.3μA (Figure 9(c)).

This circuit can be improved significantly by adding a cascode to the output using the input gate voltage $V_{GS(M1)}$ as the reference, as shown in Figure 10(a). In this case, both M1 and M2 operate in triode region, since the cascode M4 holds the drain of M2 quite low under all conditions, and $V_{DS(M1)}$ must follow this. The systematic error between the conditions of M1 and M2 are thus eliminated and the current copy is theoretically ideal. Further, the output resistance is maintained at a high value over the whole output range. When V_{OUT} is above the saturation point of M4, the value is

$$r_{OUT} \cong A\, g_{m3}\, r_{DS3}\, r_{DS2(Triode)} \quad (9)$$

and when V_{OUT} is below this level, the resistance is still quite high, as in the previous circuit when in its low offset mode. An additional benefit is that the random current error is reduced to 2.4μA RMS, again due to the reduced impact of Vt variations in triode region.

Although the latter circuit offers impressive performance both in terms of its high compliance with low systematic error, and maintaining output resistance high over the whole range, it has some penalty in the form of the output current noise. As in the case of the high compliance regulated cascode, the triode region devices mean that the noise from the op-amp is no longer subject to a large degeneration through the cascode transistor it drives, and so the noise also follows (6).

8. Regulated Input, Regulated Output Mirror

When V_{OUT} is high compared with a MOS saturation voltage, the use of an output regulation cascade is clearly advantageous, since the achievable resistance is extremely high, and there is negligible noise penalty. On the other hand, to achieve very large compliance range right down to V_{SS}, it is important to control the V_{DS} value at the input MOS device as the output device's drain is forced towards V_{SS}.

In Figure 11(a) we propose another new circuit wherein regulation is applied to both the input and the output, although in reality only one loop is controlling the circuit operation at any given time. Consider the situation when VOUT is high compared with $V_{Dsat(M4)}$. $V_{DS(M2)}$ will tend to be high, and so the loop driven by A1 will make the gate voltage of M3 large, such that it is in triode region with low channel resistance in series with the input current path, and hence with negligible effect on the input side. Now, with both of the MOS devices on the output side in saturation, and with regulation loop of A2 active, the output resistance is extremely high, as for the regulated cascode in section 5, and is also given by (5). Note that the while the drain voltages of M1 and M2 are not precisely the same since the loop driven by A1 is at its limit, the error is very small and the systematic DC error is negligible.

When VOUT is lower than the saturation voltage of M4, the output of A1 will go high to try to keep the drain voltage of M2 matched to the gate voltage of M1, so losing the effect of this loop. Hence $V_{DS(M2)}$ will start to fall, and now A1 begins to have an effect, reducing $V_{DS(M1)}$ to match. This latter loop remains operative until VOUT almost reaches VSS, in our example down to 5mV from VSS. Consequently, by ensuring that M1 and M2 always see the same terminal voltages, the output current is an accurate copy of the input current.

9. Measurements and Conclusions

The circuits were fabricated in a 0.25μm 2.5V CMOS technology using identical device sizes for each of the example circuits. The die photograph is given in Figure 4.

The current mirrors measurement results are presented in Figure 5-11(d) for five samples. The measured output current versus output voltage agrees with well simulated results. The Regulated Input regulated current mirrors provide an accurate current copy down to 35mV output voltage (Figures 9(d), 10(d) and 11(d)).

Two new input regulated current mirrors have been developed. It is shown that regulation of input reference device drain voltage to match output conditions is a useful strategy for achieving very high compliance. The Regulated Input Cascode current mirror (section 7) offers good output resistance over a very wide output voltage range and lowest random mismatch, albeit with a slight noise penalty. The Regulated Input, Regulated Output current mirror (section 8) offers the highest output resistance over a very wide output voltage range while imposing no noise penalty.

10. References

[1] K. Vilhelm, "Regulated cascode current mirror", European Patent 0356570, Sept. 1988.

[2] R. L. Barrett et al., "Current mirror and self-starting reference current generator", U.S. Patent 5612614, March 1997.

[3] T. Serrano et al., "The active-input regulated-cascode current mirror", IEEE Trans. on Circ. and Syst., vol.41, pp.464-466, June 1994.

[4] M. J. M. Pelgrom et al., "Matching properties of MOS transistors", IEEE JSSC, vol.24, pp.1433-1440, Oct. 1989.

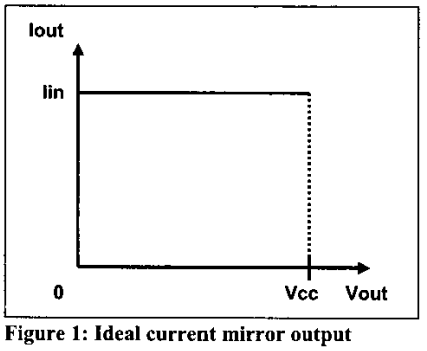

Figure 1: Ideal current mirror output current vs. output voltage

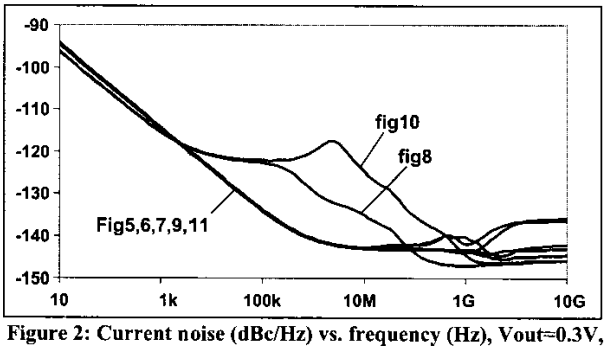

Figure 2: Current noise (dBc/Hz) vs. frequency (Hz), Vout=0.3V, Iin=100μA

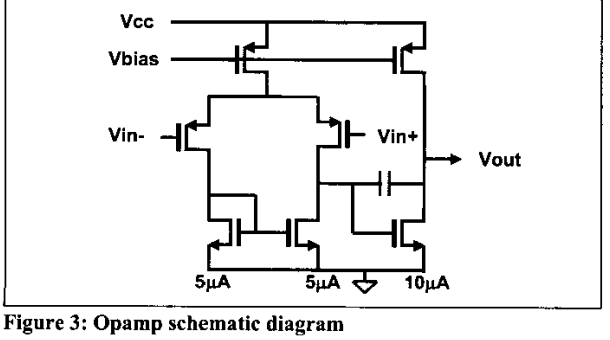

Figure 3: Opamp schematic diagram

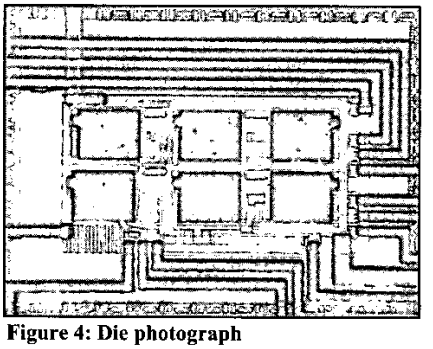

Figure 4: Die photograph

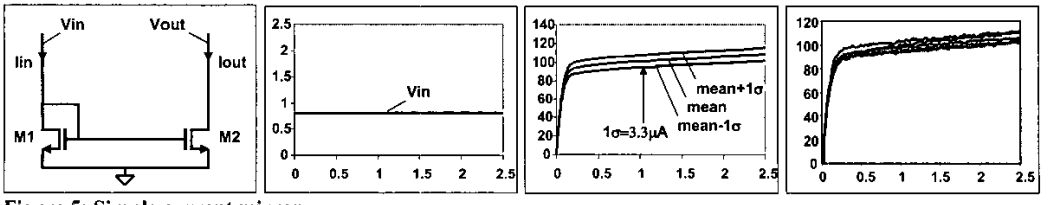

Figure 5: Simple current mirror

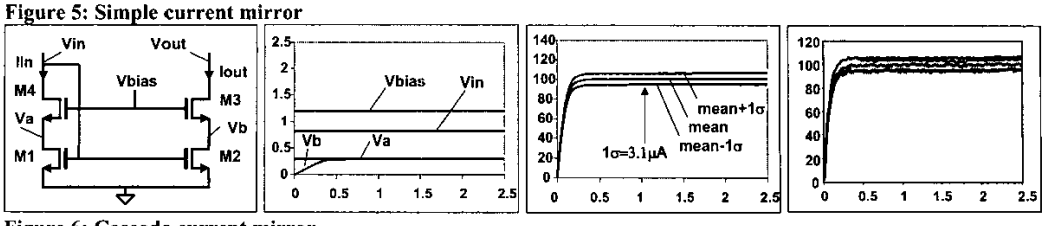

Figure 6: Cascode current mirror

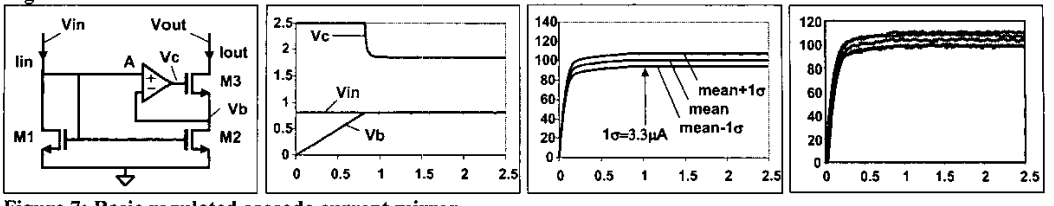

Figure 7: Basic regulated cascode current mirror

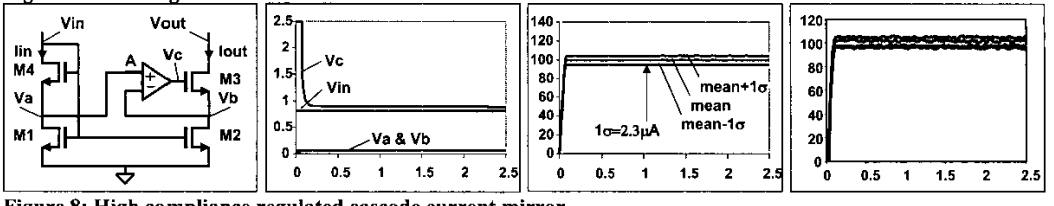

Figure 8: High compliance regulated cascode current mirror

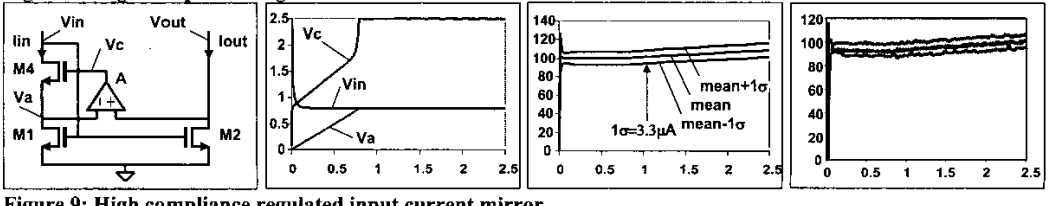

Figure 9: High compliance regulated input current mirror

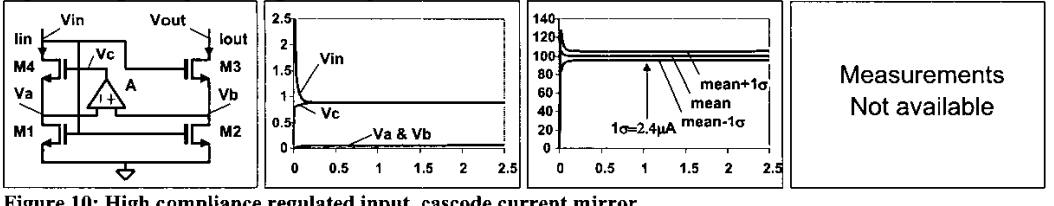

Figure 10: High compliance regulated input, cascode current mirror

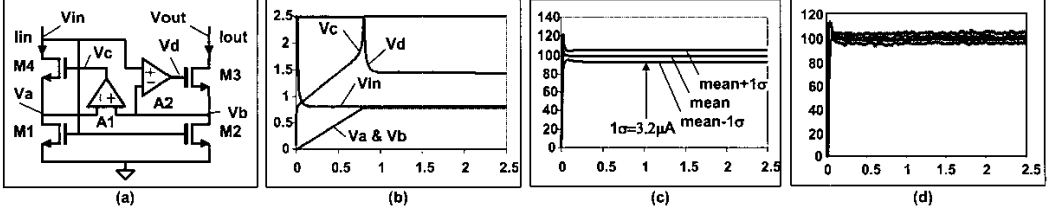

Figure 11: High compliance regulated input, output regulated current mirror

(a) Circuit diagrams - (b) Simulated node voltages (V) vs. output voltage Vout (V) - (c) Monte Carlo analysis: output current Iout (μA) vs. output voltage Vout (V) - (d) Measured output current Iout (μA) vs. output voltage Vout (V) for 5 samples. Conditions: Iin=100μA, Supply voltage=2.5V, all transistors W/L = 20μm/0.5μm